Infrared Microscopy of Joule Heating in Graphene Field Effect Transistors

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***Abstract*- We use infrared microscopy to image the temperature profile of graphene field-effect transistors operating at constant source to drain current bias. We find a peak in the temperature profile, i.e. a "hot spot" appears near the drain (anode) electrode of the graphene sheet at high current while operating in the hole-doped regime. We shift the hot spot position on the graphene sheet by tuning the gate voltage into an ambipolar transport regime. This shows a direct demonstration and manipulation of Joule heating in graphene transistors.**

BACKGROUND

Graphene is a monolayer of hexagonally arranged and sp^2-bonded carbon atoms. It is a two-dimensional system which shows novel phenomena such as an anomalous quantum Hall effect and Klein tunneling [1]. Amongst its novel electronic properties are a linear energy dispersion and a zero energy band gap. Because of its high electron mobility at room temperature [2], there is considerable interest in developing nanoscale graphene-based electronic devices. In graphene, the dominant carrier type and density are determined by the location of the Fermi level with respect to the band crossing (Dirac) point. Graphene becomes electron-doped when its Fermi level is shifted above the Dirac point and hole-doped when it is shifted below. This shift can be induced by chemical impurities and/or electrostatically when the electric potential is modified by the presence of charge traps or an applied electric field.

The Fermi level and electronic properties of graphene can be tuned with an external top or bottom gate. Thus, by varying the gate voltage (V_{GD}), the dominant charge carrier type and density can be changed in a reversible fashion, and one can build an ambipolar graphene field-effect transistor (GFET) which can go from n-type to p-type and back. When the source-drain bias (V_{SD}) is sufficiently high, there are pronounced variations of the electric potential profile along the channel of the GFET, leading to inhomogeneities in the spatial distribution of charge carrier types and densities.

Joule heating in a FET is a result of energy loss by the carriers to the lattice. Hence, the spatial distribution of Joule heating is determined by the local current density and electric field strength ($\boldsymbol{J}\cdot\boldsymbol{E}$), with regions of large local electric fields and current densities experiencing greater Joule heating [3]. The asymmetry in carrier densities and the non-uniformity of the electric field within the channel of a GFET at large V_{SD} implies that there will be regions of strong and weak Joule heating.

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In this study, we use infrared (IR) microscopy to image the spatial variation of Joule heating in two GFETs under constant source to drain (I_{SD}) current bias. We find a peak in the temperature profile in both samples; a "hot spot" appears near the drain electrode on the graphene sheet under high I_{SD} while operating in the hole-doped regime. By tuning V_{GD}, we can control the spatial variations in the carrier types and densities and hence, the spatial distribution of Joule heating within the channel. We find with increasing V_{GD} the hot spot jumps to the end of the current input electrode when operation switches from hole-doped to the electron-doped regime. Using IR microscopy, we map the inhomogeneous charge density profile along the ambipolar GFET channel under high V_{SD}.

FABRICATION AND EXPERIMENTAL METHODS

We use the mechanical exfoliation method to deposit graphene on a 300 nm layer of thermally grown SiO_2, on a highly n-doped Si substrate which serves as a back-gate [4]. Prior to deposition, the substrate is annealed in a chemical vapor deposition (CVD) furnace at 400 ºC for 35 minutes in Ar/H_2 to promote passivation of the SiO_2. After deposition, the sample is annealed again under the same conditions to remove residual organic materials from the exfoliation process [5]. Graphene is located using an optical microscope, and GFETs are fabricated by electron beam lithography techniques, as shown in Fig. 1 (device S1) and Fig. 4A (device S2). The electrodes are deposited on the graphene by electron-beam evaporation (0.6/20/20 nm Ti/Au/Pd for S1, and 5 nm/40nm Ti/Au for S2).

Electrical and thermal measurements are performed using a Keithley 2612 dual channel source-meter and the QFI Infrascope II infrared (IR) microscope, respectively. The IR imaging is performed using the IR scope's 15X objective which has a spatial resolution of 2.8 μm and a pixel size of 1.6 μm. The temperature resolution is approximately 0.1 °C. All imaging measurements for S1 and S2 are made with the IR scope stage

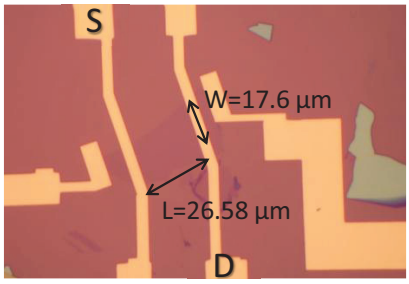

Fig. 1. Optical image of GFET S1 fabricated using mechanical exfoliation and electron beam lithography. The source (S) and drain (D) are as labeled.

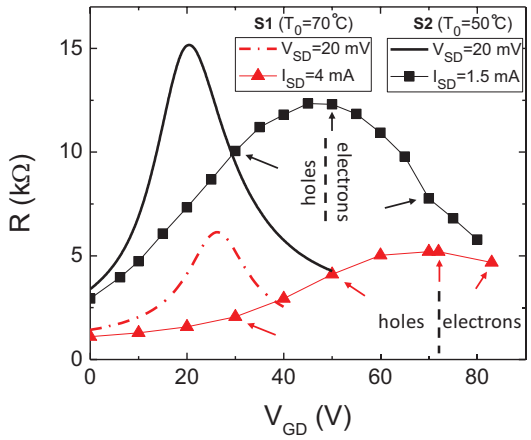

Fig. 2. Measured resistance (R) vs. gate voltage (V_{GD}) of two GFETs, S1 and S2: low-bias resistance (V_{SD} = 20 mV) and high-bias resistance at I_{SD} = 4 mA (S1) and 1.5 mA (S2) current flow. Small arrows indicate bias points where the data in Fig. 3 (S1) and Fig. 4 (S2) were taken. The location of the Dirac peak shifts with high bias conditions due to the high voltage and temperature which promote dielectric charging; the peak widens due to lower mobility at high temperature and electric fields.

temperature set to T_0 = 70 °C and 50 °C, respectively. The hot spot is monitored at current bias I_{SD} = 4 mA (S1) and 1.5 mA (S2), with varying gate voltages (V_{GD}), where the source (S) is floating and the drain (D) is ground. *For consistency, in this work we always refer to the ground electrode as the drain and the biased electrode as the source regardless of the majority carrier type or direction of current flow.* V_{GD} is increased in steps from 0 to ~80 V as shown in Fig. 2. Prior to each temperature measurement, the IR microscope is calibrated using a one-temperature emissivity method with I_{SD} = 0 [6].

RESULTS

Typical low-bias resistance vs. gate voltage (R-V_{GD}) measurements of S1 and S2 are performed at temperatures of 70 °C and 50 °C, respectively, with a low bias (V_{SD} = 20 mV) as shown in Fig. 2. In both cases, the *peak* resistances of the GFETs can be obtained at certain gate voltages, V_0 = 26.2 V for S1 and 20.5 V for S2, corresponding to minimum charge density, and the Fermi level near the GFET Dirac point. Gate voltages below and above V_0 provide holes and electrons for the majority carriers, respectively. The local graphene charge density is approximately $C_{ox}(V_{GX} - V_0)$, where X is any point along the channel between S and D, and $C_{ox} = \epsilon_{ox}/t_{ox}$ is the SiO_2 capacitance per unit area. The sheet resistivities of S1 and S2 (adjusted for aspect ratio differences) near the Dirac point are 4.1 kΩ and 4.4 kΩ, respectively. The similar resistivity values in the two different samples imply that our devices have similar carrier densities in electron-hole puddles along the graphene sheet [7]. First, we note that at low V_{SD} (20 mV) the electrostatic potential, and hence the carrier type and density, change uniformly throughout the graphene.

On the other hand, under high current bias with I_{SD} = 4 mA (1.5 mA) in S1 (S2), the peak resistance is found at V_{GD} = 72 V (47.5 V) with a broader peak width, as shown in Fig. 2. This may be attributed to Joule heating and some charge trapping in the graphene sheet under high I_{SD}, as also noted by previous studies [8]. While sweeping the gate voltage with constant current I_{SD}, V_{SD} varies from ~5 to ~25 V for both samples. The high V_{SD}, comparable to V_{GD}, induces a spatial variation of the Fermi level in the graphene channel. This gives rise to changes in the carrier density and power dissipation in the channel. In turn, this results in a spatial modulation of the graphene temperature, which is examined with the IR microscope for S1 and S2, under constant current (I_{SD}) conditions.

Fig. 3 shows IR imaging of the GFET for V_{GD} = 0 V, 50 V, 72 V and 83 V with I_{SD} = 4 mA of S1. These correspond to V_{SD} = 4.4 V, 16.4 V, 20.8 V, and 18.7 V, respectively. At V_{GD} = 0, the temperature distribution is nearly uniform throughout the GFET channel. With increasing V_{GD}, the charge (hole) density of the GFET decreases and its resistance goes up (Fig. 2). A hot spot develops near the drain electrode (right side) of the GFET operating in the hole doped regime. At V_{GD} = 50 V, the hot spot reaches an *imaged* peak temperature of about 110 °C (see Discussion on temperature below) on the right side of the graphene channel, as indicated by the arrow in Fig. 3B. Figure 3B also shows another hot spot in the middle of the graphene.

When V_{GD} = 72 V, the GFET reaches a maximum resistance as shown in Fig. 2, as the hole density reaches a minimum, and before electron-dominant conduction begins. The corresponding temperature profile is shown in Fig. 3C, where another hot spot is now formed on the *left* side of the GFET near the source electrode. As V_{GD} increases to 83 V and electrons become the dominant carriers, the hot spot near the drain disappears and two hot spots (left and middle) remain (Fig. 2). In other words, the hot spot is shifted from near the drain to near the source

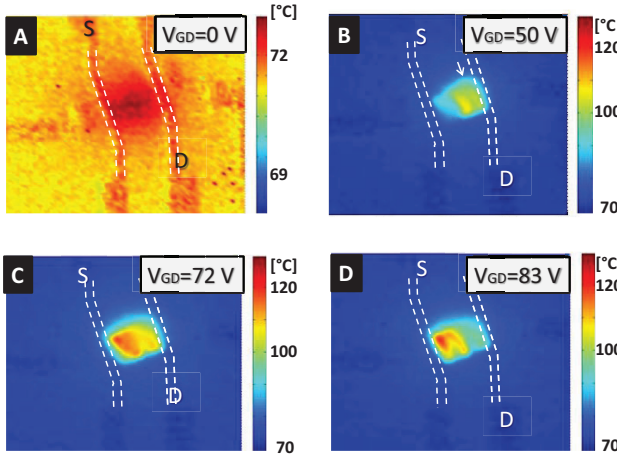

Fig. 3. Imaged temperature distribution below S1 (see Discussion) with back gate voltages, V_{GD} = 0 V **(A)**, 50 V **(B)**, 72 V (C), and 83 V **(D)** for I_{SD}=4 mA at background temperature 70°C. All images taken on same area, white dashed lines indicate the boundary of the metal electrodes. Also see Fig. 1.

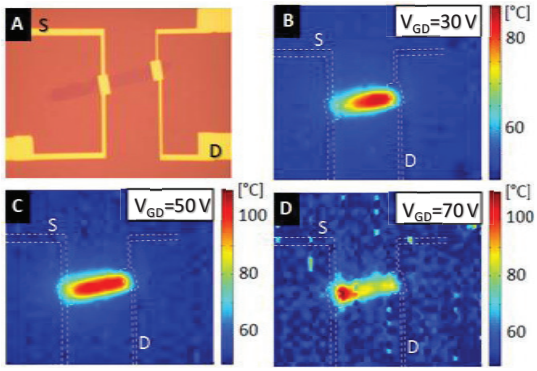

Fig. 4. (A) Optical image of GFET S2 (W= 6.5 μm, L=22.6 μm). Temperature distribution in GFET S2 with various back gate voltages, V_{GD} = 30 V **(B)**, 50 V **(C)**, and 70 V **(D)** for I_{SD}=1.5 mA at a background temperature of 50°C. All images were taken of the same area, where white dashed lines indicate the boundary of the metal electrodes.

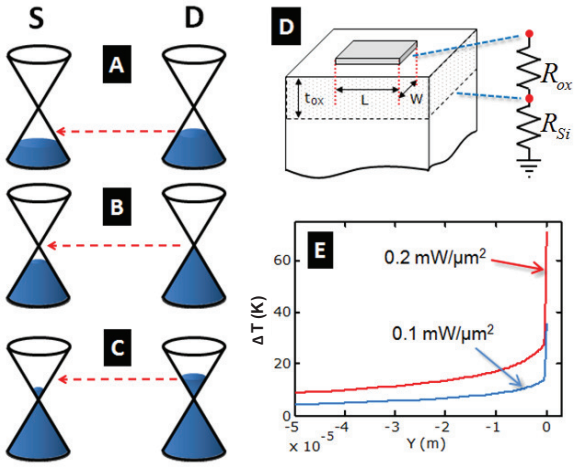

Fig. 5. Fermi level at the source, S and the drain, D with various gate voltage corresponding to **(A)** hole doped, **(B)** Dirac point, and **(C)** electron doped region. The dashed arrows indicate the Fermi level at the drain. **(D)** Schematic of the sample geometry, where a top gray box is graphene sheet, an area enclosed by dashed line is SiO_2 layer, and the underneath structure is the highly doped Si substrate. R_{ox}=1557 K/W and R_{Si}=513 K/W are thermal resistances of the SiO_2 layer and Si substrate, respectively (see Discussion).

when the dominant carrier type switches to electrons. In addition, the current flows in a non-uniform way in this relatively large and somewhat irregularly-shaped (unpatterned) graphene sheet, resulting in a current crowding behavior, represented by a deviated temperature profile near the drain as in Fig. 3C.

Figures 4B-D show IR images of the GFET S2 for V_{GD} = 30 V, 50 V, and 70 V with I_{SD} =1.5 mA. These correspond to V_{SD} = 13.2 V, 18.5 V, and 16.8 V, respectively. In this sample, the current crowding problem does not exist, probably due to the relatively narrow and more uniform width (6.5 μm) of the graphene sheet. As with sample S1, the sample S2 also shows the shift of the hot spot with various back gate voltages. In a hole doped region with V_{GD} = 30 V (see Fig. 2 and Fig. 4B), a hot spot is shown near a drain electrode. Near the Dirac point at V_{GD} = 50 V (Fig. 4C), the temperature profile is nearly uniform along the sheet. When the majority carrier type is changed from holes to electrons at V_{GD} = 70 V, the hot spot shifts to near the source electrode. The experiment was repeated with the source and drain electrodes swapped, and the same hotspot shift was observed.

Discussion: Electrostatics

The shift of the hot spot from changing V_{GD} suggests that the heating mechanism is due to energy loss by carriers in the graphene channel and not to contact resistance. To explain these observations, we consider the change of the Fermi level along the graphene channel with a high V_{SD} comparable to V_{GD}. Because the drain electrode is always ground by our convention, the Fermi level near the drain is always fixed under any bias condition. In the case of S2, with I_{SD} = 1.5 mA and V_{GD} = 30 V (hole doped region), the potential difference between the two electrodes is 13.2 eV. This potential difference lowers the Fermi level at the source end of the graphene with respect to that of the drain end of the graphene, as shown in Fig. 5A. The shift of the Fermi level occurs continuously along the channel, resulting in a continuous variation of the hole density along the channel. As a result, graphene near the drain has a lower hole density than that near the source. The hole density pinches off near the drain, resulting in higher local resistance. The highest power dissipation, therefore, occurs near the drain electrode so that the hot spot becomes localized near the drain. This is consistent with our observations in Figs. 3B (S1) and 4B (S2) in the hole doped regime.

Under constant current bias, increasing V_{GD} changes V_{SD}, and the charge carrier density profile along the channel. When the Fermi level crosses the Dirac point at a certain V_{GD}, as shown in Fig. 5B, the charge density at the drain is dominated by thermally generated carriers and electron-hole puddles [5]. Near the source end, the induced potential difference results in hole carriers. Although this picture suggests a hot spot near the drain, our observations show a broad temperature distribution along the graphene sheet as shown in Figs. 3C (S1) and 4C (S2). In the experiment, it was actually hard to fix the maximum resistance at a certain V_{GD} because the V_0 observed under a high I_{SD} of a few mA kept shifting to higher values [8]. This shift could be due to a charging effect by trapped charges between the graphene and the substrate. Thus, although we set V_{GD} to give the maximum resistance at the initial stage of the experiment, the carrier state can go to slightly hole doped region. In that case, the drain and source ends become hole doped near the neutral point. In this regime, as shown in Fig. 2, the spatial variation in the carrier density is less sensitive to V_{SD}, resulting in a near uniform temperature profile.

When $V_{GD} >> V_0$, i.e. the fully electron doped regime (Fig. 5C), the source has smaller carrier density than the drain end. One, thus, expects the hot spot to be localized near the source. Figures 3D (S1) and 4D (S2) show the hot spot near the source electrodes, which is consistent with our explanation.

DISCUSSION: Temperature

The temperature distribution along the graphene channel can be modeled with a 1-dimensional fin equation [9]. Given the dimensions and geometry of the device, this suggests that the temperature distribution has a healing length $L_H = (t_{ox}t_G k_G/k_{ox})^{1/2} \approx 0.3$ μm, where $t_G \approx 0.34$ nm is the graphene thickness and $k_G \approx 3000$ $Wm^{-1}K^{-1}$ is the graphene thermal conductivity [10]. The healing length is a measure of the lateral temperature diffusion from a heat source along the graphene. The small healing length means that the local heat generation in the graphene channel is minimally attenuated by lateral heat dissipation. In other words, there is little broadening of the hot spot, and most of the heat flow path is directly down through the 300 nm SiO_2 layer [8]. Thus, the temperature profile in the graphene qualitatively represents the heat generation profile.

We next turn to the question of the accuracy of the temperature measurement. The measured temperatures seem to be significantly lower than those consistent with the given power densities. To understand this discrepancy, let us first note that the IR scope determines the surface temperature of the sample by measuring IR radiation in the wavelength range of 2 to 4 μm [6]. However, the emissivity of graphene is estimated to be around 2.3 percent [8]. The low emissivity implies that the graphene emits a relatively small amount of the IR radiation detected, being effectively transparent to infrared at its sub-1 nm thickness. Thus, the bulk of the detected IR radiation must originate from below the graphene and it is necessary to consider the subsurface temperature profile.

A 300 nm SiO_2 layer is sandwiched between the graphene and the 500 μm-thick Si substrate. Most of the temperature drop from the graphene to the bottom of the substrate takes place within the SiO_2 layer (see Fig. 5E) because of its poor thermal conductivity. A schematic of the thermal resistances of the SiO_2 and the Si layers is shown in Fig. 5D, where $R_{ox} \approx t_{ox}/(k_{ox}WL)$ and $R_{Si} \approx 1/[2k_{Si}(WL)^{1/2}]$. We estimate the thermal resistance of the SiO_2 layer to be about 3 times greater than that of the Si substrate. Hence, the temperature rise in the Si substrate is much lower than that in the graphene, with the temperature rise in the graphene being roughly 4 times that in the Si substrate as seen in Fig. 5E.

More importantly, SiO_2, like graphene, is also transparent to IR radiation of wavelengths between 2 to 4 μm. Therefore, *the source of the detected IR radiation in fact originates in the Si substrate*. One immediate implication is that the IR scope does not measure the surface temperature of the graphene but rather that of the cooler Si substrate. Thus, the real temperature rise (ΔT) in the graphene is approximately 4 times that measured by the IR scope. *This observation applies to interpreting all raw imaged temperature data reported in Figs. 3 and 4.*

We also need to take into account the temperature variation within the Si substrate because the detected IR radiation does not simply originate from the top of the silicon but also from within. We estimate the 2 – 4 μm wavelength IR optical depths in heavily doped Si to be between 12 and 48 μm using the Free Carrier Absorption theory [11] with longer wavelength radiation (4 μm) having the shortest optical depth. In addition, a typical blackbody IR emission spectrum at these temperatures is heavily weighted towards these longer (4 μm) wavelengths, which have the shorter optical depth. The temperature profile in the Si also falls off roughly in a logarithmic fashion, implying the IR scope weighs and samples temperatures much closer to the Si/SiO_2 surface. To provide a numerical idea of the real temperature in the graphene FET, let us look at Fig. 4D. In Fig. 4D, the maximum measured (imaged) temperature in the hot spot is about 110 °C. However, after taking into account the IR transparency of the graphene and SiO_2 layers, as well as the temperature profile, we estimate the real graphene hot spot temperature to be around 300 °C. The numerical aspects of our estimates will be published in detail elsewhere [12].

CONCLUSION

In summary, we use an infrared (IR) microscope to image the hot spot formation in graphene transistors under high current bias. By varying the back gate voltage, we can control the position of the hot spot. We attribute the shift in the hot spot to modulations in the spatial distribution and the dominant type of the carriers in the graphene. These changes are determined by the electrostatics within the channel and ultimately, by the back gate and the source-drain voltage biases. We also consider the operating details of the IR scope. The imaged temperatures are lower than those consistent with the given power densities because graphene and SiO_2 are effectively transparent to IR radiation and the IR signal is detected largely from the top of the Si substrate, near the Si/SiO_2 interface. We estimate the real temperature rise (ΔT) in the graphene to be about 4 times that measured by the IR scope. Finally, we have shown that IR microscopy can be used to map the inhomogeneous charge density profile along the ambipolar GFET channel at high bias.

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