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Transport in Nanoribbon Interconnects Obtained from Graphene Grown by Chemical Vapor Deposition

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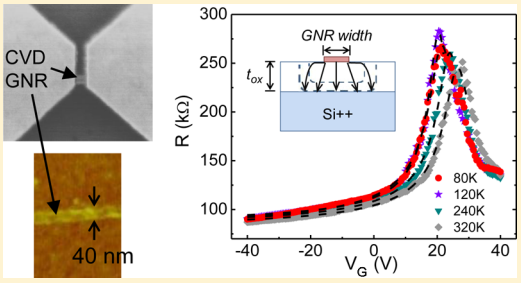
Supporting Information

ABSTRACT: We study graphene nanoribbon (GNR) interconnects obtained from graphene grown by chemical vapor deposition (CVD). We report low- and high-field electrical measurements over a wide temperature range, from 1.7 to 900 K. Room temperature mobilities range from 100 to 500 $cm^2 \cdot V^{-1} \cdot s^{-1}$, comparable to GNRs from exfoliated graphene, suggesting that bulk defects or grain boundaries play little role in devices smaller than the CVD graphene crystallite size. At high-field, peak current densities are limited by Joule heating, but a small amount of thermal engineering allows us to reach ~2 × 10^9 A/cm^2, the highest reported for nanoscale CVD graphene interconnects. At temperatures below ~5 K, short GNRs act as quantum dots with dimensions comparable to their lengths, highlighting the role of metal contacts in limiting transport. Our study illustrates opportunities for CVD-grown GNRs, while revealing variability and contacts as remaining future challenges.



KEYWORDS: *Graphene, nanoribbons, interconnects, current density, temperature*

Graphene nanoribbons (GNRs) are promising candidates for nanoelectronics building blocks as interconnects, transistors, or sensors.[1−4] Previous studies have characterized individual GNRs prepared from chemically derived,[1,2,5] mechanically exfoliated,[4,6] or epitaxially grown[7] graphene. However, these fabrication methods are less practical or more expensive for future large-scale integrated circuit fabrication. On the other hand, chemical vapor deposition (CVD) has been used as a facile approach for synthesizing large area polycrystalline graphene films[8−10] with grain sizes from tens of nanometers to micrometers.[11,12] CVD-grown graphene has been recently investigated as a promising material for micrometer-sized interconnects, either on complementary metal−oxide−semiconductor (CMOS)[13,14] or on transparent and flexible substrates.[15] However, nanometer scale GNR interconnects from CVD graphene have not been systematically studied to date. Such GNRs represent the ultimate scaling limits of graphene interconnects and could be comparable to or smaller than the average CVD graphene crystallite size, leading to few or no bulk defects in individual devices. This could achieve the dual purpose of large-scale fabrication with relatively good quality GNRs.

In this work we present a comprehensive analysis of nanoscale GNRs with widths W < 100 nm and lengths L < 800 nm obtained from patterned CVD graphene. We find that such CVD GNRs have electrical properties comparable to those obtained by any other methods, suggesting a negligible effect of bulk defects or grain boundaries on their performance. At high fields we attain some of the highest current densities recorded in either graphene or GNR interconnects (~2 × 10^9 A/cm^2); at low temperatures we note evidence of quantum dots with size comparable to the channel length, underlining how contacts determine the conductance levels in such nanoscale devices. This study also serves to identify future challenges and represents a fundamental stepping stone toward large-scale integration of nanoscale GNR interconnects.

Our CVD graphene growth and GNR device process steps are illustrated in Figure 1 and in the Supporting Information. Briefly, graphene is grown on Cu foil,[8] then transferred to SiO_2 (90 nm) on Si substrates (n+ doped), and annealed to remove water and organic residue. We define large Ti/Au (0.5/40 nm) contact pads (Figure S1 in the Supporting Information) using optical lithography, followed by smaller finger electrodes by electron-beam (e-beam) lithography. We then define and deposit a narrow "strip" of Al (2−4 nm thick) which serves as the etch mask for the GNRs (Figure 1c and Figure S1b). The thin Al oxidizes when the chip is removed from the evaporation chamber, and lift-off leaves behind an AlO_x nanoribbon

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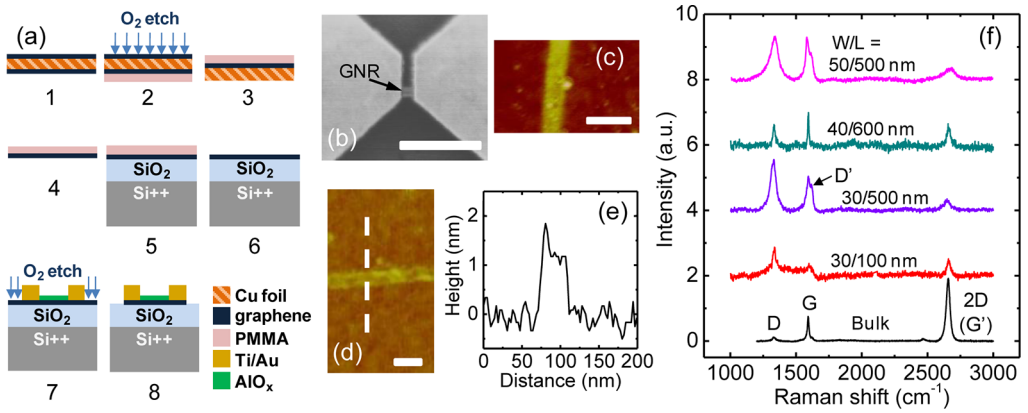

Figure 1. (a) Schematic of CVD graphene growth and GNR fabrication process. (b) Scanning electron microscope (SEM) image of a GNR ($W \sim 75$ nm, $L \sim 110$ nm) between two Ti/Au electrodes; scale bar = 1 μm. (c) Atomic force microscope (AFM) image of AlO_x strip covering a GNR ($W \sim 60$ nm); scale bar = 100 nm. Also see Figure S1. (d) AFM image of a GNR ($W \sim 35$ nm) after removal of the top AlO_x strip; scale bar = 50 nm. (e) Cross section of AFM profile along dashed line in d. The apparent topographic height in the 1−1.2 nm range (in air, including possible residue from fabrication) suggests the GNR is most likely monolayer, although a bilayer cannot be ruled out.[1,49] (f) Raman spectra (excitation wavelength 633 nm) for bulk CVD graphene (bottom curve) and several GNRs, spaced for clarity. The initial CVD graphene is predominantly monolayer (narrow 2D peak width ~35 cm^{-1}), while the D and D′ bands of GNRs are more prominent due to the presence of edges.

covering the graphene and stretching between the finger electrodes (Figure S1b,c). This AlO_x strip serves the multiple purpose of protecting the graphene, serving as a dielectric seeding layer, and being scalable for large-area fabrication. (Some, albeit not all these goals, could also be achieved with a thicker ~20 nm metal strip[16] or a nanowire mask[17,18] for etching the GNRs.) The GNRs are defined by a short O_2 plasma etch which removes the unprotected graphene. The graphene which fans out under the contacts (Figure 1b) is protected during the etch, helping manage contact resistance. The AlO_x strip was left on some devices (batch b1) and removed on others (batch b2) for the measurements.

Figure 1f compares the Raman spectrum of the unpatterned CVD graphene to several individual GNRs. All GNRs display the disorder-induced Raman D peak, and most also display the D′ peak, which are accentuated in GNRs due to the presence of edges.[19,20] The integrated D to G peak area ratio of our GNRs from CVD graphene is A_D/A_G ~1−5, comparable to A_D/A_G ~2−8 measured for arrays of GNRs from exfoliated graphene of similar widths.[19,20] For comparison, our bulk CVD graphene has $A_D/A_G \sim 0.2$. Using this ratio we can calculate the average crystallite size following Cancado et al.,[21] $L_a \sim 200$ nm or an average area ~4×10^4 nm^2. The length scale L_a approximately corresponds to the average distance between defects (including bulk defects and grain boundaries); thus it is smaller than the polycrystalline grain size in the CVD-grown graphene. Similar values were also recently estimated by scanning tunneling microscopy (STM) in our group, on comparable CVD graphene growths.[22] Thus, given GNR areas from 0.2×10^4 to 4×10^4 nm^2 in this work, it is highly likely that most samples are monocrystalline and free of bulk defects.

Low-bias measurements of both AlO_x-capped and bare CVD GNRs in air reveal similar *p*-doping (Supporting Information, Figure S2). Transferring devices to a vacuum probe station (~10^{-5} Torr) and annealing at 300 °C for 2 h removes most of the physisorbed ambient impurities such as water,[23] oxygen,[24] and poly(methyl methyacrylate) (PMMA) residue.[25] After annealing, measurements in vacuum show devices are less *p*-doped than in air and in some cases *n*-doped (Figure S2b). We note that our vacuum probe station has high-temperature capability, enabling electrical measurements after sample anneal, without breaking vacuum. We fit all electrical data with a transport model[26,27] which includes the gate dependence (V_G), thermally generated carriers (n_{th}), puddle charge (n_{pd}) due to substrate impurities, and contact resistance (R_C) effects. (More information is provided in Section C of the Supporting Information.) Since GNRs are narrow compared to the underlying oxide thickness, the effect of fringing fields on the capacitance must be included[2,28] (Figure 2a inset). Thus, we use an expression for the capacitance per unit area as:[2]

$$C_{ox} \approx \varepsilon_{ox}\varepsilon_0\left\{\frac{\pi}{\ln[6(t_{ox}/W+1)]W} + \frac{1}{t_{ox}}\right\} \quad (1)$$

where $t_{ox} \approx 90$ nm is the SiO_2 thickness, $\varepsilon_{ox} \approx 3.9$ is the relative permittivity of SiO_2, and $\varepsilon_0 \approx 8.854 \times 10^{-14}$ F/cm is the permittivity of vacuum. The first term represents the fringing capacitance, and the second term is the parallel plate capacitance between the GNR and the top of the n+ Si substrate. As an example, for a GNR with $W = 40$ nm on $t_{ox} = 90$ nm, ~72% of the total capacitance is due to fringing fields and the rest due to parallel plate capacitance. In the limit $W \gg t_{ox}$, the equation reduces to the usual $C_{ox} = \varepsilon_{ox}\varepsilon_0/t_{ox}$ as expected, and quantum capacitance[29] can be neglected due to the thickness of the buried oxide. (Figure S3 in the Supporting Information illustrates the contribution of fringing capacitance to the total capacitance as a function of *W*.)

Fitting our model against the experimental data reveals a mobility range $\mu \approx 100-500$ $cm^2 \cdot V^{-1} \cdot s^{-1}$ and contact resistance $R_C W \geq 500$ $\Omega \cdot \mu m$ at room temperature (per width), for these GNRs obtained from CVD-grown graphene.[30] The mobility values of our CVD GNRs are comparable to lithographically patterned GNRs from exfoliated graphene[4] (100−1000 $cm^2 \cdot V^{-1} \cdot s^{-1}$) and somewhat lower than GNRs from unzipped nanotubes[1,2,31] (100−3200 $cm^2 \cdot V^{-1} \cdot s^{-1}$), ostensibly due to lesser edge disorder of the latter. However, the similarity of mobility for exfoliated versus CVD-grown graphene does not exist for larger samples, as micrometer-scale (polycrystalline) CVD graphene devices consistently show lower mobility than (crystalline) exfoliated ones.[26,32] This suggests that bulk defects or grain boundaries play almost no role in lowering our GNR mobility, a consequence of the

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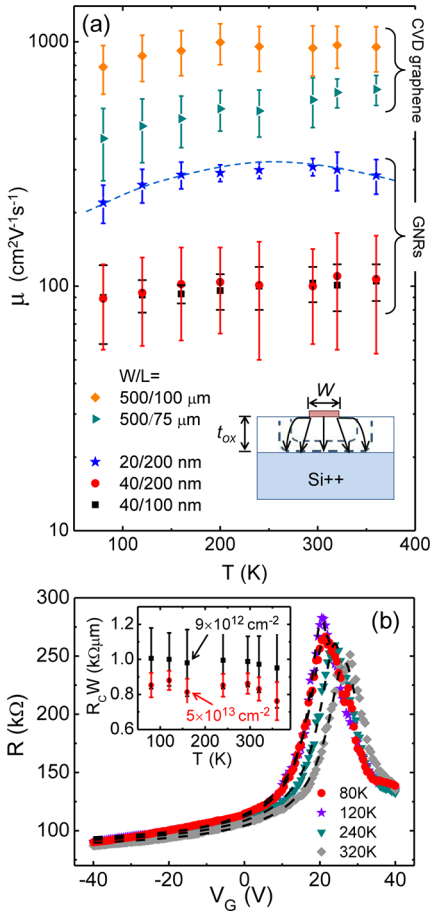

Figure 2. (a) Low-field hole mobility vs temperature for GNRs from CVD graphene (three lower data sets) and large-area CVD graphene devices (two upper sets). All data shown at a charge density $p = 5 \times 10^{12}$ cm^{-2}. The fit[26] to experimental data takes into account thermally generated carriers (n_{th}), puddle charge ($n_{pd} = 1-4 \times 10^{12}$ cm^{-2}), and contact resistance per width ($R_C W = 0.5-1$ kΩ·μm). For GNRs we include the effect of fringing fields (see inset and text). Error bars show upper and lower bounds of μ extraction from the least-squares fit[26] with $R^2 \geq 0.9$ (see Supporting Information, Section C). The dashed blue line is a guide for the eye. (b) Example of fitting GNR data (symbols) for $W \sim 20$ nm device with the model (lines) at $V_{DS} = 50$ mV. The inset shows the contact resistance fit for the same temperatures, at two carrier densities.

nanoscale GNR dimensions being comparable to or smaller than the crystallite size of CVD-grown graphene. Nevertheless, the mobility values of our GNRs from CVD graphene remain lower than those of large samples (Figure 2a), suggesting that transport is still limited by edge roughness scattering, which must be better controlled in future work.

To further understand the transport properties of our GNRs, we undertook temperature-dependent measurements on several samples, as shown in Figure 2. GNR mobility or contact resistance data over a wide temperature range have not been available until now, to our knowledge. Figure 2a displays extracted mobility from three GNRs and two large-area devices (500 × 100 and 500 × 75 μm respectively) from a comparable CVD graphene growth.[32] The large devices show mobilities that are 3−6 times higher than those obtained for GNRs and are likely limited by surface impurities and grain boundary or defect scattering,[33] as the device size is much greater than the crystallite size L_a. On the other hand the GNRs are smaller than L_a; thus their lower mobility is attributed primarily to carrier scattering with edge disorder, although differences in surface impurities between samples cannot be ruled out and could explain the variability noted.

The GNRs with lower mobility (~100 cm^2/V·s) in Figure 2a show virtually no temperature dependence. This is consistent with a transport regime where scattering rates from acoustic phonons, surface impurities, and edge roughness are nearly equal, and their opposite temperature dependence cancels out.[34] However, the ~20-nm-wide GNR with higher mobility shows a slight increase up to room temperature,[30] consistent with a transport regime limited by scattering from surface impurities.[34,35] The mobility then transitions to a weakly phonon-limited regime above room temperature, indicating that this device may be approaching the upper, intrinsic limits of achievable transport in GNRs of this width and edge roughness on SiO_2. Its mobility is also at the upper end of what was achieved in GNRs of this width patterned from exfoliated graphene.[4]

The total resistance (R) and contact resistance (R_C) dependence on temperature for this sample are shown in Figure 2b and its inset. The R_C dependence on temperature and carrier density is given through its dependence on sheet resistance R_S (see Supporting Information, Section C); thus, R_C for such GNRs is almost independent of temperature like the mobility, but it scales approximately as the inverse square root of carrier density, $\propto (n + p)^{-1/2}$ (also see refs 27, 36). The uncertainty in the R_C extraction arises partly from the fitting algorithm (as for mobility) and partly from uncertainty of the GNR width which fans out under the metal contact, taken here between W and $W + 2L_T$ where L_T is the current transfer length into the contact electrode.[36] It is important to note that our model includes thermally generated carriers[26] (n_{th}), which are sometimes neglected but turn out to be crucial in fitting the correct temperature-dependent behavior of the graphene conductance at room temperature and above.

We now turn to the high-field behavior of our GNR interconnects to understand their maximum current-carrying capacity up to electrical breakdown (BD). Figure 3 shows the results of high-field measurements at room temperature for 22 GNRs with widths $W = 15-50$ nm and lengths $L = 100-700$ nm. Figure 3a shows representative current−voltage data obtained from four GNRs in air. Figure 3b suggests that the GNR breakdown power (P_{BD}) scales approximately with the square root of the GNR area, a first indication of the role of heat dissipation from GNRs to the substrate.[2,37] Recasting our measured data as breakdown current density (J_{BD}) versus resistivity (ρ) in Figure 3c, we find scaling similar to both large-area CVD graphene interconnects[14] and GNRs from exfoliated graphene.[38] However, for a given resistivity, the current density of our GNRs from CVD graphene on 90 nm SiO_2 exceeds that of previously measured samples on 300 nm SiO_2.[14,38] To understand these scaling relationships, we apply the model of Liao et al.[2] which includes both heat loss to the substrate and to the contacts:

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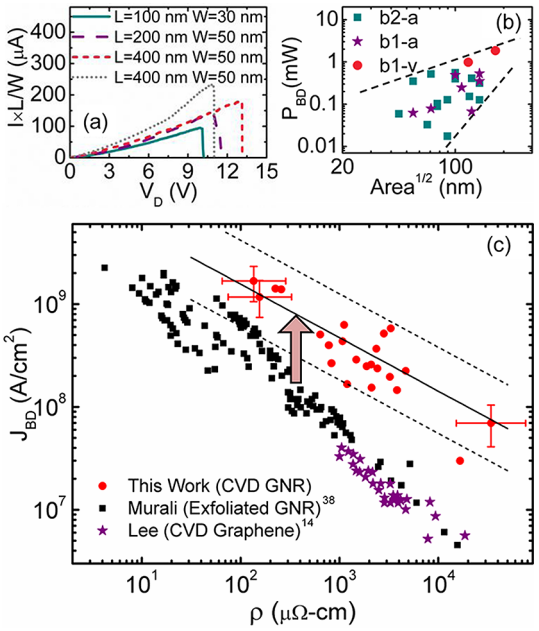

Figure 3. High-field properties of GNRs from CVD graphene. (a) Current−voltage measured up to electrical breakdown. The first three devices in the legend are GNRs capped by AlO_x; the last is uncapped. (b) Maximum power at breakdown increases approximately as square root of the device area (see text). (c) Maximum current density vs resistivity at breakdown for CVD GNRs on 90 nm SiO_2 (this work), GNRs patterned from exfoliated graphene (1 to 5 layers) on 300 nm SiO_2 (Murali et al.[38]), and large-area CVD graphene interconnects (10−20 nm thickness) on 300 nm SiO_2 (Lee et al.[14]). Our devices reach higher J_{BD} in part due to better heat dissipation on the thinner (90 nm) oxide and smaller dimensions of the GNRs. The block arrow symbolizes this size effect. Representative error bars account for the uncertainty in R_C, W, and thickness t_g of our GNRs. The lower dashed line represents the model (see text) assuming GNRs are three-layers thick, have aspect ratio W/L = 60/500 nm, graphene−oxide interface thermal resistance $R_{Cox} \sim 5 \times 10^{-8}$ $m^2 \cdot K \cdot W^{-1}$, and thermal conductivity k_g = 50 $W \cdot m^{-1} \cdot K^{-1}$. The upper dashed line assumes monolayer graphene, W/L = 15/100 nm, $R_{Cox} \sim 5 \times 10^{-9}$ $m^2 \cdot K \cdot W^{-1}$, and k_g = 500 $W \cdot m^{-1} \cdot K^{-1}$. The solid line is obtained with W/L = 35/300 nm, $R_{Cox} \sim 10^{-8}$ $m^2 \cdot K \cdot W^{-1}$, and $k_g \sim 100$ $W \cdot m^{-1} \cdot K^{-1}$, the latter being consistent with previous work on GNRs from unzipped nanotubes.[2]

$$J_{BD} = \left[\frac{g(T_{BD} - T_0)}{\rho t_g W} \times \frac{\cosh\left(\frac{L}{2L_H}\right) + gL_H R_T \sinh\left(\frac{L}{2L_H}\right)}{\cosh\left(\frac{L}{2L_H}\right) + gL_H R_T \sinh\left(\frac{L}{2L_H}\right) - 1} \right]^{1/2} \quad (2)$$

Here, T_{BD} is the breakdown temperature (~600 °C oxidation in air), T_0 is the ambient temperature (22 °C), t_g is the thickness of the GNR, $L_H = (k_g W t_g / g)^{1/2}$ is the thermal healing length,[2,39] k_g the thermal conductivity along the GNR, and R_T is the thermal resistance at the metal contacts.[2] The first fraction in eq 2 above accounts for heat sinking into the substrate, and the second fraction accounts for heat sinking into the contacts. In the limit $L \gg L_H$ the second fraction becomes unity; that is, heat sinking through the substrate dominates for long GNRs. (Complete model information is provided in Section F of the Supporting Information.) The thermal contact resistance per unit length from the GNR to the substrate is calculated as[2,37]

$$g^{-1} = \left\{ \frac{\pi k_{ox}}{\ln[6(t_{ox}/W + 1)]} + \frac{k_{ox}}{t_{ox}} W \right\}^{-1} + \frac{R_{Cox}}{W} + \frac{1}{2k_{Si}} \left(\frac{L}{W_{eff}} \right)^{1/2} \quad (3)$$

where k_{ox} = 1.4 $W \cdot m^{-1} \cdot K^{-1}$ is the thermal conductivity of SiO_2, R_{Cox} is the thermal contact resistance of the graphene−SiO_2 interface,[40−42] $W_{eff} \approx W + 2t_{ox}$ is the effective width of the heated region at the SiO_2/Si interface, and $k_{Si} \sim 100$ $W \cdot m^{-1} \cdot K^{-1}$ is the thermal conductivity of the highly doped Si substrate. We note eq 3 includes fringing heat loss from the narrow GNRs, is mathematically similar to the capacitance expression in eq 1, and was verified against finite-element simulations in ref 2.

The solid line in Figure 3c represents the model above with $W/L \sim 35/300$ nm, $t_g \sim 1.25$ graphene layers (averages for our samples, i.e., ~0.42 nm), t_{ox} = 90 nm, and $R_{Cox} \sim 10^{-8}$ $m^2 \cdot K \cdot W^{-1}$. Additional parameters of our model are the thickness of the metal electrode (t_m) and the thermal conductivities of the GNR, oxide, and metal contacts (k_g, k_{ox}, k_m), as described in Section F of the Supporting Information. The error bars and dashed lines estimate the effect of uncertainties on our extraction and model calculations, respectively. For instance, the variability of the plotted data is partly attributed to the uncertainty in device dimensions, GNR-substrate thermal coupling, thermal conductivity of the devices, contact resistance, and breakdown temperature. (More discussion is also given in the Supporting Information.) With the parameters above, the percentage contribution of the first, second, and third terms in eq 3 are 65% (thermal resistance of SiO_2 including fringing heat loss), 34% (thermal resistance of graphene-SiO_2 interface), and 1% (thermal resistance of silicon substrate). Although the last term can usually be ignored,[2] we include here all terms to highlight that their individual contributions depend strongly on device dimensions and oxide thickness. For carbon nanotubes[39] or extremely narrow GNRs, the graphene−SiO_2 thermal interface will dominate (also see Figure S5b).

We note that the current densities obtained for GNR interconnects in this work are higher (for a given resistivity and width) than those previously achieved and reach ~2 × 10^9 A/cm^2, as shown in Figure 3c. We attribute this to two advances in our understanding and thermal engineering of such small nanostructures. First, the GNRs here are shorter than previous devices,[14,38] being only slightly longer than the thermal healing length ($L_H \sim 0.1$−0.2 μm) and enabling partial cooling through the metal contacts. Second, the GNRs in this work have been deliberately placed on a thinner oxide (~90 nm) versus the ~300 nm used in previous studies.[2,14,38] The thinner oxide reduces the thermal resistance of these devices (see eq 3 and Figure S5) for a given GNR width and is an important factor enabling the higher current densities reached. A similar effect could be achieved by placing GNRs on other thin films with higher thermal conductivity (k_{ox}), or lower GNR-substrate thermal interface resistance (R_{Cox}). Such suggestions are consistent with very recent measurements of larger graphene devices (not GNRs) on nanocrystalline diamond[43] (higher k_{ox}), and on BN substrates (possibly lower R_{Cox} due to smoother graphene-BN interface).[44]

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Before concluding, we also present measurements of our GNRs from CVD-grown graphene performed at the opposite end of the temperature spectrum, down to ~1.7 K, as shown in Figure 4 and Supporting Information, Figure S6. In general, we

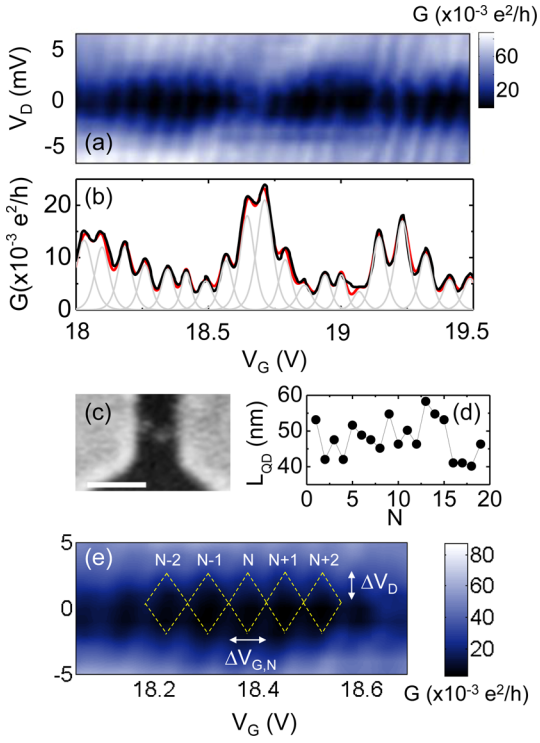

Figure 4. Low-temperature (T = 1.7 K) measurement of a GNR (L/W ~ 52/35 nm) from CVD graphene showing quantum dot (QD) behavior limited by the GNR-metal contacts. (a) Conductance map as a function of V_G and V_D. (b) Conductance profile (black curve) at V_D = 0 V. Gray curves are models including thermal broadening (see text). The red curve is the sum of all gray curves, in good agreement with the measured results. (c) SEM image of the GNR; scale bar = 100 nm. (d) Length of QD estimated from each peak N is similar to the physical length of the GNR, indicating that one QD spans most of the GNR channel. (e) Zoomed conductance map, where $\Delta V_{G,N}$ is the width of the N-th Coulomb diamond. ΔV_D is the drain voltage corresponding to the charging energy of a single electron (see text).

observed quantum-dot (QD), Fabry–Perot (FP), or universal conductance fluctuation (UCF) behavior, depending on the contact resistance (R_C) and quality of the devices (e.g., edges, impurities). Figure 4 displays such measurements for a short GNR (L ~ 52 nm, W ~ 35 nm), indicating QD-like behavior akin to previous observations in single- and bilayer GNRs patterned on exfoliated graphene.[31,45−47]

The black curve in Figure 4b shows the modulation of zero-drain-bias conductance (G) as a function of back-gate V_G. The measurement is performed with a conventional lock-in technique with an excitation voltage V_{ac} = 360 μV, corresponding to an electron temperature T_e ~ 4.2 K (cryostat temperature 1.7 K). An electron overcomes a charging energy to be added into the QD, estimated as $E_C = e\Delta V_D$ ~ 2 meV ($\gg k_B T_e$), where e is the elementary charge (Figure 4e). The Coulomb peaks in Figure 4b can be described[47,48] by $G(V_G) \sim \cosh^{-2}(\eta e(V_G - V_{G,P})/2.5k_BT_e)$ for $\Delta E < k_BT_e < E_C$. Here, $\eta = \Delta V_D/\Delta V_G$ is the "gate factor", $V_{G,P}$ is a Coulomb peak gate voltage, ΔE is the spacing between neighboring single-particle levels in a QD, and ΔV_G is the gate voltage difference between adjacent Coulomb peaks. Gray oscillations in Figure 4b are fitted to the measured black curve using the above equation (T_e = 4.2 K), confirming that the conductance variations originate from Coulomb oscillations in a QD.

We can also estimate the size of the principal QD in Figure 4d,e. The width of the N-th diamond is $\Delta V_{G,N} = e/C_G$ for single electron tunneling, where C_G is the gate capacitance. We obtain ΔV_G = 73 ± 13 mV for the Coulomb peaks in Figure 4b, resulting in C_G = 2.2 ± 0.4 aF. On the other hand, C_G can be also estimated from the device geometry including the effect of fringing fields at the GNR edges, C_{ox} = 1.4 mF/m^2 per unit area from eq 1 with W = 35 nm. This allows us to estimate[47] the size of the QD as C_G/C_{ox} = 1.6 ± 0.27 × 10^3 nm^2, which yields L_{QD} = 49 ± 9 nm (Figure 4d). The estimated length of the QD is near to the physical length of the GNR, indicating that one QD spans most of this particular GNR. The existence of an additional superimposed oscillation with a much larger period in Figure 4a–b could be attributed to a secondary coupled QD approximately ~10 times smaller in size.[45,46]

The observation of QD behavior spanning most of the GNR indicates that some of the shorter GNRs from CVD graphene are relatively defect-free quantum systems, although they do remain limited by their contacts. The presence of defects, grain boundaries, and edge roughness[22,31,45] in longer ribbons, however, can distort the transport along the channel. Among our longer GNRs (L > 100 nm), some have also demonstrated F–P-like or UCF conductance oscillations (Figure S6 in Supporting Information), and others show multiple QDs in series.

In summary, we examined the fabrication, electrical, and thermal behavior of GNR interconnects from CVD-grown graphene, a fundamental step toward their integration into large-scale applications. The GNRs presented here have low-field mobility and Raman signatures comparable to GNRs obtained by other methods. At high-field, small adjustments in thermal engineering such devices allow us to reach some of the highest current densities reported for any graphene interconnects (>10^9 A/cm^2). At low-temperatures, these GNRs display QD- or UCF-like transport behavior, depending on their dimensions and conductance levels. Transport in relatively short GNRs (L < 100 nm) appears to be dominated by contacts rather than by edge roughness, defects, or grain boundaries. This work presents a unified view of low-field to high-field transport in GNRs over a very wide temperature range and serves to identify remaining challenges which include reducing variability, surface impurities, and contact resistance.

■ ASSOCIATED CONTENT

Supporting Information

Details of fabrication process and microscopy of GNRs; additional current–voltage characteristics, effect of GNR width on fringing capacitance, complete details of electrical and thermal models; additional low-temperature data and analysis. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes
The authors declare no competing financial interest.

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Supplementary Information

Transport in Nanoribbon Interconnects Obtained from Graphene Grown by Chemical Vapor Deposition

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A. Graphene nanoribbon (GNR) fabrication from CVD-grown graphene

The graphene growth and GNR device process steps are illustrated in Figure 1a in the main text. Graphene growth by chemical vapor deposition (CVD) is performed by flowing CH_4 and Ar gases at 1000 °C and 500 mTorr chamber pressure, which results primarily in monolayer graphene growth on both sides of the Cu foil[1] (Figure 1a-1). One graphene side is protected with a ~250 nm thick layer of polymethyl methacrylate (PMMA) while the other is removed with a 20 sccm O_2 plasma reactive ion etch (RIE) for 10 seconds (Figure 1a-2). The Cu foil is then etched overnight in aqueous $FeCl_3$ (Figure 1a-3), leaving the graphene supported by the PMMA floating on the surface of the solution. The PMMA + graphene bilayer film is transferred via a glass slide to a HCl bath and then to two separate deionized water baths (Figure 1a-4). Next, the film is transferred to the SiO_2 (90 nm ± 5 nm) on Si substrate (n+ doped, 5 mΩ·cm resistivity) and left overnight to dry (Figure 1a-5). The PMMA is removed using a 1:1 mixture of methylene chloride and methanol, followed by a one hour Ar/H_2 anneal at 400 °C to remove PMMA and other organic residue (Figure 1a-6).

To create GNR devices, we first define large Ti/Au (0.5/40 nm) contacts using optical lithography and electron-beam (e-beam) evaporation (Figures 1a-7&8), followed by smaller finger contacts defining the sub-micron length (L) of the devices (Figure 1b). The width (W) of the GNRs is defined by e-beam lithography, and after the PMMA is developed, 2-4 nm of Al is deposited using e-beam evaporation. The thin Al film oxidizes when the chip is removed from the evaporation chamber[2], and PMMA lift-off leaves behind an AlO_x nanoribbon covering the graphene and stretching between finger electrodes (Figure 1b). Because liftoff of a 2-4 nm evaporated Al film can be surprisingly difficult, one may opt to evaporate a thicker (e.g. 20 nm) metal mask for etching the CVD graphene into ribbons[3]. In that case, the Al mask should be etched before electrical measurement because such thick Al cannot be fully oxidized and will

result in a parallel current path. Finally, a 10 second O_2 plasma etch removes all unprotected graphene, leaving a GNR under the Al etch mask (Figure 1a-7). The etch parameters can be tuned during this step to laterally narrow the protected GNR from the edges, thus achieving GNR widths smaller than the minimum resolution afforded by e-beam lithography[3]. The CVD graphene under the contacts is also protected during the plasma etch, achieving a larger graphene-metal contact area and reduced contact resistance. Because the AlO_x etch mask can double as a seed layer for subsequent top gate deposition[2], we left the AlO_x strip on some devices (batch b1) for the measurements. For comparison, we also removed the AlO_x etch mask using Al etch type A (Transene Company Inc.) on a subset of the devices (batch b2).

B. Microscopy images of graphene nanoribbon (GNR) devices

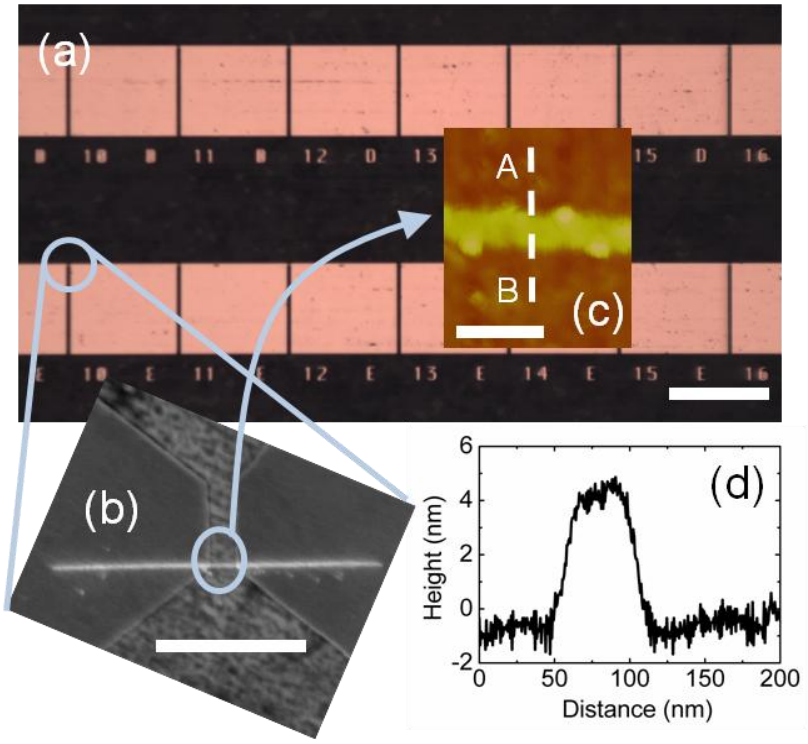

Figure S1 (a) Optical image of large contact pads used to probe individual graphene nanoribbons (GNRs) from CVD-grown graphene. Scale bar is 300 μm. **(b)** Scanning electron microscopy (SEM) image of a device between contacts extended from the large pads. The white strip is the AlOx layer used to define the GNR prior to graphene etch by O_2 plasma. (the graphene layer has not yet been patterned here.) The GNR length is defined by the spacing between contacts and the width by electron beam (e-beam) lithography. Scale bar is 1 μm. **(c)** Atomic force microscopy (AFM) image of GNR covered by AlOx after plasma etching. Scale bar is 100 nm. **(d)** AFM cross section of the GNR covered by ~3 nm AlOx, along the AB line in (c).

C. Current-voltage characteristics of the GNRs and details of the fitting model

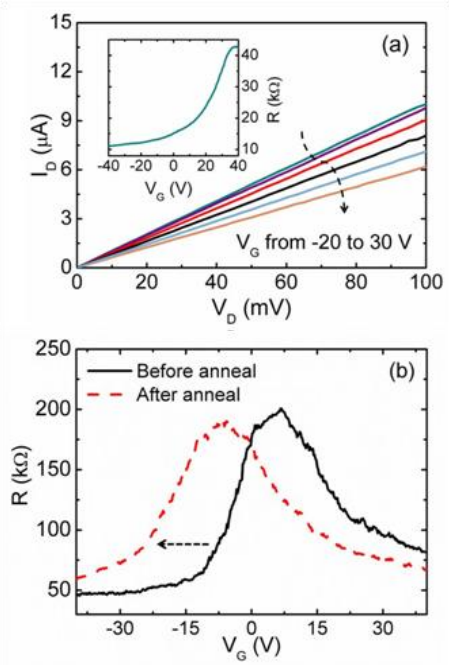

Figure S2 (a) Low field I_D-V_D for a W ~ 50 nm and L ≈ 200 nm CVD GNR at room temperature in vacuum. Inset shows the R-V_G for the same device before annealing. **(b)** Annealing in vacuum at 300 ºC (sometimes followed by a high-current anneal) removes water and other adsorbed species, shifting the Dirac point closer to zero. W/L ≈ 40/400 nm.

We fit the R vs. V_G curves with the following model[4, 5]:

$$R = \frac{L}{W} R_S + 2R_C + R_{lead} \tag{S1}$$

$$R_C = \frac{1}{W} \frac{\rho_C}{L_T} \coth\left(\frac{L_C}{L_T}\right) \tag{S2}$$

where R_C is the graphene-metal contact resistance, $R_S = [q\mu(n+p)]^{-1}$ is the graphene sheet resistance (with mobility μ, electron and hole charge densities n and p), L_C is the length of the contact covering the graphene, and R_{lead} is the resistance of the metal leads. The fitting parameter ρ_C corresponds to the contact resistance between metal and graphene per unit area, while $R_C W$ is the contact resistance per unit width (inset of Figure 2b in the main text). The current transfer length $L_T = (\rho_C/R_S)^{1/2}$ (ref. 6) accounts for current-crowding and represents the distance over which $1/e$ of the current transfers between the graphene and the overlapping metal electrode. This contact resistance model is dependent on V_G through R_S. We note that for our devices L_C ~ 10 μm ≫ L_T ~ 0.5 μm, thus coth (L_C/L_T) ~ 1 in equation S2 above, and the contact resistance simply scales as $R_C \approx \rho_C/(WL_T) = (\rho_C R_S)^{1/2}/W \propto (n + p)^{-1/2}$ as stated in the main text.

In order to compute the sheet resistance R_S, we must estimate the charge density dependence on gate voltage. Thus, we employ the relationship[4]:

$$n, p \approx \frac{1}{2}\left[\pm n_{cv} + \sqrt{n_{cv}^2 + 4n_0^2}\right] \quad \text{(S3)}$$

where lower (upper) signs correspond to electrons (holes), $n_{cv} = C_{ox}(V_0 - V_G)/q$ and C_{ox} is the oxide capacitance including the effect of fringing fields as given in the manuscript eq. 1. The term $n_0 = [(n_{pd}/2)^2 + n_{th}^2]^{1/2}$ results from spatially averaging over the puddle charge (n_{pd}) inhomogeneity and the thermally generated carriers, $n_{th} = (\pi/6)(k_B T/\hbar v_F)^2$ (ref. [4]).

To extract the key independent parameters (ρ_C, n_{pd} and μ) of a device, we perform a least-squares fit by comparing the above models with the experimental data. To simplify this extraction, we first assume a mobility that is independent on carrier density and obtain least-squares fits of n_{pd} and ρ_C. We then use these values to re-fit the model R_S vs. V_G against the experimental data, and obtain the dependence of mobility on carrier density as $\mu = [qR_S(n+p)]^{-1}$.

D. Effect of fringing fields on the capacitance of the nanoribbons

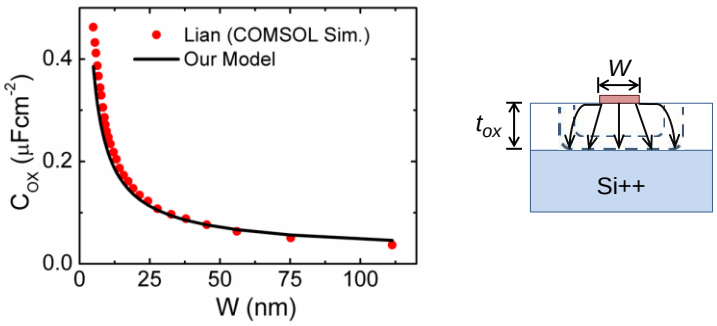

Figure S3 Fringing back-gate capacitance of a GNR as a function of W, here on t_{ox} = 300 nm SiO_2. At large widths the capacitance per unit area saturates to the well known ~ε_{ox}/t_{ox}, at small widths it increases significantly due to fringing field effects (see schematic). Our analytic model presented by equation (1) in the manuscript matches 2D COMSOL simulations by Lian et al.[3] (additional comparison with COMSOL simulations at varying t_{ox} was also done in the supplement of Ref. [7].)

E. High-current breakdown of GNR interconnects from CVD graphene

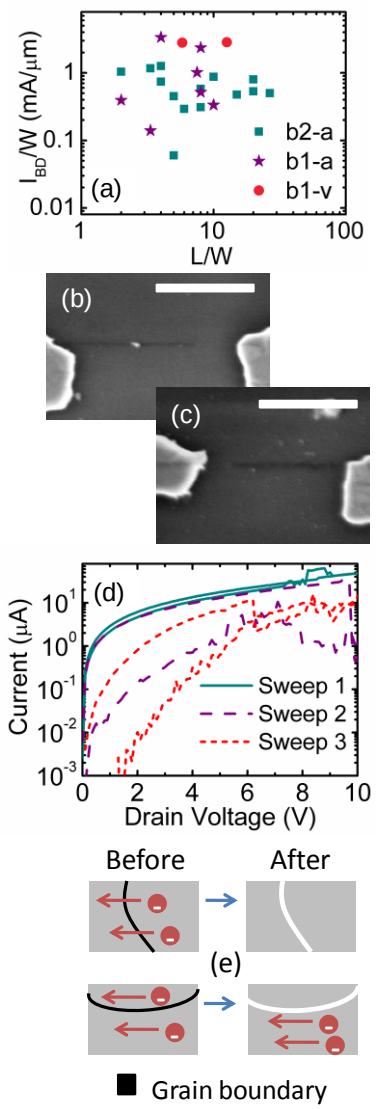

Figure S4 (a) Normalized I_{BD} does not appear to scale with L/W, suggesting it is at least partly limited by GNR edges. Most devices from batch b1 (covered by AlO_x) were broken in air ("b1-a") except two that were broken in vacuum ("b1-v"). **(b) & (c)** SEM images of broken GNRs with width $W \sim 20$ nm. Scale bar is 500 nm. **(d)** A wider GNR (W/L = 50/200 nm) undergoing successive partial breakdowns. Resistance of the GNR increases during the first V_D sweep. During the second sweep the device resistance increases by an order of magnitude but continues to conduct. The GNR completely breaks and stops conducting by the end of the third sweep. As such behavior was only observed in wider GNRs (narrower ones typically break in one step), we hypothesize that the graduate deterioration could occur due to partial breakdown along graphene grains. As graphene grain boundaries locally impede electrical transport, breakdown is more likely to occur at these resistive grains from self-heating **(e)** When a grain boundary runs from one edge of the GNR to the other, physical breaking of the graphene due to self heating will completely impede current flow. However, when the grain boundary starts and ends on the same side of the GNR, breakdown at the boundary will only reduce minimum GNR width, but the GNR still conducts. By contrast, as narrower ($W < 40$ nm) GNRs typically break in one step, they are very likely composed of a single grain.

F. Model used for calculating the breakdown current density

Equation (2) in the manuscript is repeated here,

$$J_{BD} = \left(\frac{g(T_{BD} - T_0)}{\rho\, t_g W} \times \left[\frac{\cosh\left(\frac{L}{2L_H}\right) + gL_H R_T \sinh\left(\frac{L}{2L_H}\right)}{\cosh\left(\frac{L}{2L_H}\right) + gL_H R_T \sinh\left(\frac{L}{2L_H}\right) - 1} \right] \right)^{1/2} \quad \text{(S4)}$$

where $L_H = (k_g W t_g/g)^{1/2} \sim 0.1$ μm is the thermal healing length along the GNR[7], $R_T = [L_{Hm}/(k_m t_m(W + 2L_{Hm})]$ is the thermal resistance at the metal contacts where t_m is the thickness of the contact and k_m is the

thermal conductivity of the contact and $L_{Hm} = (k_m t_{ox} t_m / k_{ox})^{1/2}$ is the thermal healing length of heat spreading into the metal contacts[7]. The heat loss from the GNR to the substrate per unit length (g) is given by equation (3) in the manuscript. The breakdown current expression includes heat loss to the substrate (including fringing effects through g) and heat loss to the metal contacts[7]. The expression reduces to

$$J_{BD} \approx \left[\frac{k_{ox}(T_{BD} - T_0)}{\rho\, t_g t_{ox}} \right]^{1/2} \qquad \text{(S5)}$$

in the limit of large interconnects (L, $W \gg t_{ox}$) on relatively thick oxide layers ($t_{ox} \geq 300$ nm). In this case, the breakdown current density is only a function of the breakdown temperature ($T_{BD} \sim 600$ °C in air, due to graphene oxidation), the properties of the underlying oxide, and J_{BD} scales with resistivity as $\sim\rho^{-1/2}$, as previously found in a study of large-area CVD-graphene interconnects[8].

To analyze our experimental data of GNRs, we used typical values for many of the parameters in the model based on previous studies, both from our group and others. R_{Cox} has a range between 5×10^{-9} and 5×10^{-8} m^2KW^{-1} for typical graphene-oxide interfaces[9-11]. $t_m = 40$ nm is the average thickness of our contacts and $k_m \sim 220$ $Wm^{-1}K^{-1}$ the thermal conductivity of the contacts is calculated by applying the Wiedemann-Franz law to the electrical resistivity measured on separate Ti/Au (0.5/40 nm) test structures. Our data presented in Figure 3c of the main manuscript can be fit with an average L/W = 300/35 nm, R_{Cox} = 10^{-8} Km^2W^{-1} and $k_g \sim 100$ $Wm^{-1}K^{-1}$. Figure S5 shows the dependence of J_{BD} and g^{-1} on W and t_{ox}.

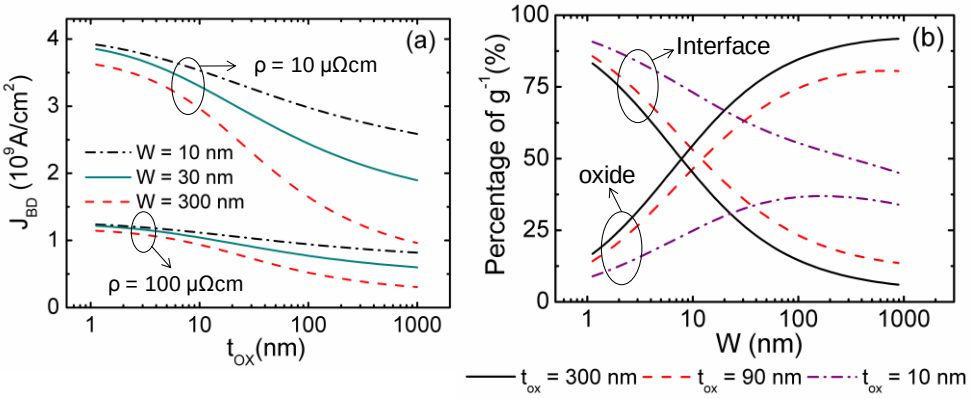

Figure S5 (a) Calculated dependence of maximum current density (J_{BD}) on oxide thickness and GNR width based on eq. (2). Parameters used are $k_{ox}/k_m/k_{Si}/k_g$ = 1.3/220/100/100 $Wm^{-1}K^{-1}$, R_{Cox} = 10^{-8} Km^2W^{-1}, t_m/L= 40/600 nm for several monolayer GNR widths W and resistivity ρ. For maximum current density narrower GNRs benefit more from fringing heat spreading effects[7], but wider ribbons benefit more from a reduction of t_{ox}. Current densities >10^9 A/cm^2 are achievable if GNRs are well heat-sunk and less resistive. **(b)** Percentage of contribution to total thermal resistance (g^{-1}) from the graphene-SiO_2 interface and the SiO_2, as a function of GNR width based on eq. (3). Parameters used are same as above. Thin oxides have low thermal resistance, thus the interface plays a significant role even for wide ribbons. For thicker oxides the interface dominates the thermal resistance at narrow GNR widths, as for carbon nanotubes[12].

G. Temperature dependence of the GNR conductance

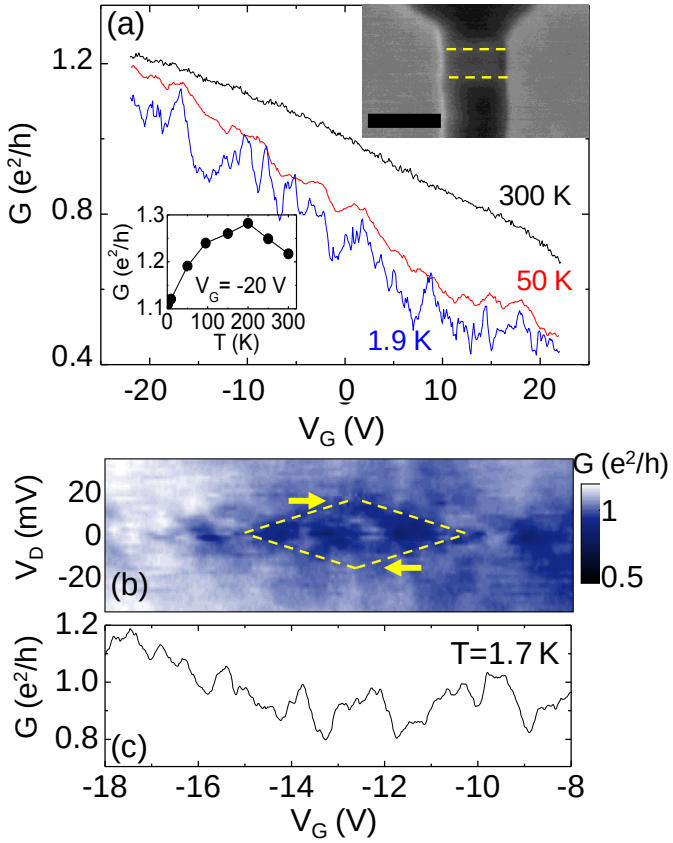

Figure S6 (a) Normalized conductance of a GNR (L/W ~ 160/85 nm) as a function of V_G at various temperatures (V_{SD} = 10 mV). Top inset shows an SEM image of the GNR between the contacts. Scale bar is 200 nm. Bottom inset shows the dependence of G on T at V_G = -20 V. **(b-c)** Conductance map and conductance profile at V_D = 0 V, showing conductance fluctuation. Two arrows indicate $V_c \approx 15$ mV where left- and right-leaning conductance trends meet (see the text).

Figure S6a shows the temperature dependence of the electrical conductance for a GNR (L ~ 160 nm, W ~ 85 nm) with ~26 kΩ resistance at room temperature and zero gate bias. This resistance is comparable to the inverse of the conductance quantum. At T = 50 K, the data shows weak conductance modulation, which evolves to a pronounced repeatable conductance fluctuations at T = 1.9 K. Figure S6b shows the conductance map as a function of V_G and V_D obtained using a lock-in technique with an excitation voltage V_{ac} = 0.35 mV at T = 1.7 K. A diamond-like pattern composed of low and high conductance regions is weakly distinguishable in the color map (surrounded by dashed lines in Figure S6b). Figure S6c shows quasi-periodic conductance fluctuations for zero V_D in the conductance map, which are consistent with Universal Conductance Fluctuations (UCF).[13] When the sample length is not much longer than the phase coherence length, Fabry-Perot (F-P) interference effects are also present while the UCF remains the dominant transport mechanism[14]. Even for devices in which diffusive transport is dominant, a weak F-P interference effect can still be observed as long as a significant portion of electrons experience coherent reflections at the metal contacts.[14, 15]

F-P-like interference has been previously reported in pristine carbon nanotubes,[13] graphene[15] and GNRs with smoother edges prepared by unzipping carbon tubes.[16, 17] In our case, assuming phase coherent transport between the contacts, we can write the round-trip phase shift as[13] $2LeV_c/(\hbar v_F) = 2\pi$. Here V_c

is the drain bias voltage at the crossing point of adjacent left- and right-sloping interference lines[13] and $v_F \sim 10^6$ m/s is the Fermi velocity. We numerically estimate $V_c \approx 13$ mV, in good agreement with the visual estimate of ±15 mV, marked by two arrows on the conductance map. This agreement suggests that the oscillations observed are primarily caused by reflections from the contacts rather than by edge roughness or even grain boundary scattering in such small GNRs from CVD-grown graphene. However, presence of structural defects, charge puddles and impurities (as in our GNRs) would distort F-P oscillations and make a case for simple UCF transport. For example, the broadening of features in Figure S6b and the lack of clear long-range oscillatory behavior can be attributed to effects of disorder and underlying substrate impurities, and lack of atomic-scale abruptness of the graphene-metal contacts.[13, 16-18]

Supplementary References

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