Electrical and Thermoelectric Transport by Variable Range Hopping in Thin Black Phosphorus Devices

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S *Supporting Information*

ABSTRACT: The moderate band gap of black phosphorus (BP) in the range of 0.3−2 eV, along a high mobility of a few hundred cm^2 V^{-1} s^{-1} provides a bridge between the gapless graphene and relatively low-mobility transition metal dichalcogenides. Here, we study the mechanism of electrical and thermoelectric transport in 10−30 nm thick BP devices by measurements of electrical conductance and thermopower (S) with various temperatures (T) and gate-electric fields. The T dependences of S and the sheet conductance ($\sigma_\square$) of the BP devices show behaviors of $T^{1/3}$ and $\exp[-(1/T)^{1/3}]$, respectively, where S reaches ∼0.4 mV/K near room T. This result indicates that two-dimensional (2D) Mott's variable range hopping (VRH) is a dominant mechanism in the thermoelectric and electrical transport in our examined thin BP devices. We consider the origin of the 2D Mott's VRH transport in our BPs as trapped charges at the surface of the underlying SiO_2 based on the analysis with observed multiple quantum dots.

KEYWORDS: black phosphorus, thermopower, electrical conductance, variable range hopping
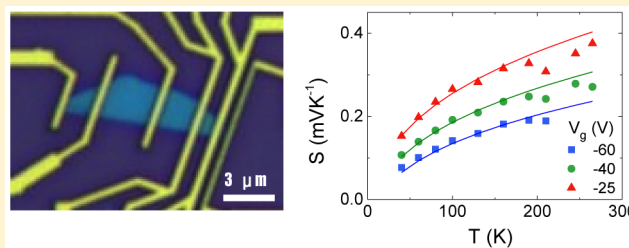
Two-dimensional (2D) electronics based on graphene and transition metal dichalcogenide (TMD) materials have recently provided new possibilities to develop energy-efficient nanoelectronics and optoelectronics due to their low dimensionalites.[1−3] Although optically transparent graphene[4] provides exceptionally high electrical mobility (μ)[5] and thermal conductivity,[6] the gapless feature of graphene limits its application in logic circuits.[7] Layered TMD materials, such as MoS_2 and WSe_2, have exhibited band gaps of 1.3−2.5 eV, depending on their thicknesses, which have been applied in low-dimensional semiconducting electronics.[8−10] However, relatively high Schottky barriers at TMD−metal contacts have limited the development of high-performance electronics.[11,12] Layered black phosphorus (BP) has relatively higher mobility and lower band gap (0.3−2 eV) than those of semiconducting TMD materials.[13−20] Electrical and optical characterizations of few-layer BP flakes have been performed to evaluate their potential future applications in 2D nanoelectronics devices.[21−23] For applications in energy harvesting, BP also has been theoretically suggested for highly efficient thermoelectrics.[24−26] The thermopower or Seebeck coefficient (S) of

BP has been predicted to be in the range of 0.3−2 mV/K depending on the thickness and doping. In experiments, S has been found to be <0.1 mV/K for BP with a thickness of 5−100 nm at temperature (T) of 77−300 K, which was estimated by an indirect method based on photothermoelectric measurements.[27,28] In a traditional electrical measurement setup, it was found that the S of bulk BP reaches 0.3−0.4 mV/K for T = 300−400 K.[29] However, systematic studies of thermopower in thin BP films as a function of T and charge density (i.e., gating dependence) are presently lacking.

In this study, we measured the electrical conductance and S of thin BP flakes with various T and back-gate-electric field (V_g). Near room T, an S ∼ 0.4 mV/K was measured for 10−30 nm thick BP devices. With the T and gate-field-dependent electrical conductance of BP devices including the μ, we confirmed that the $T^{1/3}$ dependence of the S originates from the 2D Mott's variable range hopping (VRH) mechanism, so-called
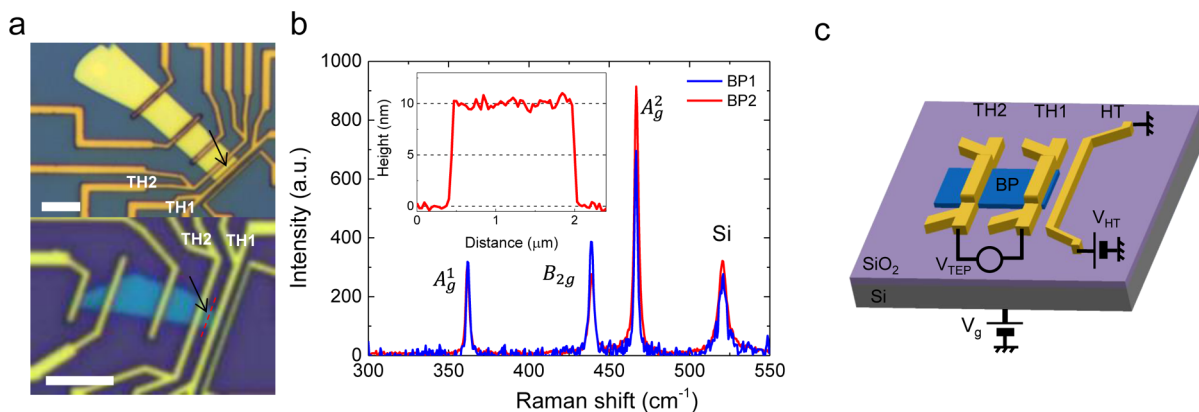
Figure 1. Characterization and measurement setup of BP devices. (a) Optical microscope images of BP1 (upper panel) and BP2 (lower panel) prepared on 300 nm-thick SiO_2/Si substrates. Arrows indicate the regions measured for the thermopower (S). The sample lengths are the same, $L =$ 0.8 μm, and the sample widths are $W = 4.5$ μm (BP1) and 1.5 μm (BP2). Scale bars are 5 μm. (b) Raman spectra of BP1 and BP2, which show the A_g^1, B_{2g} and A_g^2 peaks of BP at ~361.7, ~ 439.2, and ~466.8 cm^{-1}. A peak at 520.4 cm^{-1} originates from the Si substrate. The inset: height profile of BP2 along the dashed line in the lower panel of (a) obtained by AFM. The thicknesses of BP1 and BP2 are 30 and 10 nm, respectively (see Supplementary section 2). (c) Experimental scheme to measure S: the two thermometers TH1 and TH2 are used to measure the temperature gradient along the sample, where the temperature gradient is due to V_{HT} applied to the heater line (HT). The pair of electrodes is also used to measure the thermovoltage (V_{TEP}) and conductance of the sample as a function of gate voltage (V_g).
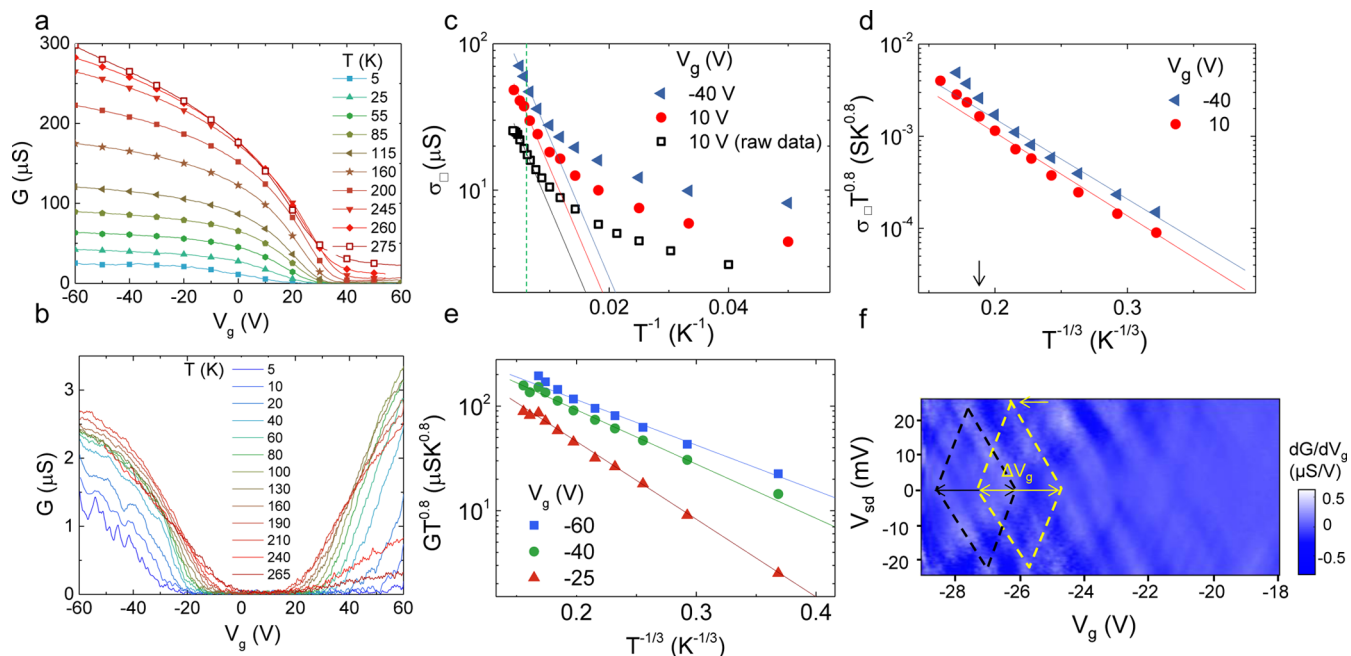
Figure 2. Electrical properties of BP devices. (a,b) Conductance vs gate voltage ($G-V_g$) of BP1 (a) and BP2 (b) for various T, respectively, where G was obtained by the two-probe measurement. c, Electrical sheet conductance ($\sigma_\square$) of BP1 channel without contact resistance as a function of T^{-1} (scattered closed points) for $V_g = -40$ and 10 V. Data depicted by open squares were obtained by the two-probe measurement including contact resistance. Solid lines are fit-results with thermally activated hopping model (eq 1) and a vertical dashed line corresponds to temperature ~150 K, where the data deviate from the thermal activation model with lowering temperature. (d) $\sigma_\square T^{0.8}$ vs $T^{-1/3}$ of BP1 for $V_g = -40$ and 10 V (scattered points) and fit-results (solid lines) with the 2D Mott's VRH model (eq 2), which agrees with experiments for $T < 150$ K, as indicated by the arrow. (e) $GT^{0.8}$ vs $T^{-1/3}$ of BP2 for $V_g = -60$, -40, and -25 V (scattered points) and fit results (solid lines) with the 2D Mott's VRH model, which agrees with experiments for $T < 200$ K. (f) dG/dV_g map as a function of source-drain voltage (V_{sd}) and V_g of BP2 at $T = 5$ K, which shows parallel multiple quantum dots structure. The arrow indicates a representative charging energy of a quantum dot of ~24 meV. Corresponding conductance (G) map is shown in Figure S15b.

hopping thermopower. As the origin of local trap sites for the 2D VRH transport, we suggest trapped charges at the surface of the SiO_2.

BP-based electric devices to measure the S and electrical conductance with various T and V_g are fabricated on 300 nm thick SiO_2/Si substrates using the mechanical exfoliation method and microfabrication process (see Method for details).

As soon as the fabrication process was completed, the devices were coated with a PMMA layer to protect the BP to minimize contamination from moisture absorption under ambient conditions.[30] The PMMA layer on the sample also protects the BP from the formation of large water spots via cohesion of neighboring water spots during the vacuum process at room temperature (see the Supporting Information, section 1).

Figure 1a shows optical microscope images of the completed devices (top, BP1; bottom, BP2). The Raman spectra of the BP1 and BP2 with a 514.5 nm wavelength laser in Figure 1b show four peaks at ~361.7, ~ 439.2, ~ 466.8, and ~520.4 cm^{-1}, which correspond to the optical phonon modes of A_g^1, B_{2g} and A_g^2 of BP and of the Si substrate, respectively.[15] The thickness of BP1 and BP2 were measured by an atomic force microscope (AFM) as ~30 nm and ~10 nm, respectively; the inset of Figure 1b shows the height profile of BP2 after all measurements and removing the PMMA layer (see the Supporting Information, section 2). Two electrodes at the end of the right side of the BP flakes with four extended legs for each electrode, named by TH1 and TH2 in Figure 1a, are used to measure the temperature, electrical conductance, and S of the regions indicated by arrows. Other electrodes with different spacing were prepared to perform the transfer length method and obtain the intrinsic electrical conductivity of the BP channel without contact resistance. Figure 1c shows the configuration used to measure the thermovoltage, V_{TEP}, in response to a temperature gradient along the BP channel due to a heater (HT) biased by V_{HT}, where the highly doped Si substrate serves as a back-gate electrode. After measuring the temperature difference, ΔT_{12}, between TH1 and TH2 at the same V_{HT}, we obtained S from the relation $S = -V_{TEP}/\Delta T$ (see Methods and Supporting Information, sections 3 and 8, for the measurement details, error evaluation, and reliable tests).[31] We note that the widths of the two electrodes are 460 nm and the BP channel lengths are 800 nm for both samples, where we consider that the 460 nm wide electrodes have relatively uniform temperature distribution compared to the 800 nm long BP channel (see Figure S7e in the Supporting Information).

Figure 2a and b show conductance (G) as a function of back-gate voltage (V_g) of BP1 and BP2, respectively, for various T. At $T = 5$ K, the G of BP1 is lowered with positively increasing V_g and becomes zero near $V_g = 20$ V, which indicates that the device shows a p-type character in the examined V_g region. Here, the threshold voltage, V_{th}, is defined as the V_g at which the extrapolated line of a G–V_g curve near a depletion region crosses the zero conductance (see Figure S12a in the Supporting Information). With increasing T, the V_{th} was found to shift to a more positive V_g region. The G–V_g curves at $T = 245$ and 260 K are shifted horizontally, based on an approximately linear dependence of V_{th} with temperature (see the Supporting Information, section 4).[32] The G–V_g curves of BP2 in Figure 2b show both carrier types, e.g., hole (h)- and electron (e)-doped regions for $V_g < -10$ V and $V_g > 20$ V, respectively, at $T = 210$ K. The G–V_g curves in the h-doped region change from a monotonic to a modulated behavior when T is lowered down to ~20 K. The modulated conductance with V_g is a symptom of a formation of quantum dots, which will be discussed later. We note that the G of BP2 is approximately 2 orders of magnitude lower than that of BP devices in previous reports for a similar thickness.[14] The G of BP1 generally decreases with lowering T at a given V_g. Because G was obtained by a two-probe method, the T-dependence of G is affected by both the contact and channel regions. To understand which one plays a dominant role in G, we obtained the intrinsic channel sheet conductance ($\sigma_\square$) based on the transfer length method (see the Supporting Information, section 5). Figure 2c shows a semilog plot of $\sigma_\square$ (without contact resistance) as a function of the inverse of temperature, T^{-1} (triangle and circle scattered points) for two representative V_g of −40 and 10 V, with data indicated by 10 V (raw data)

before subtracting the contact resistance (square scattered points). The solid lines are fit results based on the thermally activated hopping model

$$\sigma_\square \sim \exp[-(E_a/k_B T)] \tag{1}$$

where k_B is the Boltzmann constant and E_a is a barrier energy of a trap site. For all three data sets, E_a was estimated as ~19 meV for $T > 150$ K as indicated by a vertical dashed line in the plot. This indicates that the contribution of the BP channel is dominant for electrical transport when $V_g < 10$ V, rather than the Schottky or tunnel barriers forming at the metal contact regions. This also implies that there are trap sites for charge carriers in the BP channel. On the other hand, G as a function of T^{-1} of BP2 does not show such clear signature related to the thermally activated hopping process as shown in Figure S15.

The transport mechanism in the BP1 channel in Figure 2c appears to deviate from the thermally activated hopping process for $T < 150$ K. For this range, the T-dependent $\sigma_\square$ (solid two lines) in Figure 2d agrees with the 2D VRH model

$$\sigma_\square \sim \sigma_0 T^{-0.8} \exp[-(T_0/T)^{1/3}] \tag{2}$$

with $T_0 = 9 \times 10^3$ K and 8×10^3 K for $V_g = 10$ V and −40 V, respectively. Here, we assumed that electrical transport in the BP channel is mainly attributed to the 2D transport through few surface layers of the BP bottom region interfaced by a SiO$_2$ layer although the number of BP layer is ~60 for the 30 nm thick BP. This assumption can be supported by recent observations of quantum oscillations due to the two-dimensionally confined charge carriers near the bottom surface of the BP even in 10−40 nm thick BP devices with sufficiently high gate-electric field conditions.[33−35,18] For BP2 in Figure 2e, the T-dependent G for $V_g = -25$ V, −40 V and −60 V also show a good agreement with the 2D VRH model up to ~200 K with $T_0 = 5 \times 10^3$ K, 1.7×10^3 K and 10^3 K, respectively, based on eq 2. Because Mott's VRH is related to multiple localized sites along the channel, the sites could act as multiple quantum dots at a low T region.[36] Figure 2f shows the dG/dV_g map of BP2 as a function of the source-drain voltage (V_{sd}) and V_g at $T = 5$ K, which shows multiple parallel diamond-like structure as indicated by solid and dashed lines. This indicates that there are multiple quantum dots through the BP channel. The solid lines present distinctive diamond structures corresponding to a potential well, which has a charging energy of ~24 meV, indicated by an arrow. With $\Delta V_g \sim 2.3$ V, we obtained the size of a quantum dot or trap site as $a \sim 25$ nm, based on the equation $\Delta V_g = e/C_a$, where e is the elementary charge and C_a is the capacitance for an area corresponding to the quantum dot. T_0 is related to the size of the trap site as $T_0 = 13.8/[k_B g(\varepsilon_F) a^2]$,[36] where $g(\varepsilon_F)$ is the density of states at the Fermi level. For MoS$_2$ devices,[36] it has been suggested that the trapped charges at the surface of the SiO$_2$ layer beneath the very thin MoS$_2$ generate local potential wells for charge carriers in the devices. This can also be applied to our BP system when the 2D layer exists at the bottom of BP with proper gate electric fields. If we simply use the $g(\varepsilon_F)$ as generally accepted trapped density at the SiO$_2$ surface, $\sim 4 \times 10^{12}$ cm^{-2}eV^{-1},[37] we get $T_0 \sim 6.6 \times 10^3$ K, which is in a similar range to the fitted results based on 2D Mott's VRH model in Figure 2d,e. The T-dependent conductance of the examined two BP devices reveals that the charge-transport mechanism changes from the thermally activated hopping process to the 2D Mott's VRH process
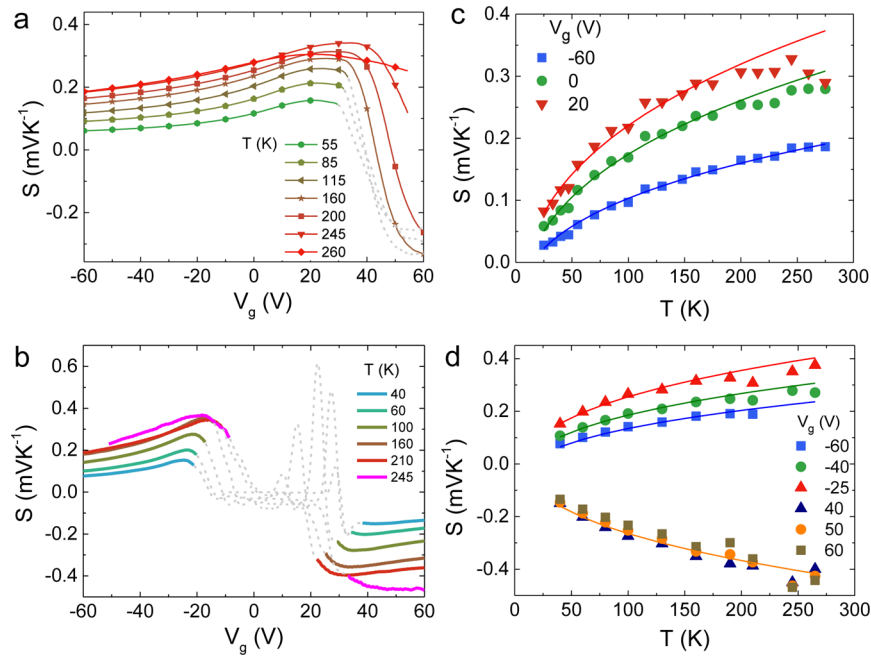
Figure 3. Thermopower of BP devices. (a,b) Thermopower vs gate voltage ($S-V_g$) of BP1 (a) and BP2 (b) for various T, respectively. The gray dashed curves in (a) represent a region that shows a significant resistance fluctuation with varying V_g although the sample resistance, R_s was lower than the input impedance (10 MΩ) of the lock-in system. The gray dashed curves in (b) represent a region that shows R_s larger than the input impedance. The regions could lead to unreliable S; thus, we do not consider S obtained in the regions for further analysis. The max loading error in S for BP2 near R_s = 10 MΩ was <30 μV/K. For the BP1 case, it was <2 μV/K due to its relatively low R_s (see details in section 3 of the SI). (c,d) S of BP1 (c) and BP2 (d) (scattered points) as a function of T for various V_g, respectively. The solid curves in (c) and (d) are fit-results with a relation of $S \propto T^{1/3}$ based on the 2D Mott's VRH model.
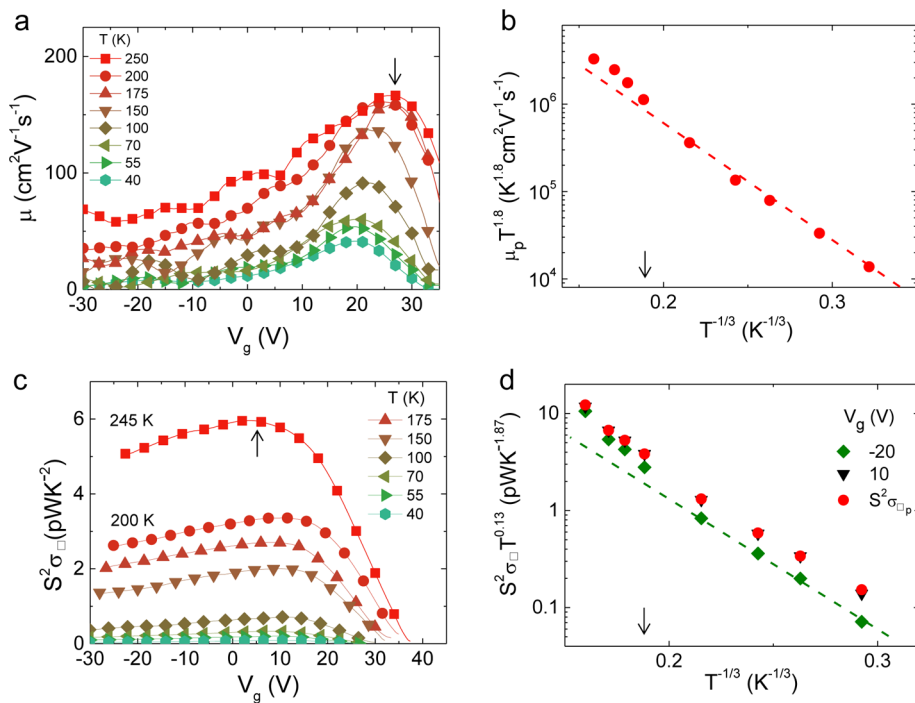
Figure 4. Temperature dependence of mobility and sheet power factor of BP1. (a) Mobility (μ) as a function of V_g with various T, where a peak value of μ_p indicated by an arrow at T = 250 K increases with increasing T and saturates near 170 K. (b) $\mu_p T^{1.8}$ vs $T^{-1/3}$, which shows a deviation from the 2D Mott's VRH model for T > 150 K (indicated by an arrow). (c) $S^2\sigma_\square$ (sheet power factor) as a function of V_g for various temperatures. The arrow indicates a peak value of $S^2\sigma_\square$ at T = 245 K. (d) $S^2\sigma_\square T^{0.13}$ vs $T^{-1/3}$ data (scattered symbols) for various V_g, with the peak value of $S^2\sigma_\square$ ($S^2\sigma_{\square p}$). The dashed line is obtained based on the 2D Mott's VRH model, which also shows a deviation from the 2D Mott's VRH model for T > 150 K (indicated by an arrow).

with lowering temperature. In the 2D Mott's VRH regime, it is expected that the S shows $T^{1/3}$ dependence.

The S for BP1 and BP2 as a function of V_g for various T are shown in Figures 3a and b, respectively. In both cases, the S shows a similar range, that is, $|S| \sim 0.2-0.4$ mV/K for the range of examined V_g, contrary to the large differences in their G values shown in Figure 2a,b. The positive S increases when the hole density decreases and reaches a maximum value near V_{th} for the h-doped region before rapidly decreasing to zero. For the e-doped region, the S of BP2 shows negative values. The gray dashed curves in Figure 3a,b were excluded in the analysis due to reliability issues (see details in section 3 of the SI).[38,39] In both samples, with increasing T, S increases in the beginning and saturates at a high temperature region. Such behavior is plotted in Figures 3c (BP1) and 3d (BP2) for the h-doped region of BP1 and for the h- and e-doped regions of BP2, respectively, at several fixed V_g values. We find that all of them overall show $T^{1/3}$ dependence regardless of V_g values, as indicated by solid curves. It has been known that the $T^{1/3}$ dependence of S is related to Mott's VRH of charge carriers in a 2D material.[40,39] The deviation from the $T^{1/3}$ dependence at V_g = 20 V for $T > 200$ K for BP1 in Figure 3c may be related to thermionic hopping process over the Schottky barriers or through the channel (see the Supporting Information, section 8 (Figure S23)).

Now, we consider the T dependence of the electrical mobility (μ) and sheet power factor ($S^2\sigma_\square$) of BP1, which determines the ability of the device as a field-effect transistor and thermoelectric generator or cooler, respectively. Here, we employed the sheet power factor because the thickness of the effective electrical channel was not quantitatively determined. The low-field mobility is estimated from $\mu = \frac{1}{C_{ox}}\frac{\partial G_{ch}}{\partial V_g}$, where C_{ox} is the gate capacitance per unit area and G_{ch} is the BP channel conductance without contact contribution (see the Supporting Information, section 5). The $\mu-V_g$ curves are plotted in Figure 4a for various T based on the above relation, which shows that $\mu(V_g)$ overall increases with T and saturates near 200 K. If we assume that the carrier density n_c is proportional to T,[41] one expects that $\mu \propto T^{-1.8}e^{-(T_0/T)^{1/3}}$ based on a relation of $\sigma = n_c e \mu$. Figure 4b shows a semilog-scaled plot of $\mu_p T^{1.8}$ vs $T^{-1/3}$ (scattered symbols, where μ_p is the peak value of μ, as indicated by an arrow on the curve at $T = 250$ K in Figure 4a). On the other hand, Figure 4c shows the $S^2\sigma_\square$ as a function of V_g for BP1 with various T, where the $S^2\sigma_\square$ also shows a peak value for each temperature, for example, $S^2\sigma_{\square p} \sim 6$ pWK^{-2} at T = 245 K as indicated by an arrow. On the basis of the 2D Mott's VRH model, one gets a relation of $S^2\sigma_\square \propto T^{-0.13}$exp-$[-(T_0/T)^{-1/3}]$. The semi log-scaled plot of $S^2\sigma_\square T^{0.13}$ vs $T^{-1/3}$ (scattered symbols) for various V_g along with $S^2\sigma_{\square p}$ are shown in Figure 4d. In both cases of mobility and power factor in Figure 4b,d, the T dependences show a deviation from the 2D VRH model for $T > 150$ K (as indicated by arrows in the figures), which is consistent with the T deviated from the Mott's VRH fit result for $\sigma_\square$ and S observed in Figures 2d and 3c, respectively, for the same sample, BP1. Thus, we confirmed that $\sigma_\square$ and S as well as μ and $S^2\sigma_\square$ obtained from our $\sim$30 nm thick BP devices agree with the 2D Mott's VRH model very well. We note that a control experiment in section 7 of the Supporting Information showed that a 15 nm thick BP device (similar thickness to BP2) showed electrical transport behavior based on the 2D VRH model for $T < 150$ K regardless of PMMA capping layer. This indicates that a $\sim$2 nm etching by a

PMMA capping layer during measurements from the top of the BP devices (see Figure S4) plays a minor effect on the mechanism of the electrical and thermoelectric transport. This is also consistent with the charge confinement in few bottom layers of BP devices with a sufficiently high gate-field condition. The arrow in Figure 4c indicates a peak value of $S^2\sigma_\square$ at T = 245 K, ~ 6 pWK^{-2}. This value is comparable to recently reported $S^2\sigma_\square \sim 8$ pWK^{-2} of 15 nm thick MoS$_2$ device at room temperature.[42]

Before concluding, we remark that the S measurement on a relatively thick BP device could not provide the intrinsic S value because a gate-electric field is not applied through all layers due to the screening effect of the bottom layers while the top two probes measure the S. As a result, our measured S could be interpreted as a lower boundary of the intrinsic S. To examine the thickness dependence of S, we fabricated $\sim$8 nm thick sample as shown in Supporting Information, section 9. We found that $S(T)$ of 8−30 nm thick BP devices followed the $T^{1/3}$ dependence in the VRH mechanism, whereas the magnitude of S was relatively suppressed for a 8 nm thick BP device, although more experiments with various sample thicknesses are needed to make a consistent result. We note that although the gating effect is more efficient with decreasing thickness, the thermo-power measurement becomes more sensitive to the charge impurities at the interface. Such an effect on the electrical mobility was already reported in ref 14. Thus, one needs to separate the BP device from the extrinsic charge potentials to observe the intrinsic S values. This could be achieved by putting a BP device on a hexagonal BN layer.

In conclusion, we have demonstrated the electrical and thermoelectric transport in 10−30 nm thick BP devices. The $\sigma_\square$ and S of BP devices show T dependences of $\exp[-(1/T)^{1/3}]$ and $T^{1/3}$, respectively, in terms of 2D Mott's VRH mechanism. We suggest the origin of the local-trap sites for the VRH regime in our BP devices to be trapped charges at the surface of the SiO$_2$ based on the analysis with observed multiple quantum dot structures. This indicates that the thermoelectric transport including the electrical transport in thin BP devices is very sensitive to trapped charges in the substrates; thus, one could manipulate the thermoelectric property of BP devices by substrate engineering, accompanied by the control of the thermal[43−45] and electrical conductivity.[25]

Methods. *Sample Fabrication.* BP single crystals were commercially purchased (smart-elements). Flakes of BP were deposited on 300 nm thick SiO$_2$/Si substrates (Si wafer: p+ doped with a resistivity <0.005 Ω-cm) by the mechanical exfoliation method with Nitto tape under ambient conditions. Because BP is easily contaminated by environmental moisture, double PMMA (poly(methyl methacrylate)) layers (495 K A2/950 K A4) were directly coated onto the substrate after selecting a proper flake by its color with an optical microscope. For the thermoelectric and electrical measurements on the selected BP flake, we deposited Ti(60 nm)/Au(30 nm) metal electrodes onto the selected BP flake by microfabrication processes including electron(e)-beam lithography and e-beam evaporation. As soon as the fabrication process was completed, the devices were again coated with a PMMA layer (495 K A2) to protect the BP to minimize moisture contamination and measured.

Electrical and Thermoelectric Measurements. The four-probe electrical resistances of TH1 and TH2 thermometer electrodes were measured with a lock-in system in a four-terminal scheme to provide temperature information. The

excitation rms voltage, 1 V with a 1 MΩ resister, produces an excitation rms current of 1 μA. The output frequencies for the TH1 and TH2 are 1.333 and 1.533 kHz, respectively. The temperature distribution of the experimental structure was simulated to convince the measurements by using finite element method (see Figure S7 in the Supporting Information).[46,47] The thermovoltage, V_{TEP}, was measured with an excitation voltage for the heater line, V_{HT} = 1 V. The output frequency for V_{HT} was 2.197 Hz. The V_{TEP} of the BP sample was measured at 2 × 2.197 Hz with TH1 and TH2. Here, S was obtained from the equation $S = -V_{TEP}/\Delta T$, where $V_{TEP} = \sqrt{2} V_{lock-in}$ and $V_{lock-in}$ is a value read by the y channel of the lock-in. The BP device conductance was measured with two probes (TH1 and TH2) by a lock-in system with an excitation voltage of 100 μV and an output frequency of 33.77 Hz, and a gate voltage was applied to the highly doped Si substrate.

AFM and Raman Characterization. The Veeco Dimension 3100 was used to obtain the AFM images under tapping mode. The Raman spectra were obtained on a Labram HR system (Horiba Scientific) equipped with a 514.5 nm laser and a × 100 objective lens. The beam exposure time was 10−15 s.

ASSOCIATED CONTENT

Ⓢ Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.5b04957.

> Environmental effect on BP, thickness of BP devices, measurement setup, temperature dependence of threshold voltage and conductance, control experiment for PMMA effect on a BP device, reliable tests of conductance and thermoelectric measurement, transfer length method, thermopower of ∼8 nm thick BP device. (PDF)

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Notes
The authors declare no competing financial interest.

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Supplementary Information

Electrical and thermoelectric transport by variable range hopping in thin black phosphorus devices

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S1. Environmental effect on black phosphorus
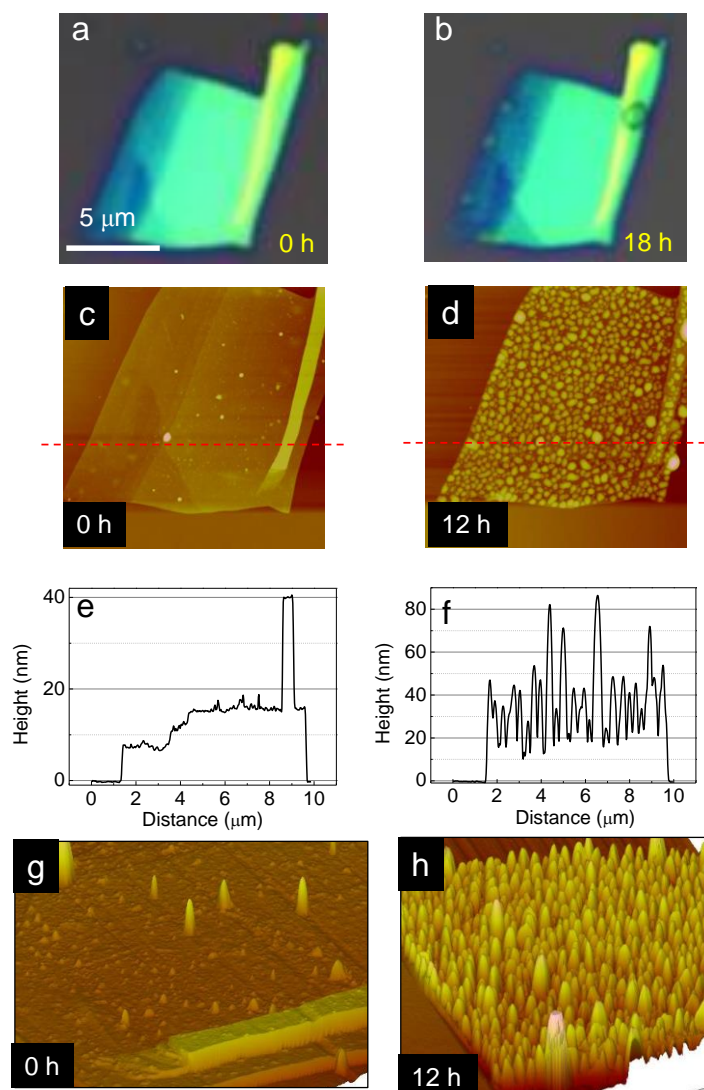
Figure S1. Surface morphology of BP with time under ambient condition. a,b, Optical microscope images of a BP flake for the initial condition and after 18 hours, respectively. **c,d,** AFM images of the same BP for the initial condition and after 12 hours, respectively. **e,f,** Height profiles along the dashed lines on AFM images of **c** and **d**, respectively. **g,h,** Tilted AFM images of the same BP for the initial condition and after 12 hours, respectively. In the initial condition, the ~40 nm thick BP region also shows rougher surface than that of SiO_2 region. Surface roughness of BP increases with time due to absorbed water between the BP and SiO_2 layer.

It has been known that BP flakes on SiO_2/Si substrates absorb moisture from environment under ambient condition, which resulting in degradation of electrical performance, and even reduction of its thickness[S1]. Figure S1 shows the AFM images of BP with time to see such degradation of the sample. Indeed, under ambient condition, the surface roughness increases from ~1 nm to ~17 nm for 18 hours from the initial condition (directly scanned after deposition of the BP flake). The water spots between the BP and SiO_2 layer are nearly homogeneously spread out through entire BP regardless of thickness of BP (10 nm - 40 nm). On the other hand, a BP flake in vacuum shows rather different behavior as shown in Figure S2. The direct AFM image after deposition of a BP flake in Fig. S2c shows a relatively homogeneous distribution through the BP-flake region. The AFM image after 6 hours in vacuum of ~10^{-2} Torr shows a big water spot with a height of ~170 nm and other spots gets rather flattened. In a vacuum process, the water spots start to move and cohere from each other, probably resulting in such a big spot. If its increased weight becomes too large to move by force of a vacuum machine, it would not move. This situation is shown in Figs. S2d and S2e.
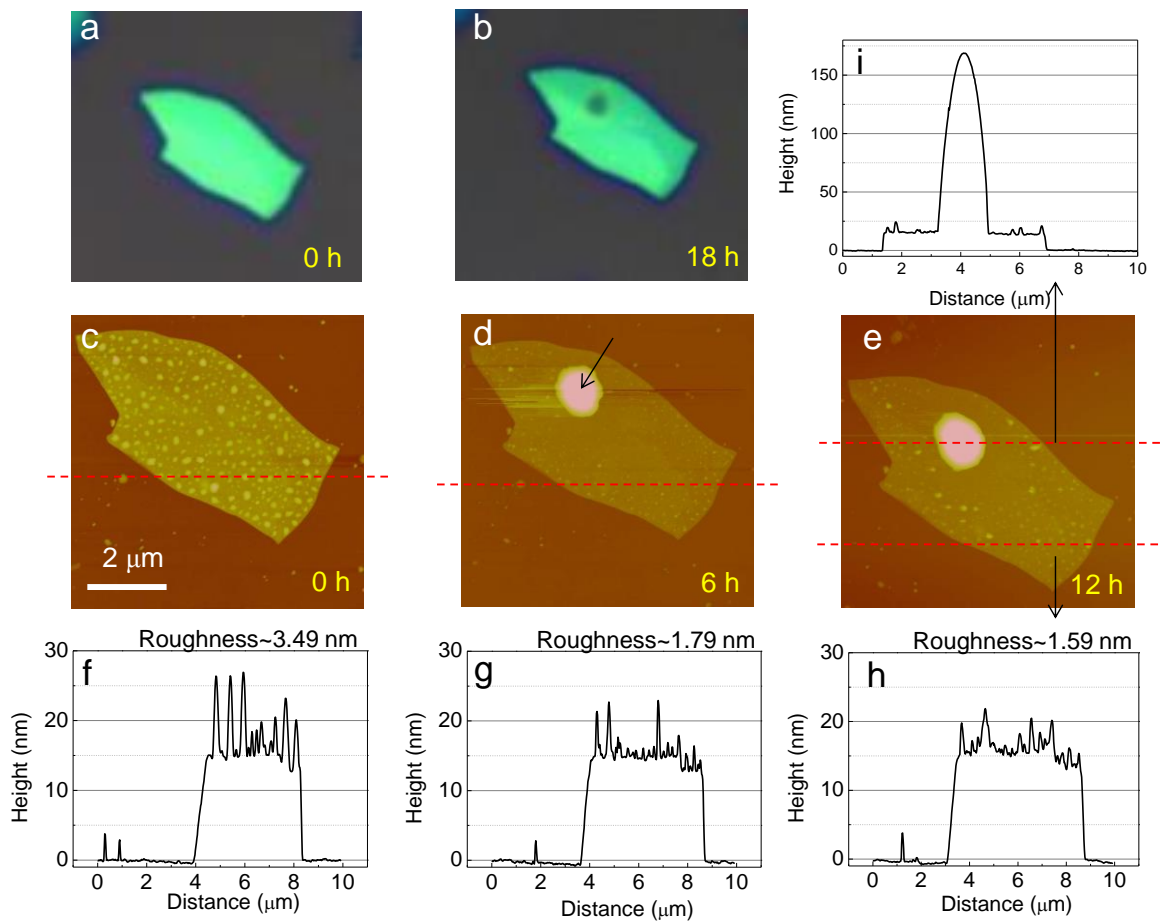
Figure S2. Surface morphology of BP with time under vacuum condition (~10^{-2} Torr). a,b, Optical microscope images of a BP flake for the initial condition and after 18 hours, respectively. **c,d,e,** AFM images of the same BP for the initial condition and after 6 and 12 hours, respectively. **f,g,h,i,** Height profiles along the dashed lines on AFM images of **c**, **d** and **e**, respectively. Surface roughness of BP decreases with time and water is gathered, forming a larger spot as indicated by an arrow in **d**.
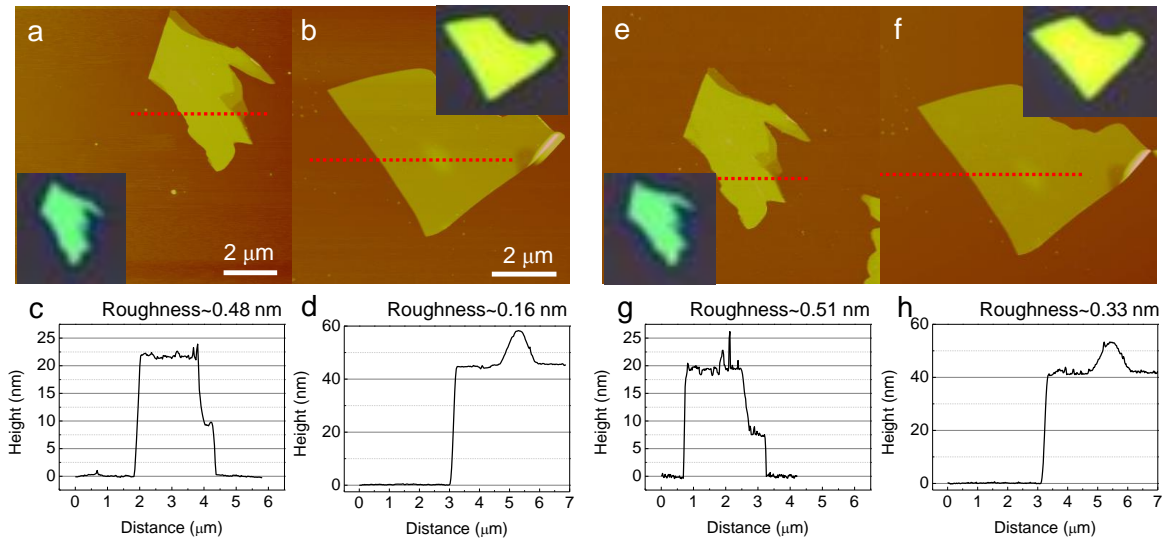
Figure S3. PMMA effect on the surface morphology of BP under vacuum condition ($\sim10^{-2}$ Torr). **a,b** AFM images and optical images (insets) of two BP flakes. **c,d,** Height profiles along the dashed lines on AFM images of **a** and **b**, respectively. **e,f,** AFM images and optical images (insets) of two BP flakes after 24 hours in vacuum environment. Here, the substrate was covered by a PMMA layer in vacuum and the PMMA layer was removed by acetone to get the AFM images. **g,h,** Height profiles along the dashed lines on AFM images of **e** and **f**, respectively.

In experiments, we covered the BP devices with a PMMA layer (495K A2) to prevent such interaction with water during sample preparation process. We found that the PMMA layer etch the BP with time as 2 nm-3 nm per day at room temperature under a vacuum condition as shown in Figure S3. This thickness was also reduced under vacuum condition ($\sim10^{-2}$ Torr). For the electrical measurements, samples have been in He air at $T < 200$ K for ~3 days, usually. As shown in Fig. S4, in such environment we found that the thickness of the BP was changed ~2 nm for 3 days. We note that the already trapped-water spots in the PMMA-coated BP sample were remained at $T = 4.2$ K for 12 hours in vacuum, as shown in Figs. S4e-h although the sizes of the BP bubbles were reduced.
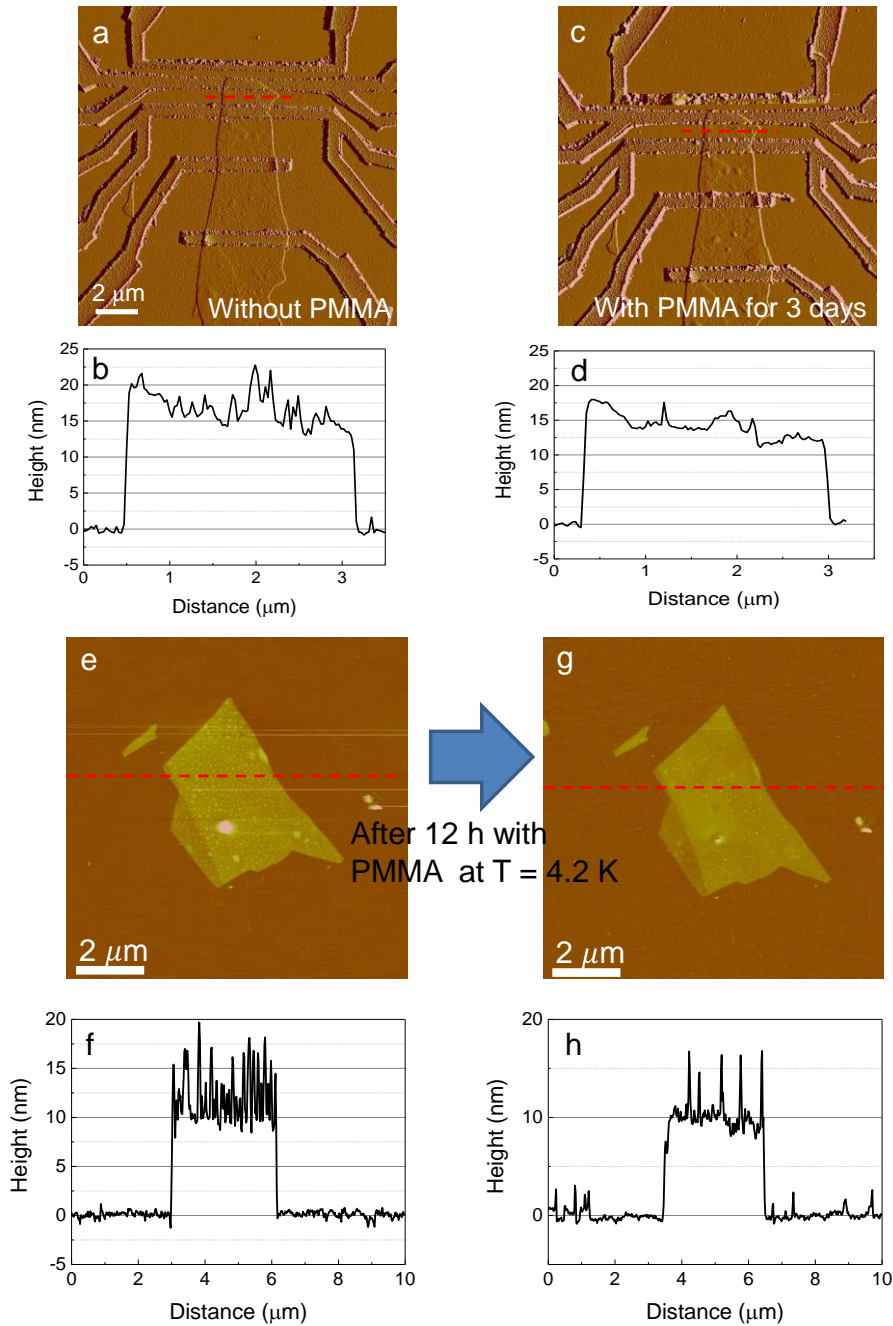
Figure S4. PMMA effect on the surface morphology of a BP device in helium air at *T* < 200 K.
a,b, AFM image and height profile along the dashed line in **a**, respectively, as an initial condition
before PMMA coating. **c,d,** AFM image and height profile along the dashed line in **c**, respectively,
where BP was covered by a PMMA layer for 3 days at *T* < 200 K and the PMMA layer was removed
for the AFM imaging. **e,f,** AFM images and height profile along the red dashed line in **e** in the initial

condition of a BP flake. **g,h,** AFM images and height profile along the red dashed line in **g** after remaining the sample at a low temperature condition of 4.2K for 12 hours.

We found that the PMMA layer on the BP very slowly lowers the height of the BP at a rate of ~ 0.7 nm per day under a He atmosphere (~15 Torr) for $T < 200$ K. Nevertheless, we confirmed that this PMMA etching process does not change the electrical and thermoelectric behavior of ~15 nm-thick BP devices for at least 3 days, which is a typical period for a full measurement (see also sections 7).

S2. Thickness of BP devices
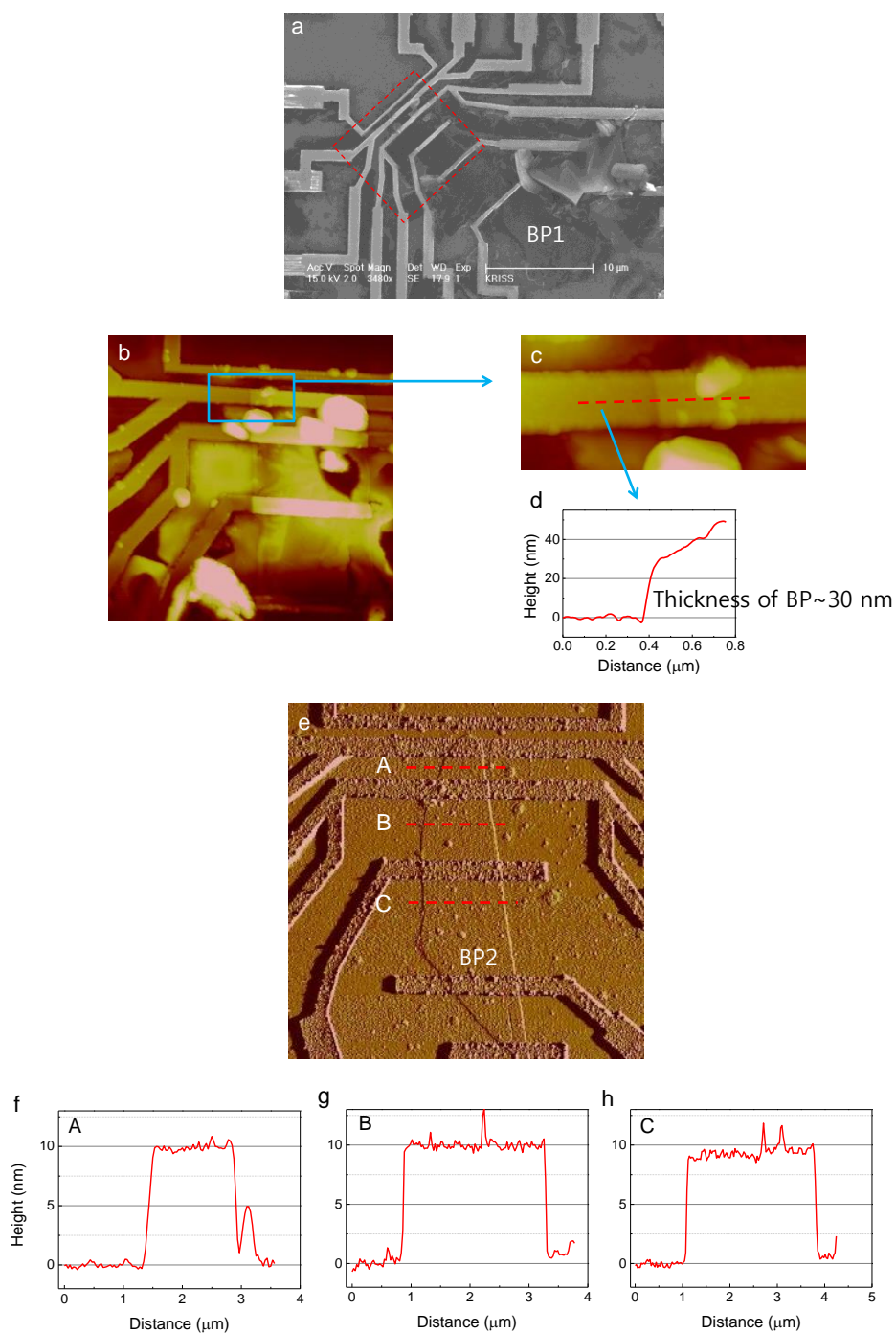
Figure S5, Thickness of BP1 and BP2. a, SEM image of BP1 after measurements and removal of

PMMA by acetone. The sample was damaged by burning of BP channels during measurement, which

leads to failure of cleaning process of PMMA by acetone. Because of this, we took the height profile by AFM of metal electrodes where BP is located beneath metal as shown in **b** and **c**. It provides ~30 nm thickness for BP1 as shown in **d**. **e,** AFM image of BP2. **f,g,h,** Height profiles of BP2 at locations indicated by A, B and C in **e**. Thickness of BP2 is ~10 nm.

S3. Electrical and thermoelectric measurements
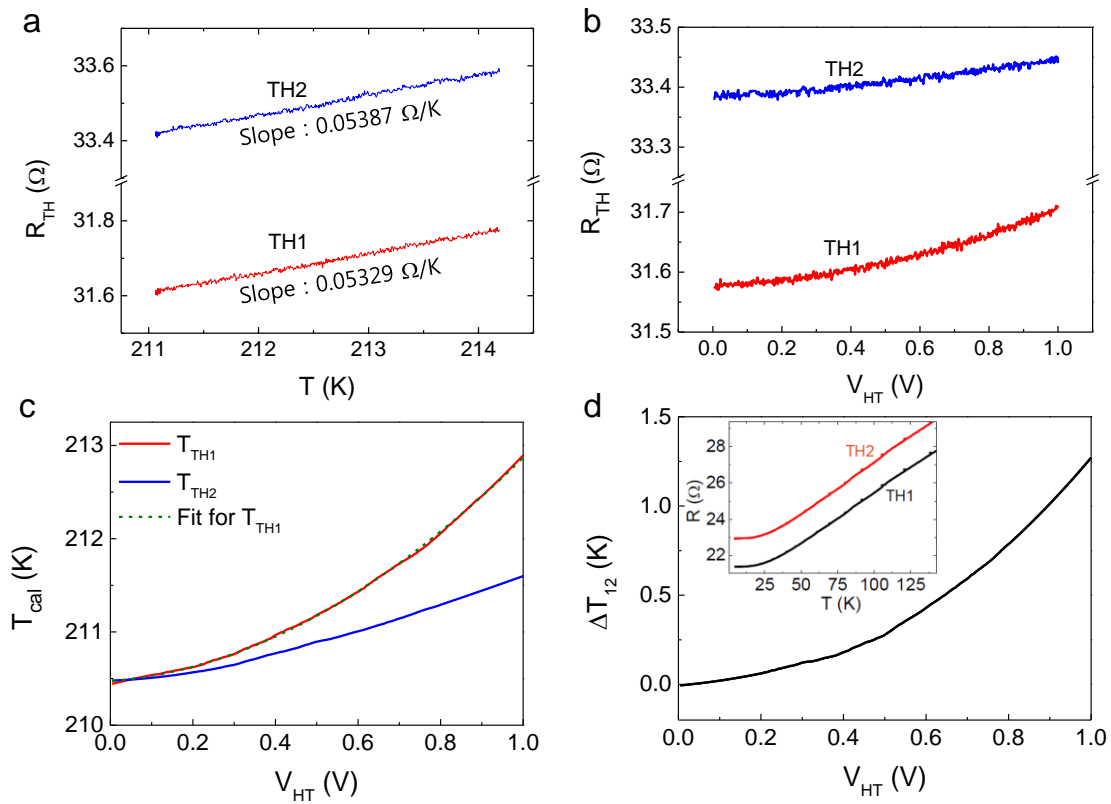
Figure S6. Temperature calibration of BP2 near T = 211 K. a, Resistances vs temperature of TH1 and TH2 in Fig. 1c in the main text. The resistance is measured by four probes with a lock-in system. The excitation rms current is 1 μA. The out-put frequency for the TH1 and TH2 are 1.333 kHz and 1.533 kHz, respectively. **b,** Resistances of TH1 and TH2 vs voltage applied to the heater line. **c,** Calibrated temperature of two thermometer electrodes with increasing V_{HT} are obtained from **a** and **b**.

d, Temperature difference between TH1 and TH2 (ΔT_{12}) as a function of V_{HT}. The inset of **d:** Resistance as a function of temperature (R-T) of TH1 and TH2, where R is saturated for $T < 25$ K and thermometers could not be operated in a proper way in the saturated region. Thus, we only considered S for $T > 25$ K for BP1 and BP2 devices.
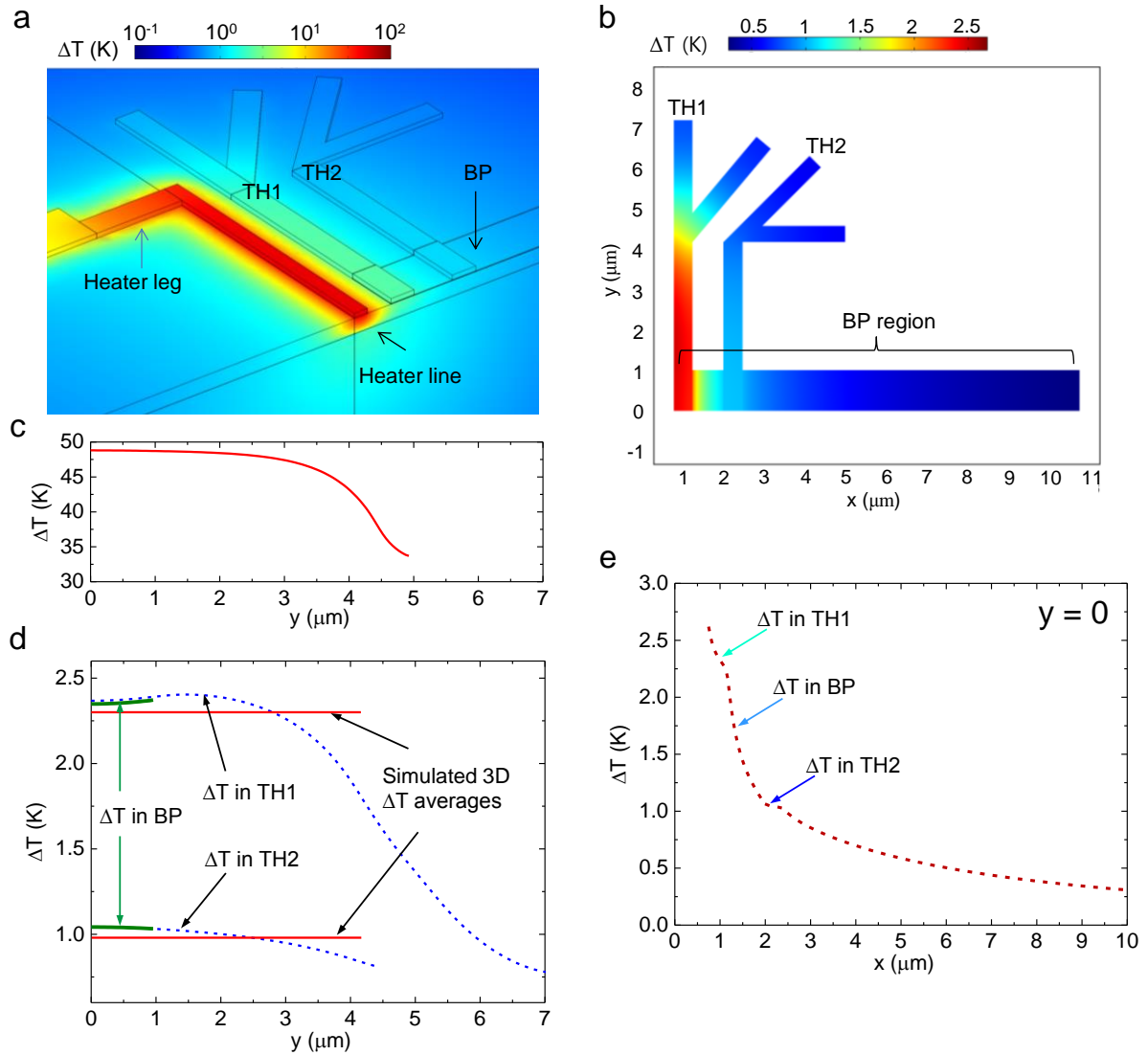

Figure S7. Numerical calculations for the temperature distribution in the thermopower measurement set-up based on the 3D finite element method [S2,S3] at $T = 211$ K for BP2. a,b, Calculated distributions of temperature rise ΔT corresponding to measurements at $V_{HT} = 1$ V in Fig. S6. Table S1 shows the environmental thermal information for the calculation, such as thermal

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conductivity and thermal boundary resistance of components in the device. Here, the BP flake is approximated as a rectangle and its detailed shape have negligible influence on the temperature gradient generated by the heater. **c,** ΔT profile along the heater line (surface of the heater). Temperature gets lower when the position approaches the heater leg. **d,** ΔT profiles along the two thermometer lines (two dashed curves, upper one: TH1, lower one: TH2) follow the non-uniform temperature profile of the heater line. If the heater length was sufficiently longer than those of the two thermometers, one could get more uniform temperature distribution along the thermometer lines. In our case, the voltage probes to read the resistances of the thermometers are located near the heater leg, so we was not able to avoid such non-uniform temperature profiles in the resistance-reading regions of the thermometers. However, we emphasize that our measured temperature represents the 3D average of temperature distribution within the measured segment of the thermometer, and as shown in the calculations, the difference of such averaged thermometer temperatures (red lines) is nearly the same (within ~0.02 K) as the difference of actual temperatures in the BP flake underneath two thermometers (green curves). So, our experimental configuration to perform the thermoelectric measurement is validated by these numerical calculations. **e,** ΔT gradient along x-axis in the middle of BP ($y = 0$, $z = 5$ nm). Temperature drop in the flake is slower at the portion underneath thermometers than that between thermometers, because thermometers help with heat spreading and equilibrium.

k_{Si}	50 Wm^{-1}K^{-1}	$R_{Si/ox}$	1.1×10^{-8} m^{2}KW^{-1}
k_{ox}	1.2 Wm^{-1}K^{-1}	$R_{m/ox}$	1.2×10^{-8} m^{2}KW^{-1}
k_{m}	32 Wm^{-1}K^{-1}	$R_{BP/ox}$	1.2×10^{-8} m^{2}KW^{-1}
k_{BP}	10 Wm^{-1}K^{-1}	$R_{BP/m}$	1.2×10^{-8} m^{2}KW^{-1}

Table S1. Environmental thermal information used to perform the numerical calculations for the temperature distribution in Fig. S7. Here, k_x and R_x are the thermal conductivity and thermal boundary resistance (TBR) of components of the device. The subscripts Si, ox and m mean silicon, SiO$_2$ and metal electrodes, respectively. k_{Si} and k_{ox} are from Refs. [S4] and [S5]. k_m is calculated from the measured electrical resistance according to the Wiedemann-Franz Law. k_{BP} is based on the recent experimental reports[S6]. TBRs are

based on Refs. [S2, S3]. We note k_{BP} and TBR values have very little influence on the thermometer temperatures: ΔT in thermometers only changes <5% if these values change by a factor of 5.
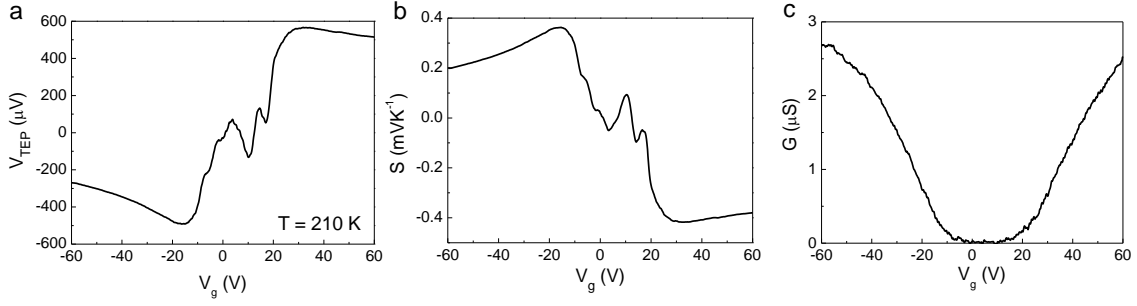

Figure S8. V_{TEP}, S and conductance of BP2 at $T = 210$ K. a,b, Thermovoltage vs. back-gate voltage (V_{TEP}-V_g) and corresponding thermopower vs. back-gate voltage (S-V_g), respectively. V_{TEP} is measured under $V_{HT} = 1$ V (an excitation voltage of lock-in applied to HT). The output frequency for V_{HT} is 2.197 Hz. V_{TEP} of the BP sample is measured at 2×2.197 Hz by the y-channel of the lock-in with TH1 and TH2. The frequency of the modulating temperature due to the V_{HT} is two times higher than the frequency of V_{HT} because the increasing temperature is proportional to the square of V_{HT}. It also leads a change of the phase of the signal as much as -90°, thus V_{TEP} should be read at the y-channel of the lock-in. In addition, the displayed value, $V_{lock-in}$ in the lock-in is an rms value of V_{TEP}, so that V_{TEP} becomes $\sqrt{2}V_{lock-in}$. Finally, S is obtained by a relation of $S = -V_{TEP}/\Delta T$., where ΔT is the temperature difference of the two thermometers with $V_{HT} = 1$ V, as shown in Fig. S6. **c,** Conductance vs. back-gate voltage (G-V_g), which is measured with two probes (TH1 and TH2) by a lock-in system with an excitation voltage, 100 µV and out-put frequency, 33.77 Hz.
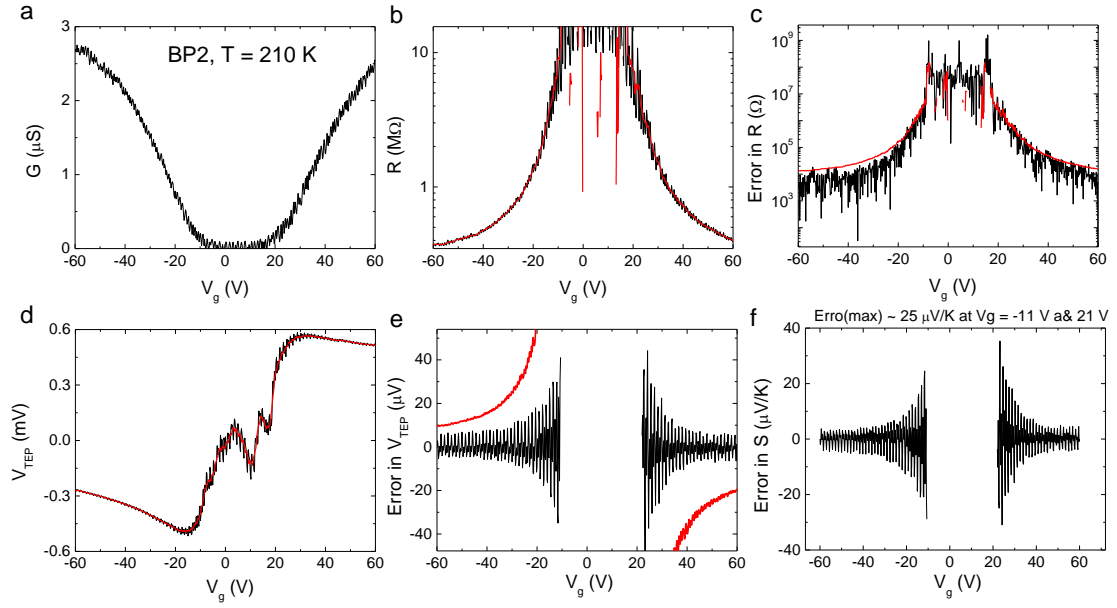
Figure S9. Error evaluation in the sample resistance and *S* in BP2 at *T* = 210 K. a,b, *G*-*V_g* and *R*-*V_g* curves (black curves) before the average treatment. A red curve in **b** is an average curve of *R*-*V_g* curve with neighbor 8 points in *V_g*. **c,** Error in *R*-*V_g* curve. Black one (experimental error) was obtained after subtracting the red curve from the black curve in **b** and taking absolute values of the differences. The red curve was obtained based on a relation of the loading error due to the input resistance. The loading error is given by $R_s \times [R_s/(R_s+R_i)]$, where R_s and R_i are the sample resistance and the lock-in input resistance. The lock-in (SR830) which has been used to measure the resistance and thermovoltage of the devices has R_i = 10 MΩ. R_s was obtained from the average curve (the red curve in **b**). The measured resistance errors (black curve) were consistent with the estimated loading error (red curve). **d,** V_{TEP}-*V_g* curve. Black and red ones: raw data and average curve with neighbor 8 points in *V_g*. **e,** Error in V_{TEP}-*V_g* curve. Black one (experimental error) was obtained after subtracting the red curve from the black curve in **d**. The red curve was obtained by $V_{TEP} \times [R_s/(R_s+R_i)]$, where V_{TEP} was obtained from the average curve (a red curve in **d**). It was deviated from the experimental error with factor of ~2.5. **f,** Experimental error in *S* as a function of *V_g*. The maximum error was ~25 μV/K at V_g = -11 V and 21 V. The V_g values which give the maximum error correspond to V_g which the sample resistance reaches to 10 MΩ (R_i of lock-in). Here, the criterion for the maximum error

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followed Ref. [S7]. In the report, it was turned out that when the 2-terminal resistance of the device channel is on the same order as the input impedance of the measurement instrument, the measured values of S become unreliable. For the BP1 case, the loading error in S was in ~2 µV/K through all examined temperature ranges because R_s of BP1 was much smaller, compared to the R_i.
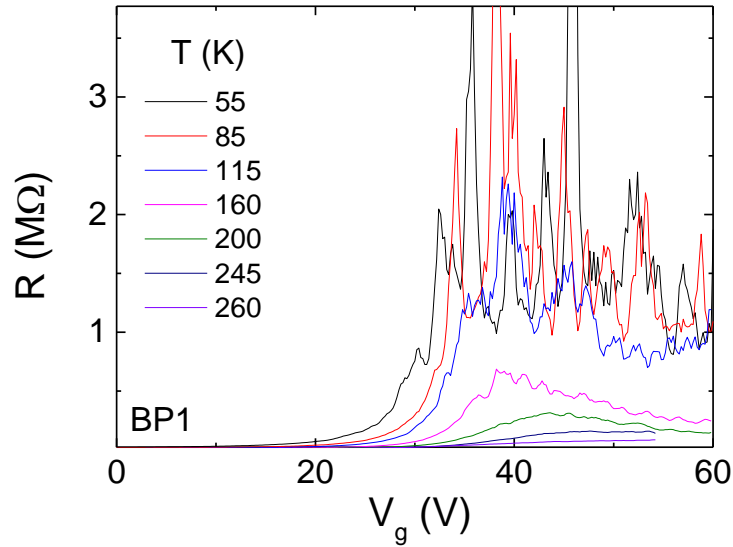

Figure S10. R-V_g curves of BP1 for various temperatures. For $T < 115$ K, although the sample resistance is lower than 10 MΩ for all examined V_g and there are significant resistance fluctuations for $V_g > 30$ V. In Fig. 3a, thus, we did not consider S for the regions at $T < 115$ K.
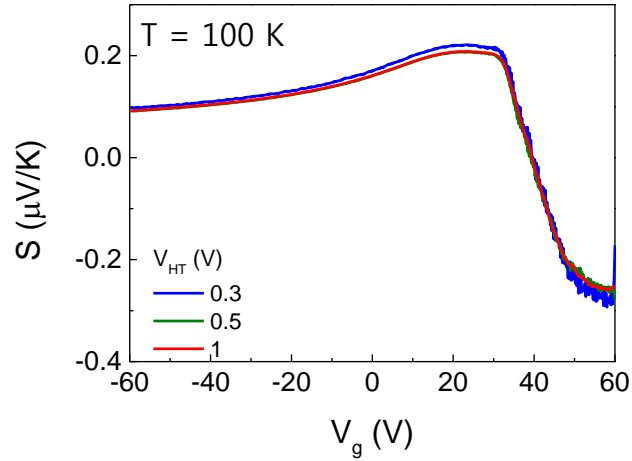
Figure S11. Effect of V_{HT} on S of BP1. Thermoelectric power vs. back-gate voltage (S-V_g) at $T = 100$ K for various V_{HT}, which does not show significant difference while V_{HT} changes from 0.3 V to 1 V, which indicates that our experimental scheme is very reproducible up to $V_{HT} = 1$ V. Based on this, we have used $V_{HT} = 1$ V to increase the ratio of signal to noise.

## S4. Temperature dependence of threshold voltage, V_{th}

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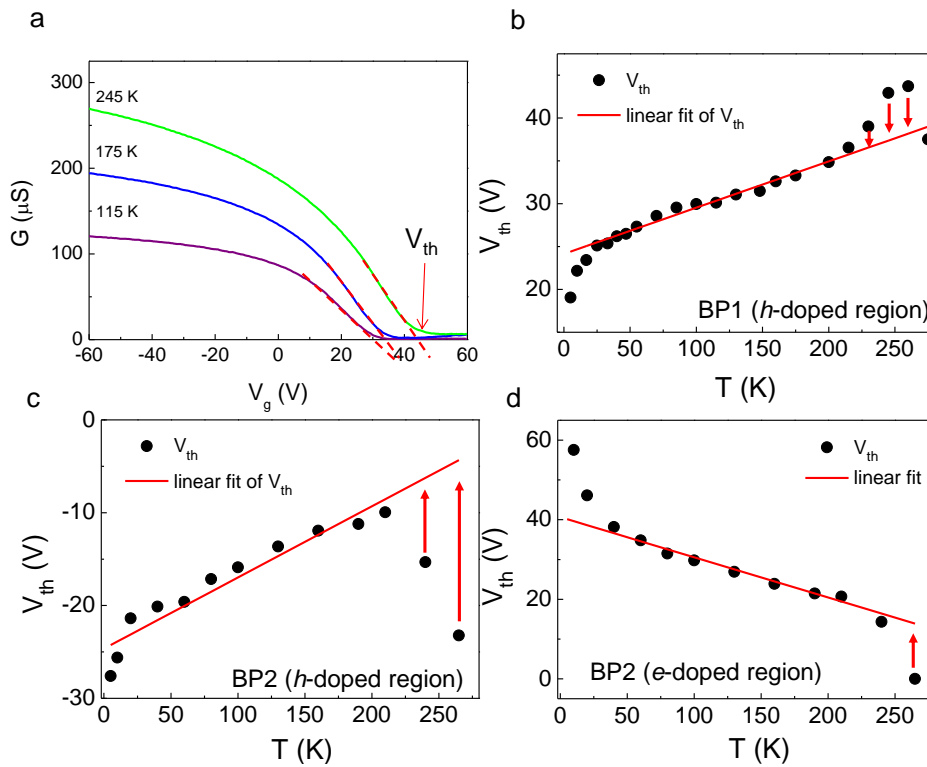
Figure S12. Effect of temperature on V_{th} for BP. a, Raw G-V_g curves for several temperatures. The threshold voltage, V_{th} is a V_g where an extrapolated line of G-V_g curve near the depletion region crosses the *x*-axis (see dashed line on each G-V_g curve). **b,** V_{th} as a function of temperature of BP1 (hole-doped region). **c,d,** V_{th} as a function of temperature of BP2 for *h*- and *e*-doped regions, respectively. It has been known that V_{th} shows a linear function of temperature, but, several data points at high temperature regions show deviation from best-fitted linear lines. To make a consistency, those were vertically shifted into the lines as shown by arrows.

S5. Transfer length method and mobility
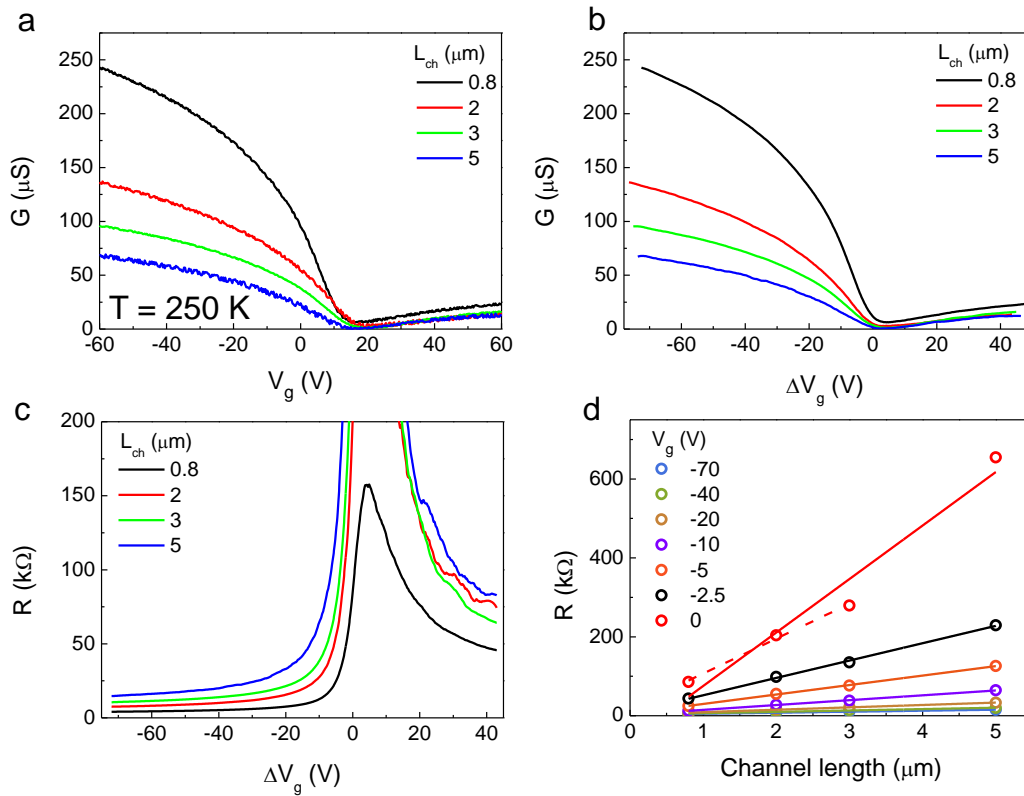
Figure S13. Transfer length method (TLM) for BP1. a, Conductance vs. back-gate voltage (G-V_g) for various channel lengths (L_{ch}) at T = 250 K. **b,** G-ΔV_g curves obtained from **a**, where $\Delta V_g = V_g$-V_{th}

and the original curves were averaged. **c,** Resistance vs. back-gate voltage (R-ΔV_g) for various channel lengths, which are obtained from **b**. **d,** Resistance vs. channel length (R-L_{ch}) at various V_g, obtained from **c**, where the intersection of the extrapolated line from data and y-axis gives the contact resistance ($2R_c$) and the slope of the data corresponds to the channel resistance per L_{ch} without contact resistance.
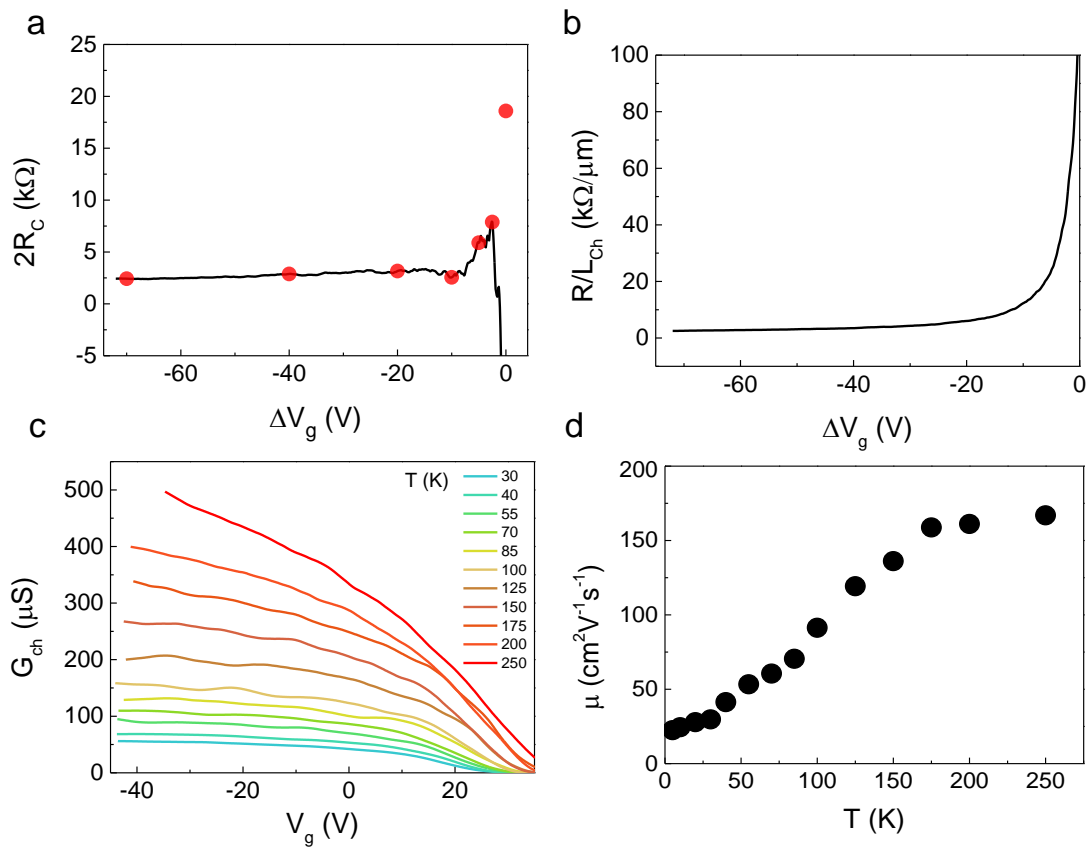

Figure S14. Contact, channel resistances, channel conductance and mobility. a,b, Contact ($2R_c$), channel resistances divided by channel length (R/L_{ch}) as a function of ΔV_g at $T = 250$ K, respectively. $2R_c$ are obtained from Fig. S13d, where a solid curve and scattered points were obtained by fit with 4 points (solid lines) and 3 points (a dashed line). **c,** Channel conductance (G_{ch}) as a function of V_g for

L_{ch} = 0.8 µm channel, where V_{th} of G_{ch}-V_g curve for each temperature was again aligned to match that in Fig. S12b. **d,** Mobility of BP1 as a function of temperature.

In a two-probe measurement, a measured resistance includes the contact resistance. The transfer length method with multiple contacts with various channel lengths as shown in Fig. 1a in the main text provides a chance to extract the contact resistance and channel resistivity without contact resistance as shown in Figures S13 and S14. Slopes of R-L_{ch} curves in Fig. S13d correspond to the resistance per channel length, R/L_{ch} without contact resistance (see Fig. S14b). The inverse of R/L_{ch} is GL_{ch}. Now, we get the channel conductance G_{ch} = GL_{ch}/0.8 µm of L_{ch} = 0.8 µm device for various temperatures in Figure S14c. We also define the mobility by $\mu = \frac{1}{C_{ox}}\frac{\partial G_{ch}}{\partial V_g}$ and Fig. S14d shows a temperature dependence of μ of BP1.

## S6. Temperature dependence of *G* and multiple quantum dot in BP2
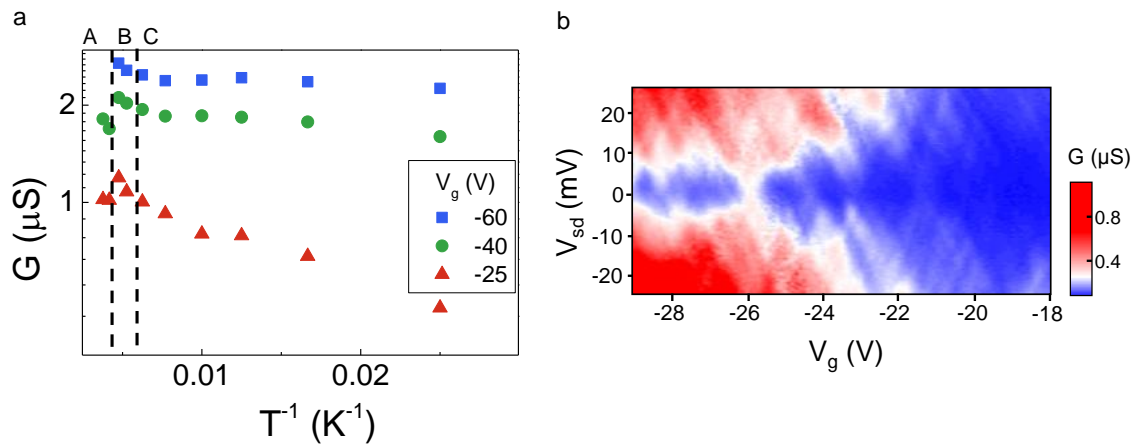
Figure S15. *G* **vs** *T*⁻¹ **curve of BP2 for various** V_g **conditions and multiple quantum dot in BP2. a,** In a temperature region of A (*T* > 220 K), it shows a metallic behavior. Only, a small region of B (170 K < *T* < 220 K) could be related to a thermally activated hopping region, compared to the C region (*T*

< 170 K) which shows a definitely different slope from few points in B. For the e-doped region of V_g > 40 V, G also shows a metallic behavior for T > 160 K (Fig. 2b in the main text). **b,** Conductance (G) map as a function of V_{sd} and V_g of BP2 at T = 5 K. Many conductance peak lines as indicated by white color form multiple diamond structures which are overlapped from each other and indicates a formation of parallel multiple quantum dots in the BP channel[S8].

## S7. Control experiment for PMMA effect on a BP device
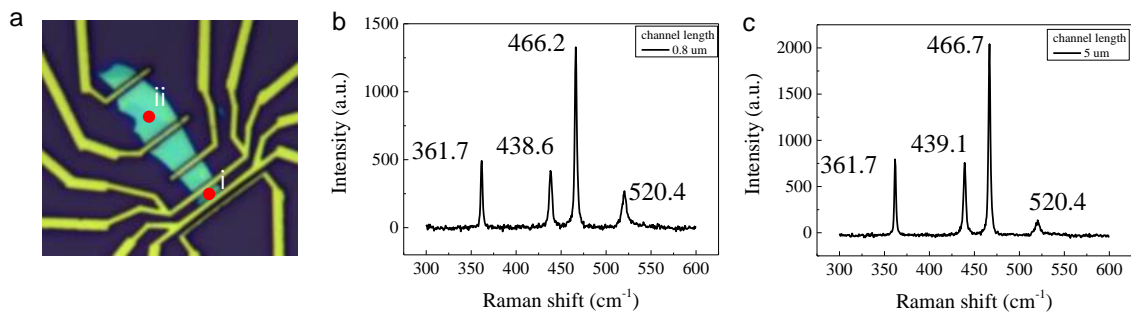
Figure S16. BP3 for control experiment. a, Optical image of BP3. **b,c,** Raman spectra at locations indicated by i and ii in **a**, respectively.
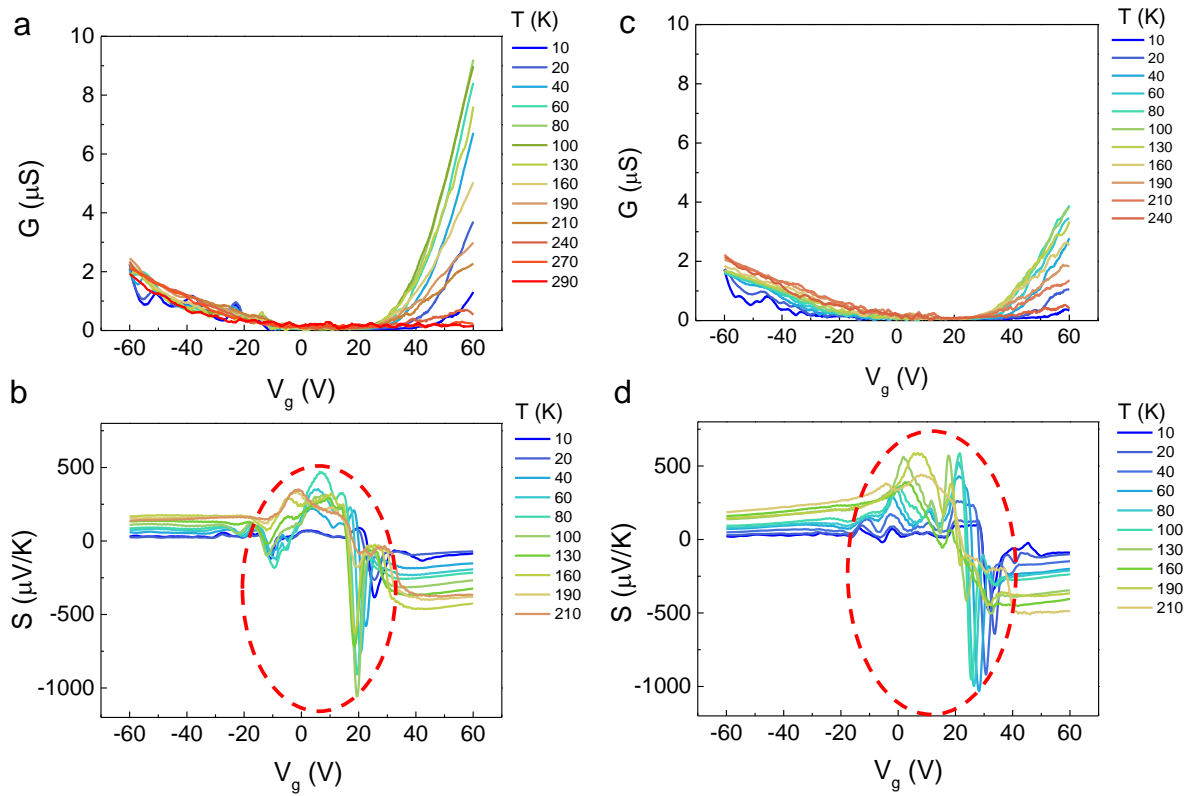
Figure S17. Electrical conductance and thermopower of BP3 (i region in Fig. S16a). a,b, conductance (G) and thermopower (S) as a function of V_g for various temperatures for an initial condition before coating a PMMA layer. **c,d,** G and S as a function of V_g for various temperatures after 3 days with coating a PMMA layer at $T < 200$ K. The anomalous S in the depletion region is shown in both cases of **b** and **d**, as indicated by enclosed dashed curves, which could be artifact due to the high resistance in the depletion region. S in **b** and **d** show similar values.
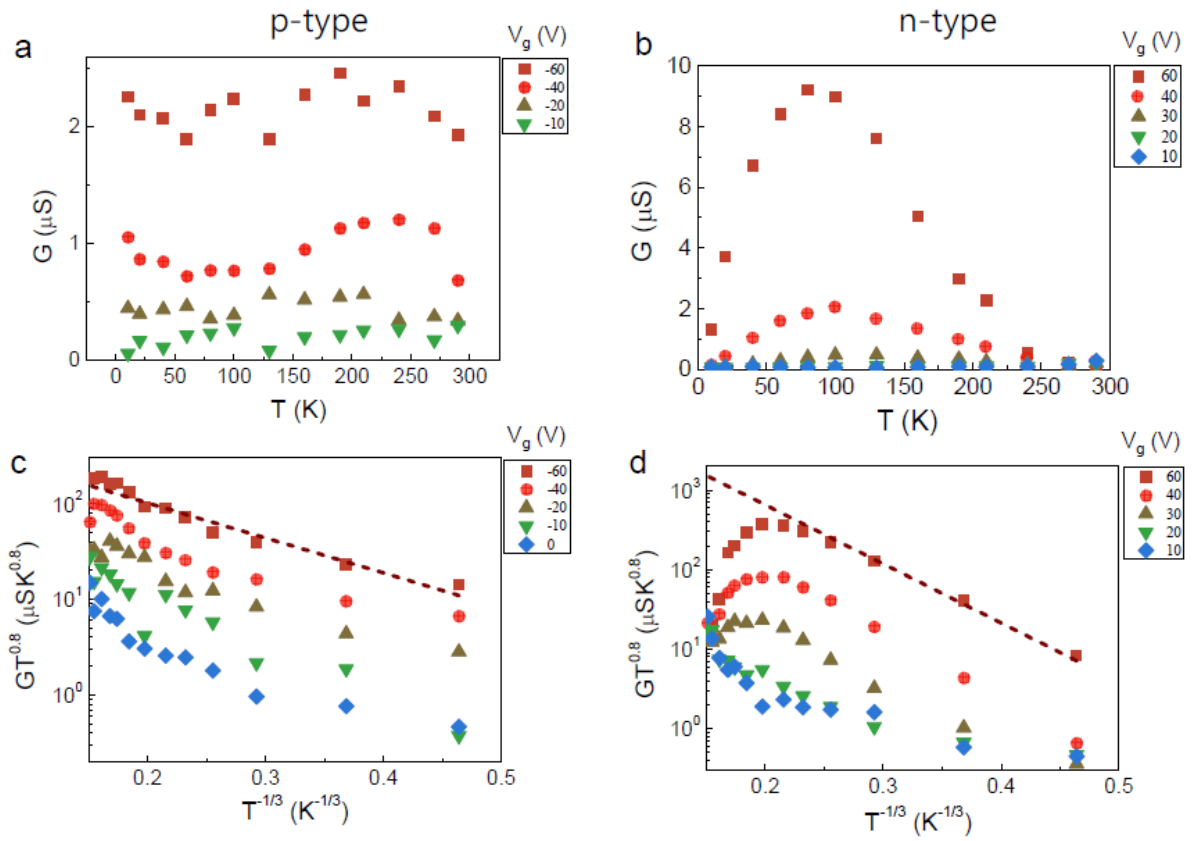
Figure S18. 2D Mott's VRH models for electrical transport in BP3 before coating a PMMA layer. a,b, conductance (G) as a function of temperature (T) for *p*- and *n*-doped regions, respectively. G in **b** decreases with increasing temperature $T > 100$ K, which could be related to the metallic phase. **c,d,** 2D Mott's VRH model : $GT^{0.8}$ vs. $T^{1/3}$ for *p*- and *n*-doped regions, respectively. Dashed lines at V_g = -60 V and 60 V in **c** and **d** were obtained with a relation of $G = BT^{-0.8}\exp(T_0/T)^{-1/3}$ with T_0 = 6×10² K and 5×10³ K, respectively, which are in a similar range with those estimated from BP1 and BP2 in the main text.
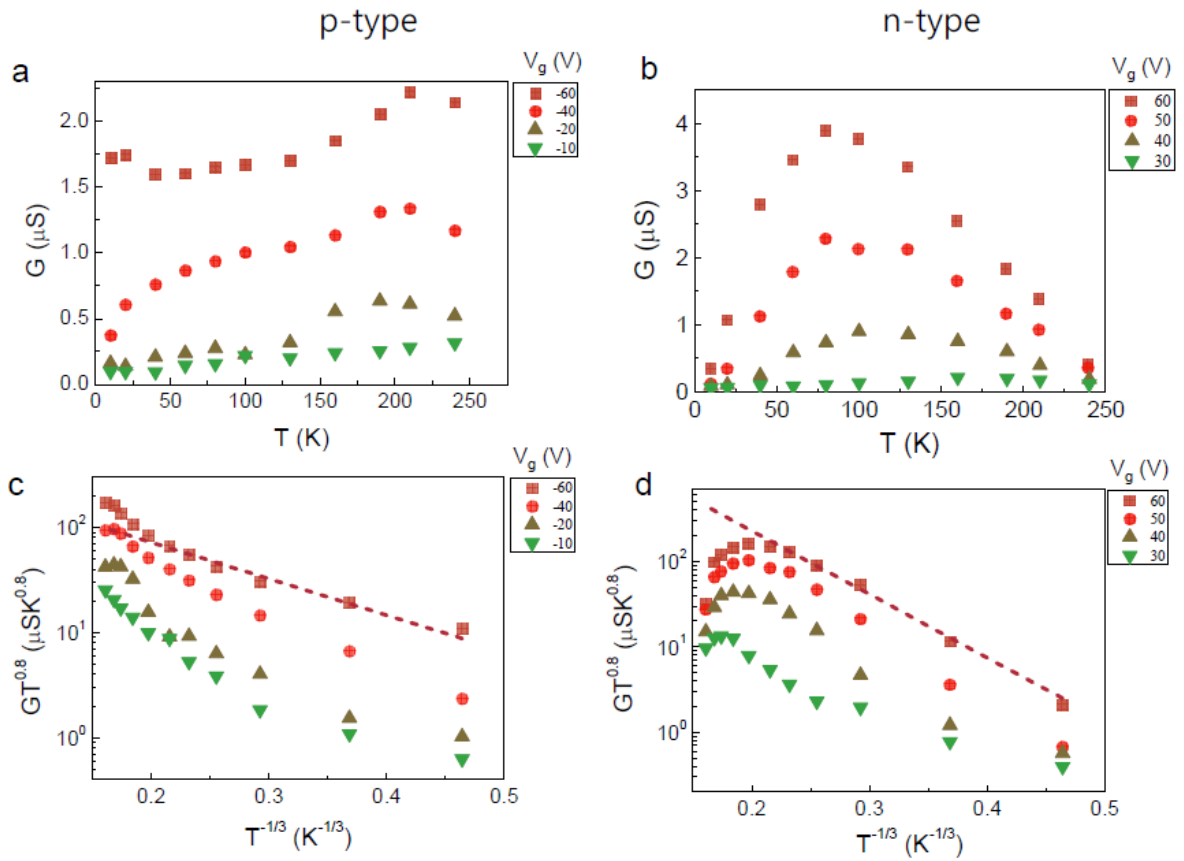
Figure S19. 2D Mott's VRH models for electrical transport in BP3 after coating a PMMA layer.

a,b, conductance (G) as a function of temperature (T) for *p*- and *n*-doped regions, respectively. G in **b** decreases with increasing temperature $T > 100$ K, which could be related to the metallic phase. **c,d,** Mott's VRH model: $GT^{0.8}$ vs. $T^{1/3}$ for *p*- and *n*-doped regions, respectively. Dashed lines at $V_g = -60$ V and 60 V in **c** and **d**, respectively, were obtained with a relation of $\boldsymbol{G = BT^{-0.8}\exp(T_0/T)^{-1/3}}$ with $T_0 = 5\times10^2$ K and 5×10^3 K, respectively, which are in the same range with those estimated from BP3 before coating a PMMA layer. This indicates that the observed electrical behaviors before and after PMMA treatment are the same although the PMMA on the ~17 nm thick BP reduces the thickness of BP as much as ~2 nm for 3 days. This negligible effect of the reduced thickness on the electrical measurements are probably because the most electronic transport occurs through few bottom BP layers of the device with proper gate-electric fields.

# S8. Reliable tests of conductance and thermoelectric measurements of BP device
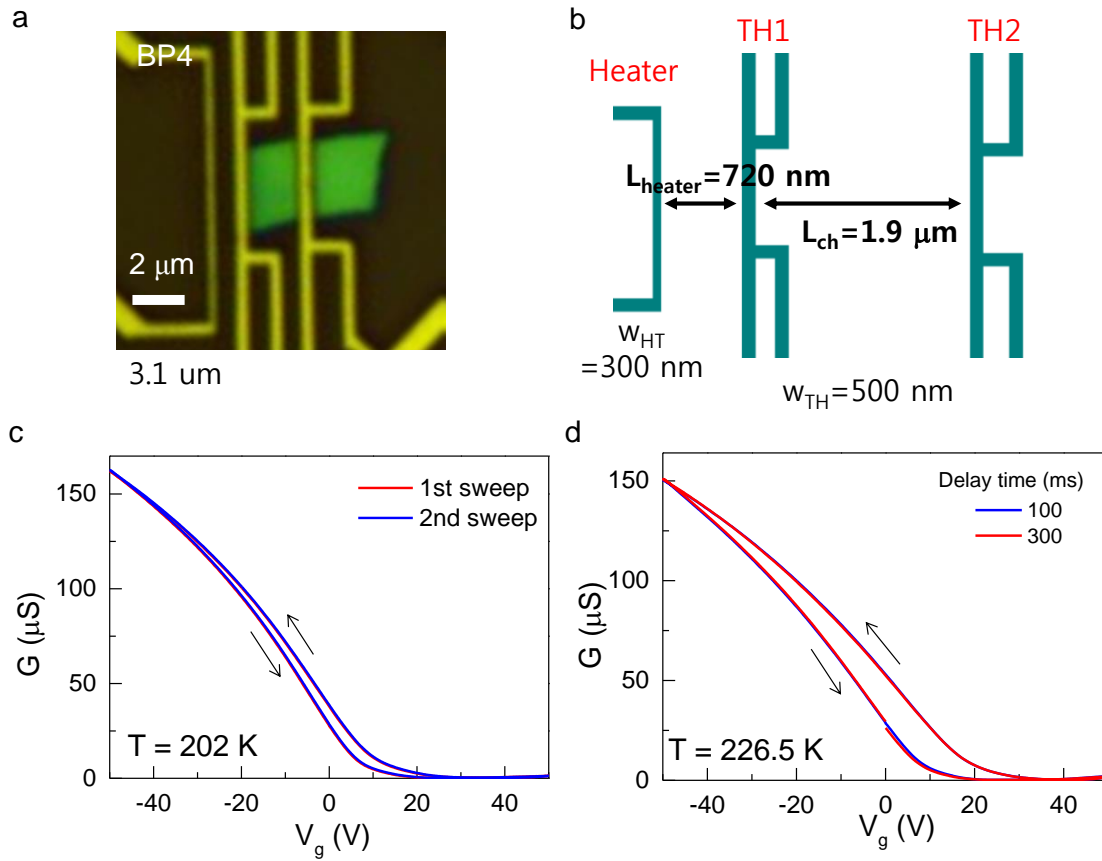
Figure S20. Reliable test of *G-V$_g$* curve of BP4. a,b, optical microscopy image and sample geometry information. Here, we designed that the length of the heater line is sufficiently longer than those of two thermometers to make sure a uniform temperature distribution along the thermometer lines. Here, W_{HT} and W_{TH} are widths of heater and thermometers, respectively. **c,** *G-V$_g$* curves at *T* = 202 K. Although there is a hysteresis, the same sweep direction (see arrows) gives a single curve for two-time repeated measurements (red and blue curves). Our all measurements in the main text were obtained for a forward sweep direction, thus our measurements give consistent data. **d,** Sweep speed dependence of *G-V$_g$* curves at *T* = 226.5 K, which shows the same curves for two delay times of 100 ms (blue curve) and 300 ms (red curve). Here, the delay time is defined as a time interval between two neighbor *V$_g$* values during measurement. This indicates that *G-V$_g$* curve will give the same curve for a delay time > 100 ms. Since *G* and *V$_{TEP}$* have been measured with a delay time, 300 ms and 2 sec,

respectively, for V_g, thus we confirm that our measurements have been performed in a reliable way, although the hysteric curves appeared with increasing temperature.
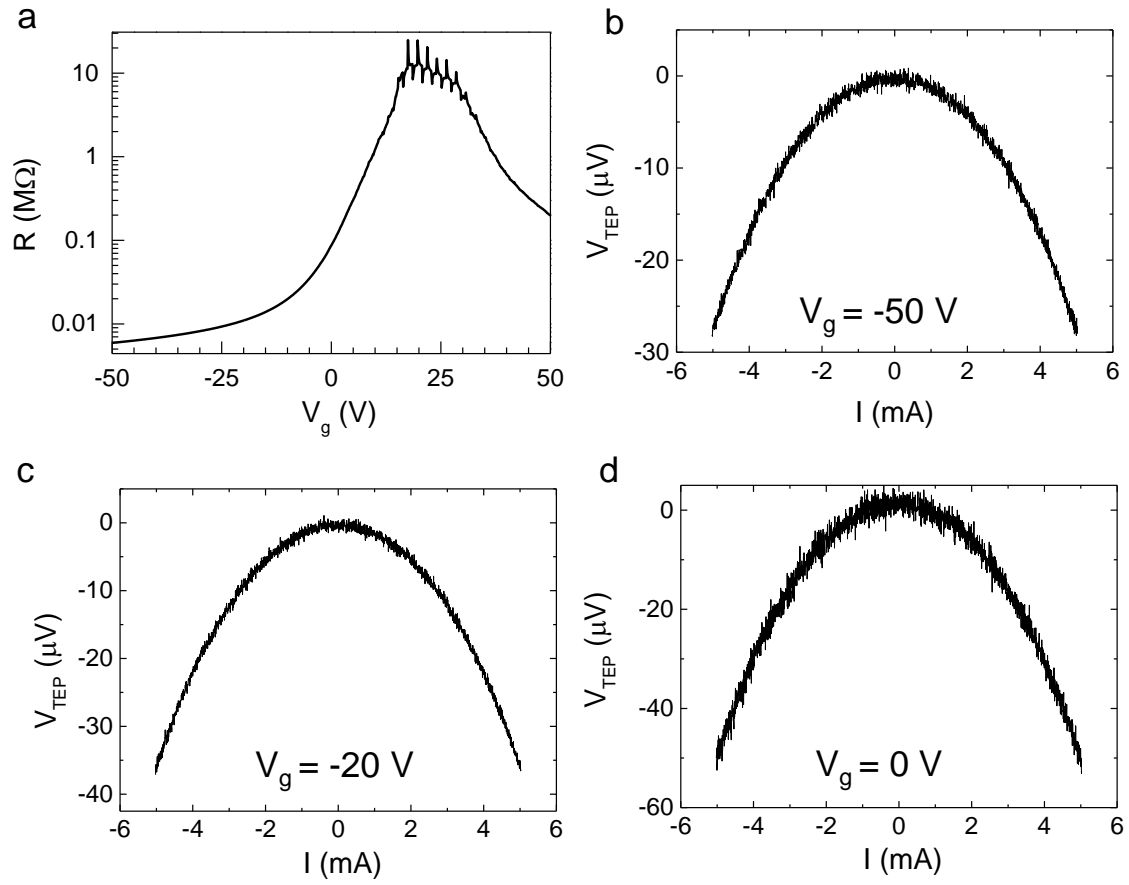

Figure S21. Reliable test of DC thermovoltage measurement in low R_s regions of BP4. a, R-V_g curve at $T = 226.5$ K. **b,c,d,** Thermovoltage (V_{TEP}) as a function of heater current (I) at $V_g = -50$, -20 and 0 V, respectively. The R_s for $V_g < 0$ V is < 0.1 MΩ, where the V_{TEP}-I curves show the parabolic shape as expected.
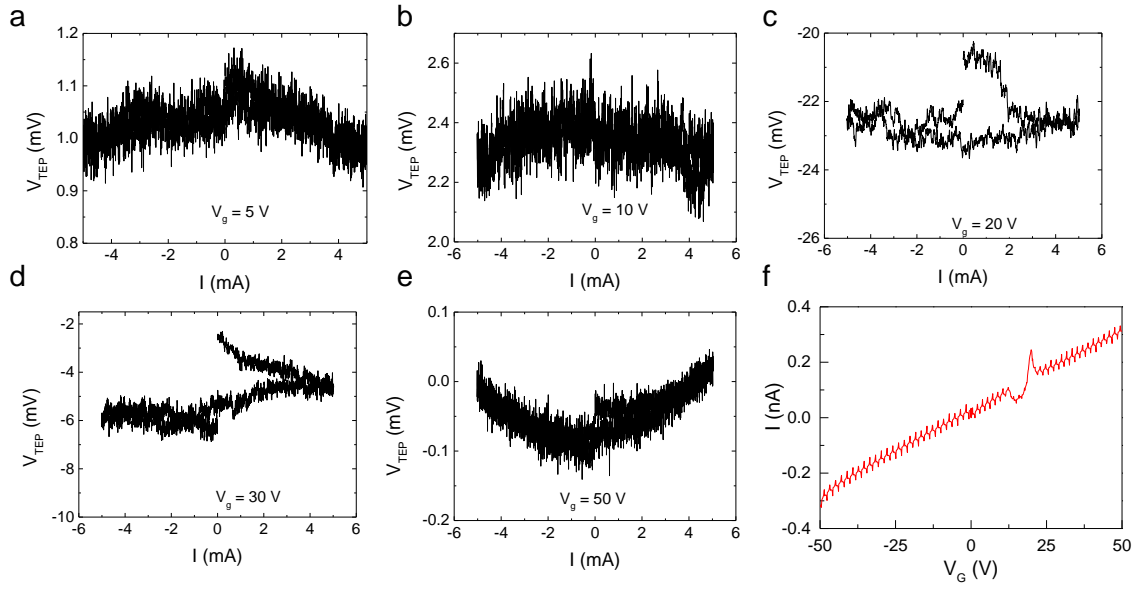
Figure S22. Reliable test of DC thermovoltage measurement in high R_s regions of BP4. a,b,c,d,e, Thermovoltage (V_{TEP}) as a function of heater current (I) at $V_g = 5$ ($R_s = 0.3$ MΩ), 10 (1.24 MΩ), 20 (>10 MΩ), 30 (5.8 MΩ) and 50 V (0.2 MΩ), respectively. Here, R_s value at a given V_g was obtained from Fig. S21a. With increasing R_s, the off-set V_{TEP} at $I = 0$ mA and noise get higher. Interestingly, the gate-leakage current test in **f** shows an abnormal region where leak-current peaks at 12 V < V_g < 23 V, which could cause the relatively high off-set V_{TEP} observed at $V_g = 20$ V in **c**. Thus, it is clear that V_{TEP} for a few MΩ is unreliable for this sample case.

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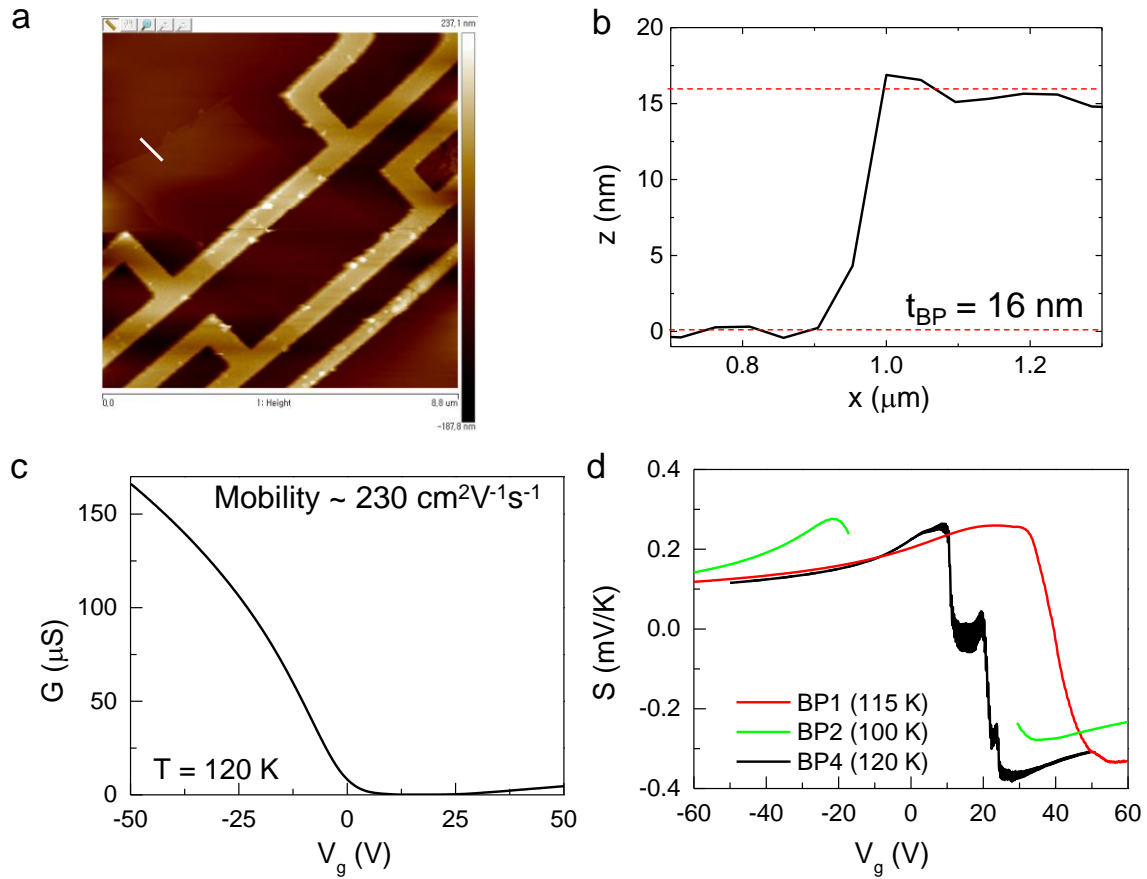
Figure S23. Comparison of _S_ observed in BP1, BP2 and BP4. a, AFM image of BP4. **b,** Height profile along a white line in **a**, which shows that the thickness of BP4 is 16 nm. **c,** Conductance as a function of V_g (G-V_g) for BP4 at $T = 120$ K. The mobility at this temperature was estimated as ~230 $cm^2V^{-1}s^{-1}$, which is in the range of reported values[S9].**d,** Thermopower as a function of V_g (S-V_g) for BP1, BP2 and BP4 at similar temperatures. Regardless of different channel length, _L_ of the three devices ($L = 0.8$ μm for BP1 and BP2, $L = 1.9$ μm for BP4), they showed similar _S_ for highly hole-doped regions, which indicates that the BP channel plays a dominant role in _S_ in the highly doped regions. In the highly doped region, the contributions of the Schottky barrier on the electrical conductance and thermopower get lower and the BP channel is dominant. Near the threshold voltage (V_{th}), however, the Schottky barrier will mainly contribute on the conductance and the thermopower. Figure S14a shows the contact resistance (R_c) as a function of ΔV_g ($= V_g$-V_{th}) of BP1 at $T = 250$ K, where R_c becomes rapidly higher near $\Delta V_g > -10$ V (see red scattered points). This corresponds to V_g ~ 30 V at the temperature. Figure 3c shows _S-T_ curves for $V_g = -60$, 0 and 20 V. Here, the $V_g = 20$ V data show a deviation from the variable range hopping model for $T > 200$ K, which could be because of the thermionic hopping process over the Schottky barriers at the contacts or through the channel.

S9. Thermopower of ~8 nm thick BP device

In the analysis, we assumed that the electrical transport in the BP channel is mainly attributed to the 2D transport through few surface layers of the BP bottom region interfaced by a SiO_2 layer although the number of BP layer is ~60 for the 30 nm thick BP. Recent reports related to the observation of the quantum oscillations and quantum Hall effect in ~10 nm thick BP have shown that there is a charge confinement effect induced by the gate, resulting the narrow quantum well at the interface between the BP and dielectric substrate.[S10-S13] In this view, since a thick BP is effectively composed of 'gated' bottom few-layers in parallel with top 'non-gated' few-layers, the thermopower measured by the top probes becomes a mixed result of parallel layers from the effectively gated-bottom parts and top non-gated parts, leading to an underestimated thermopower responses in a magnitude and temperature dependence from the intrinsic values. To see the thickness effect, we fabricated a ~8 nm thick BP device (BP5) in addition, as shown in Figure S24.

Figures S25a and S25b show G-V_g curves of BP5 for various temperatures and $GT^{0.8}$-$T^{-1/3}$ plot at $V_g = $ -60 V, respectively. The $GT^{0.8}$ as a function of $T^{-1/3}$ (scattered pints) is fitted to the VRH model (solid line) with $T_0 = 5000$ K very well. The conductance map as a function of V_g and V_{sd} at $T = 4.2$ K in Fig. S25c shows multiple quantum dots structure, where the charging energy of the quantum dots are 20~25 meV as indicated by arrows. The values of T_0 and charging energy of quantum dots are consistent with those observed in BP2 in the main text. After correction of the V_{th} at T ~246 K as indicated by an arrow in Fig. S25d, we plotted S-V_g curves for various temperatures in Figure S25e. Figure S25f shows S-T dependence (scattered points) at $V_g = $ -60, -40 and -25 V, where the $S(T)$ follows $T^{1/3}$ behavior, which is also consistent with the VRH model for this ~8 nm thick BP device.
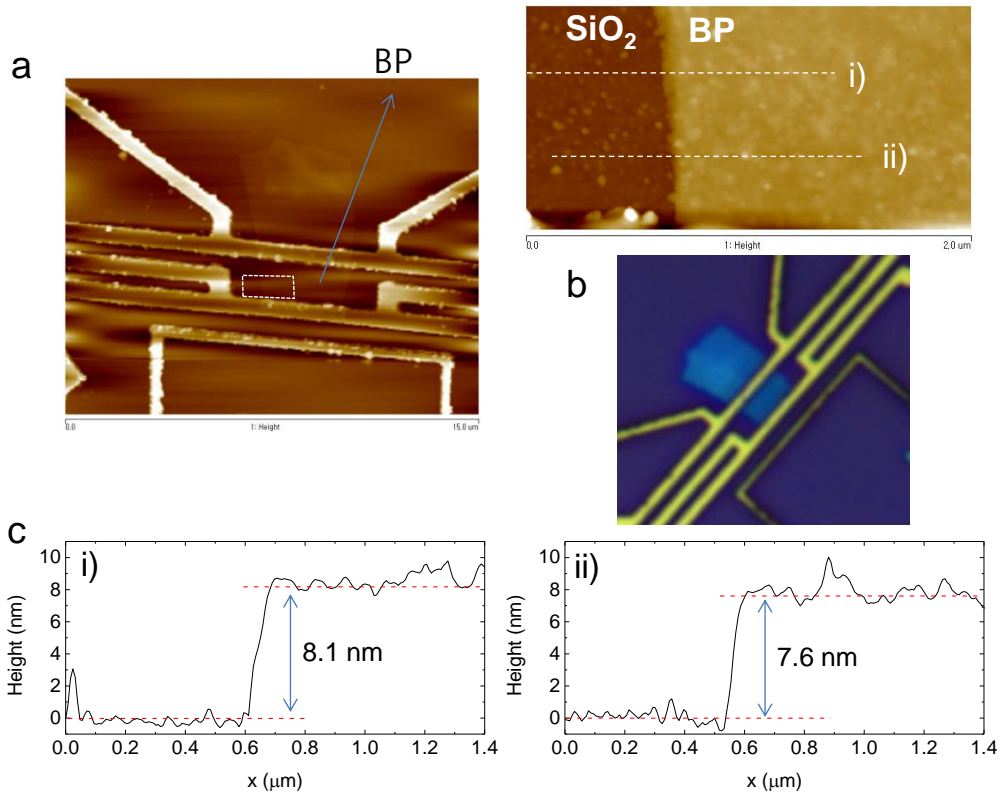
Figure S24. a, Left: AFM image of BP device, BP5. Right: AFM image of a region indicated by a dashed box. **b,** Optical image of the sample. **c,** Height profiles of BP5 along two dashed lines in the right panel of **a**.

Figure S26 shows a summary of *S-T* curves at V_g -V_{th} ~ -60 V for BP1, BP2 and BP5 with thicknesses of 30, 10 and 8 nm, respectively, where we considered the threshold voltage, V_{th} for a proper comparison in the *S* magnitude. The temperature dependence of *S* follows $T^{1/3}$ behavior (as indicated by solid curves) through all samples while *S* values in BP5 are relatively lower than those of BP1 and BP2. With decreasing thickness of BP, the BP devices get sensitive to the charges trapped in the SiO_2 layer. This implies that the VRH mechanism for the charge-carrier transport becomes dominant with decreasing thickness, as reported in a single-layer MoS_2 and bi-layer graphene.[S14,S15] Thus, we expect the $S(T)$ ~ $T^{1/3}$ behavior could be kept for thickness < 10 nm. Importantly, the gating effect through all BP layers gets

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efficient with decreasing thickness of BP, thus, the magnitudes of S would approach to the intrinsic value for a homogeneously gated device, which could be larger than those obtained from relatively thicker devices. However, the S values for 8 nm thick BP5 showed lower magnitudes than other thicker devices. Since the S in the VRH regime gets more sensitive to the extrinsic charge potential with decreasing thickness, it could be hard to show its intrinsic S value, regardless of the efficient gating effect. Thus, one needs to separate the BP device from the extrinsic charge potentials to observe the intrinsic S values. This could be achieved by placing BP flakes on a hexagonal BN layer.
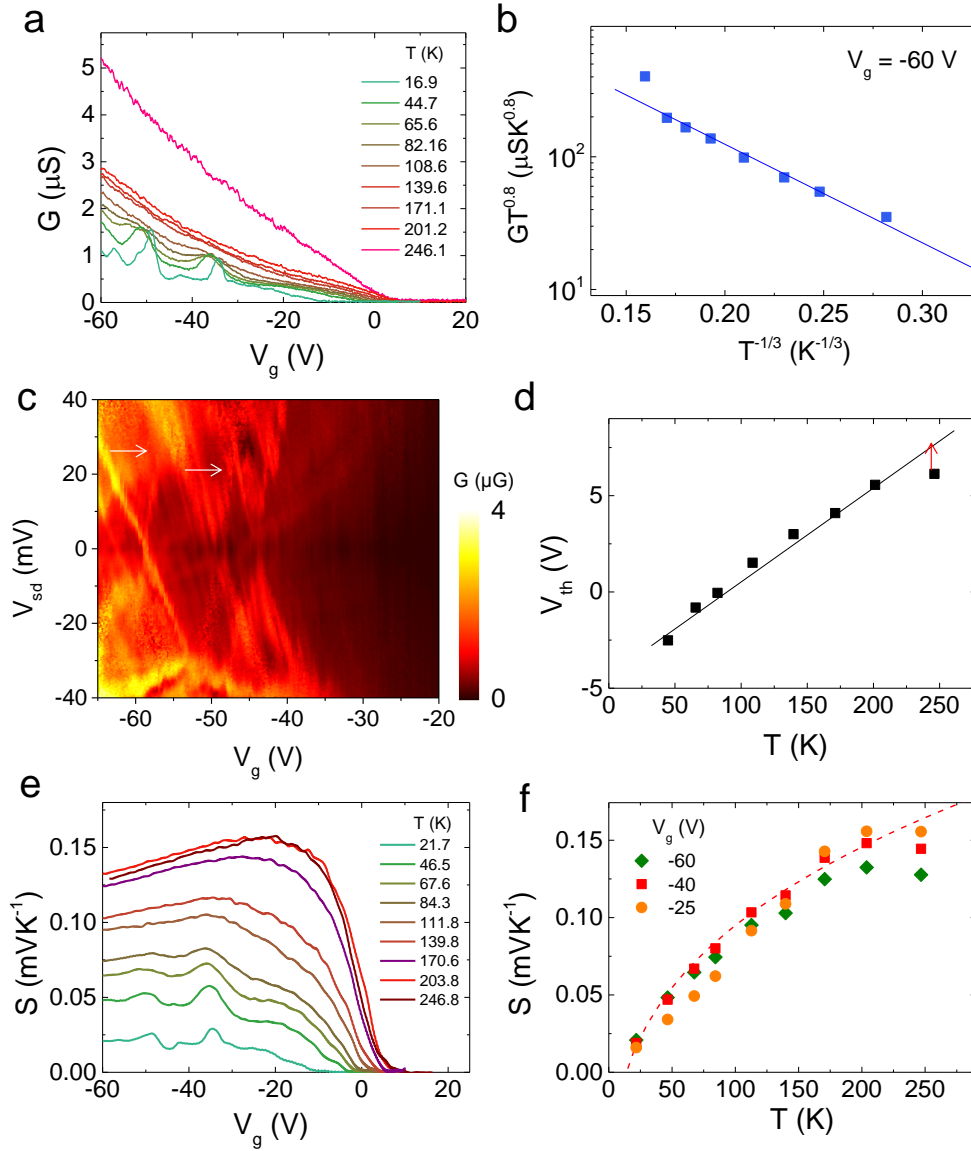
Figure S25. Electrical and thermopower measurement of BP5. a, G-V_g curves for various temperatures. **b,** $GT^{0.8}$-$T^{-1/3}$ curve (scattered points) at V_g = -60 V. solid line: fit result with the VRH model. **c,** Conductance map as a function of V_{sd} and V_g at T = 4.2 K. **d,** Threshold voltage as a function of temperature (V_{th}-T). **e,** Thermopower as a function of V_g (S-V_g) for various temperatures. **f,** S-T plots (scattered points) at V_g = -60, -40 and -25 V. dashed curve: fit result with the VRH model.
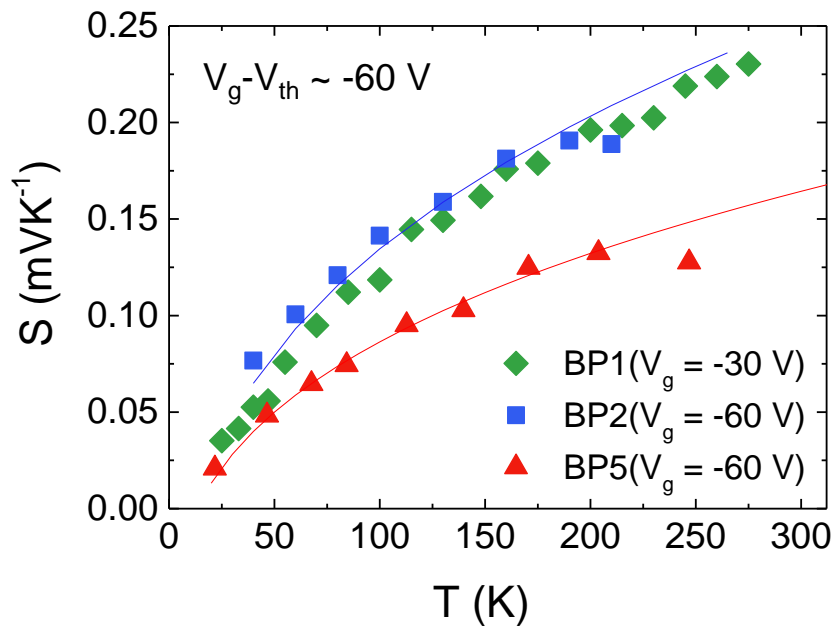
Figure S26. Summary of temperature dependence of S of BP1, BP2 and BP5.

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