2D Materials

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LETTER

Reduction of hysteresis in MoS_2 transistors using pulsed voltage measurements

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Abstract

Transistors based on two-dimensional (2D) materials often exhibit hysteresis in their electrical measurements, i.e. a dependence of measured current on voltage sweep direction due to charge trapping. Here we demonstrate a simple pulsed measurement technique which reduces this hysteretic behavior, enabling more accurate characterization of 2D transistors. We compare hysteresis and charge trapping in four types of devices fabricated from both exfoliated and synthetic MoS_2, with SiO_2 and HfO_2 insulators, using DC and pulsed voltage measurements at different temperatures. Applying modest voltage pulses (~1 ms) on the gate significantly reduces charge trapping and results in the elimination of over 80% of hysteresis for all devices. At shorter pulse widths (~1 μs), up to 99% of hysteresis is reduced for some devices. Our measurements enable the extraction of a unique value of field-effect mobility, regardless of voltage sweep direction, unlike measurements that rely on forward or backward DC measurements. This simple and reproducible technique is useful for studying the intrinsic properties of 2D transistors, and can be similarly applied to other nanoscale and emerging devices where charge trapping is of concern.

1. Introduction

Two-dimensional (2D) semiconductors like molybdenum disulfide (MoS_2) are promising for applications in low-power electronics due to their electrical properties, atomically thin nature, and lack of dangling bonds [1, 2]. The electrical characteristics, including current drive, mobility, and current on/off ratio, of MoS_2 field-effect transistors (FETs) have been widely studied over the last several years [1–10]. However, DC electrical measurements of these and most novel devices often exhibit hysteresis in their current versus gate voltage (I_D–V_{GS}) measurements. Hysteresis, defined here as the difference in threshold voltage (V_T) between the reverse and forward voltage sweeps (ΔV_T), typically depends on voltage sweep rate, sweep direction, sweep range, and environmental conditions during the measurement [7, 11–13]. The difference in I_D–V_{GS} curves is due to trapped charges on the surface of the MoS_2, in the gate dielectric, at the MoS_2/dielectric interface, or in the MoS_2 itself [7–10, 13–16]. Electrostatic screening by adsorbed water molecules, with electric dipoles aligned along the gate-induced electric field, has also been proposed as a contributor to this hysteresis [6, 7, 17]. As field-effect mobility (μ_{FE}) and V_T are often extracted from I_D–V_{GS} sweeps in the forward or reverse direction, hysteresis in DC measurements leads to uncertainty in the electrical characteristics of such 2D devices. While hysteresis can be reduced through device encapsulation, e.g. with a high-quality Al_2O_3 dielectric [18] the majority of new and prototype devices are often tested without encapsulation or in air, where their electrical evaluation remains challenging.

In this study, we apply voltage pulses to the gates of MoS_2 transistors to eliminate hysteresis, examine charge trapping, and extract device parameters (like mobility) that represent the intrinsic behavior of these devices. Using this simple yet effective technique, hysteresis is nearly eliminated, which we quantify as

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a reduction by more than 80% under all conditions tested (~99% in some cases), and the extracted mobility converges to a unique value. We apply this technique to FETs fabricated using both exfoliated and synthetic, chemical vapor deposition (CVD) grown MoS_2, as well as different gate dielectrics (SiO_2 and HfO_2). We compare the different types of devices and examine the effects of air versus vacuum and temperature-dependent measurements on hysteresis. Finally, we use a tunneling front model to examine the depths of charge traps in our gate dielectrics.

2. Results and discussion

Four types of MoS_2 transistors were examined in this work: exfoliated multi-layer (ML) and monolayer (1L) devices with global back-gates, as well as CVD-grown monolayer devices with global and local back-gates. All MoS_2 channels were lithographically patterned and etched into rectangles using either XeF_2, which was used for exfoliated devices, or O_2, which was used for CVD-grown devices (conditions for XeF_2 and O_2 etches can be found in the supplements of [3, 19], respectively). Contacts to all devices were patterned by optical lithography or electron-beam (e-beam) lithography with either Ni, Ag, or Au contacts, consistent with previous studies from our group [3, 19]. Optical images of all devices are shown in figures 1(a)–(d). Typical global and local back-gated (LBG) device schematics with biasing setups are displayed in figures 1(a) and (d) respectively. Figures 1(e) and (f) shows the pulsed measurement scheme (for details see Methods section). We introduce each device configuration in the sections below and then make comparisons between the different devices, discussing the overall results.

2.1. Exfoliated multi-layer MoS_2 devices

Exfoliated ML (~5 nm thick) MoS_2 devices were prepared as described in [3], here with Ni contacts (40 nm) on SiO_2 (90 nm) and Si (p^+) substrates, which also serve as global back-gates. Figure 1(a) shows an optical image and a schematic of Devices 1 and 2 with channel lengths $L_1 = 1.5$ μm, $L_2 = 1.25$ μm, and widths $W_{1,2} = 2.5$ μm. Device 3 (not shown) has dimensions $L_3 = 1.7$ μm and $W_3 = 1$ μm. DC and pulsed drain current (I_D) measurements are performed by forward and backward sweeps of gate voltage V_{GS} from −10 V to 25 V, with drain voltage $V_{DS} = 1$ V. We vary the pulse widths from $t_{on} = 500$ μs to 500 ms, with $t_{off} = 500$ ms and rise and fall times $t_{R,F} = 10$ μs (see figures 1(e)–(f) and Methods section for more details).

Figures 2(a) and (b) show the DC and pulsed I_D–V_{GS} measurements of Device 1 at room temperature in air and in vacuum (~10^{-5} Torr), respectively, after annealing in the vacuum probe station at 250 °C for 2 h. The forward and reverse sweeps, as well as the hysteretic difference in threshold voltage between the two sweeps (ΔV_T), are indicated in figure 2(a). For simplicity, each V_T is extracted using the constant current method at $I_D = 0.7$ μA μm^{-1} [20].

These n-type MoS_2 devices are dominated by donor-like trap states [6, 21], as follows. Under negative V_{GS}, the Fermi level in the MoS_2 channel moves closer to the valence band. The traps above the Fermi level are emptied of electrons and have positive charge, causing a negative V_T shift. Under positive V_{GS}, electrons fill the charge traps, rendering them neutral and leading to a positive V_T shift. Electrons remain trapped until the reverse sweep, during which they de-trap [22, 23]. This is illustrated in the band diagrams of figure 2(c), which show how electrons trap and de-trap under positive and negative V_{GS}. The V_T shift causes the forward I_D–V_{GS} curve to look 'stretched' and the reverse 'compressed,' leading to clockwise hysteresis. Clearly, these effects also render any field-effect mobility estimates from such DC measurements to be incorrect with respect to the 'true' mobility of the device. In contrast, pulsed measurements (as in figure 1) minimize hysteresis when t_{on} is smaller than the time constants of most traps, and smaller than alignment times of water molecule electric dipoles. A short t_{on} prevents traps from becoming populated [12, 24] or water dipoles from becoming aligned with the gate-induced field [6, 7, 17]. Additionally, during t_{off}, some of the trapped charge de-traps [9, 11] and surface-adsorbed water dipoles relax and become unaligned.

Figure 2(d) shows a reduction in ΔV_T as the pulse widths (t_{on}) decrease for Devices 1–3, both in air and in vacuum. We note that ΔV_T is larger in air than in vacuum due to increased charge trapping from air and water adsorbates and the effect of water dipoles on the surface [6, 7, 9, 13, 14, 17, 25, 26]. This suggests that *top surface* contaminants in air are more influential than MoS_2/SiO_2 interface traps or bulk traps, because performing DC measurements in vacuum leads to a reduction in ΔV_T of ~90%. However, as these devices have ΔV_T ~ 0.5–1 V for DC measurements even after the 250 °C vacuum anneal and 12 h in vacuum, we conclude that surface traps do not account for all the hysteresis in these devices. The MoS_2/SiO_2 interface likely has charge traps from dangling bonds at the surface of the SiO_2, and the hysteresis may result from shallow traps at the interface during the V_{GS} sweep [27, 28]. Other sources of traps stem from defects in bulk SiO_2 and the few-layer MoS_2 itself [8, 10, 11, 14, 27, 29].

Quantitatively, with modest pulses of $t_{on} = 1$ ms and $t_{off} = 500$ ms applied to all devices, $\Delta V_T \leqslant 0.73$ V in air and 0.07 V in vacuum, which corresponds to a reduction in hysteresis by ~92% and ~84%, respectively, compared to DC measurements. At the shortest pulse width ($t_{on} = 500$ μs), hysteresis is reduced by nearly 97% and 90% in air and vacuum, respectively. Accounting for the oxide thickness, we can convert this 'residual hysteresis' into an effective interface trap density (N_{it}):

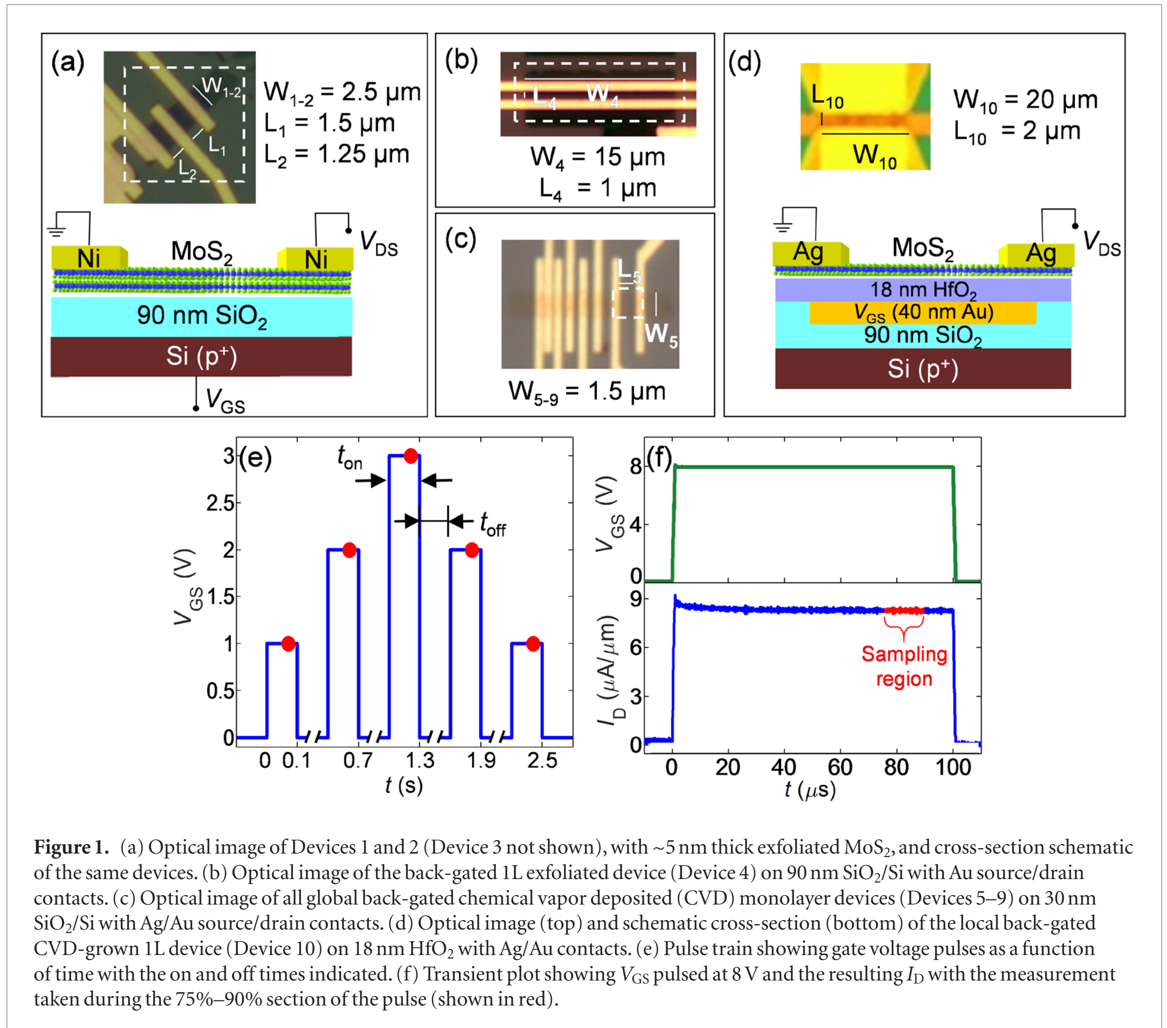

Figure 1. (a) Optical image of Devices 1 and 2 (Device 3 not shown), with ~5 nm thick exfoliated MoS_2, and cross-section schematic of the same devices. (b) Optical image of the back-gated 1L exfoliated device (Device 4) on 90 nm SiO_2/Si with Au source/drain contacts. (c) Optical image of all global back-gated chemical vapor deposited (CVD) monolayer devices (Devices 5–9) on 30 nm SiO_2/Si with Ag/Au source/drain contacts. (d) Optical image (top) and schematic cross-section (bottom) of the local back-gated CVD-grown 1L device (Device 10) on 18 nm HfO_2 with Ag/Au contacts. (e) Pulse train showing gate voltage pulses as a function of time with the on and off times indicated. (f) Transient plot showing V_{GS} pulsed at 8 V and the resulting I_D with the measurement taken during the 75%–90% section of the pulse (shown in red).

$$N_{it} = \frac{1}{q} C_{ox} \Delta V_T, \tag{1}$$

where $C_{ox} \approx 38$ nF cm^{-2} is the capacitance per unit area of the 90 nm thick SiO_2 used here and q is the elementary charge. Thus, we estimate $N_{it}(\text{air}) \leqslant 1.8 \times 10^{11}$ cm^{-2} and $N_{it}(\text{vacuum}) \leqslant 1.7 \times 10^{10}$ cm^{-2} at $t_{on} = 1$ ms. For these devices, this implies that at least ten times more hysteresis is caused by surface-adsorbed contaminants or water dipoles (pulsed measurements in air) than is trapped in MoS_2 defects or the SiO_2 interface beneath (measurements in vacuum). We note that the density of defects in the MoS_2 could be higher, but not all defects are active charge traps. In addition, due to the thinness of the MoS_2, most charge traps within it are likely to have very fast time constants, much faster than our pulse times. Nevertheless, for a highly-scaled equivalent oxide thickness (EOT) of 1 nm, the equivalent hysteresis would be less than ~8.2 mV and ~0.78 mV, much smaller than a scaled 1 V supply voltage.

We calculate the field-effect mobility μ_{FE} as

$$\mu_{FE} \approx \frac{L}{W C_{ox} V_{DS}} \frac{dI_D}{dV_{GS}}. \tag{2}$$

We note that μ_{FE} is an underestimate of the actual mobility since we do not account for contact resistance in our measurements. μ_{FE} for all three devices is reported at a carrier density of $n_{2D} = 2.8 \times 10^{12}$ cm^{-2}, where n_{2D} is estimated assuming a linear charge dependence on the gate overdrive voltage, $n_{2D} \approx C_{ox}(V_{GS}–V_T)/q$. The plot of μ_{FE} for Devices 1–3 in air and in vacuum versus pulse width is shown in figure 2(e), at room temperature. As t_{on} pulse widths decrease, the mobility values extracted from the forward and reverse sweeps converge to a single value. Therefore, pulsed measurements enable the extraction of a unique mobility value, while μ_{FE} extracted from forward or reverse DC measurements would be either an under- or an overestimate, respectively. This observation could, in part, explain the large spread of MoS_2 mobility values reported in the literature when extractions were obtained purely from DC forward (or backward) sweeps.

We have also performed temperature-dependent DC and pulsed measurements in vacuum. The hysteresis is largest at 375 K, as shown in figure 2(f), suggesting the presence of thermally activated traps [9, 30]. The measured ΔV_T at 150 K, 225 K, and 300 K display similar trends as a function of t_{on}, and have the highest values during DC measurements. ΔV_T is effectively eliminated at all temperatures when $t_{on} \leqslant 10$ ms, demonstrating that most traps have time constants longer

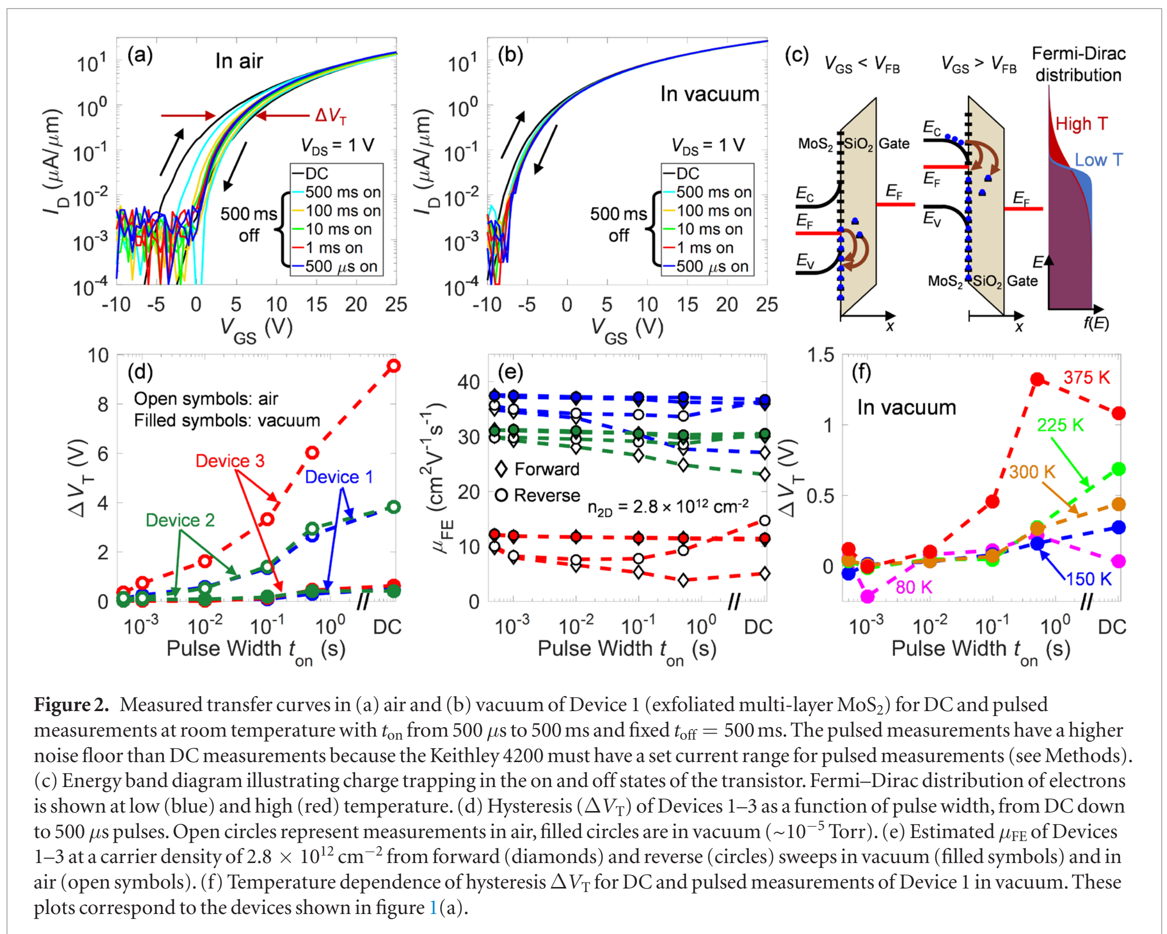

Figure 2. Measured transfer curves in (a) air and (b) vacuum of Device 1 (exfoliated multi-layer MoS_2) for DC and pulsed measurements at room temperature with t_{on} from 500 μs to 500 ms and fixed t_{off} = 500 ms. The pulsed measurements have a higher noise floor than DC measurements because the Keithley 4200 must have a set current range for pulsed measurements (see Methods). (c) Energy band diagram illustrating charge trapping in the on and off states of the transistor. Fermi–Dirac distribution of electrons is shown at low (blue) and high (red) temperature. (d) Hysteresis (ΔV_T) of Devices 1–3 as a function of pulse width, from DC down to 500 μs pulses. Open circles represent measurements in air, filled circles are in vacuum (~10^{-5} Torr). (e) Estimated μ_{FE} of Devices 1–3 at a carrier density of 2.8×10^{12} cm^{-2} from forward (diamonds) and reverse (circles) sweeps in vacuum (filled symbols) and in air (open symbols). (f) Temperature dependence of hysteresis ΔV_T for DC and pulsed measurements of Device 1 in vacuum. These plots correspond to the devices shown in figure 1(a).

than 10 ms. ΔV_T at 80 K is smaller than at any other temperature for the DC measurement and is nearly constant with decreasing pulse width. This apparent freeze-out of traps at low temperature is consistent with previous studies [12, 25, 31, 32].

The behavior of hysteresis with respect to temperature matches our expectations based on the temperature-dependence of charge trapping mechanisms [33]. The capture rate of electrons is proportional to $T^2 \exp\left[\frac{E_F - E_C}{kT}\right][1 - f(E_T)]$, where T is temperature, E_F is the Fermi level, E_C is the conduction band edge of MoS_2, k is the Boltzmann constant, E_T is the energy level of the trap, and $f(E_T)$ is the Fermi Dirac distribution at energy E_T [34]. The emission rate of electrons from trap states is proportional to $T^2 \exp\left[\frac{E_T - E_C}{kT}\right] f(E_T)$ [34]. The first exponential term will dominate in most cases for both the capture and emission rates, but broadening of the Fermi function can also slightly modify these rates, as shown in figure 2(c). If $E_F > E_T$, the capture rate will be larger than the emission rate at both high and low temperatures, leading to hysteresis. Due to the exponential dependence on temperature, however, the capture rate at high temperatures will be significantly larger than at low temperatures, which agrees with our observation of larger hysteresis at 375 K than at 80 K or 150 K. At lower temperatures, the electron capture and emission rates are greatly reduced, effectively 'freezing' the traps in their current states, resulting in minimal to no hysteresis. If $E_F < E_T$, the emission rate will be larger than the capture rate, which will not contribute much to hysteresis since the trap states are more likely to remain empty.

2.2. Exfoliated monolayer MoS_2 devices

As before, we prepare MoS_2 devices by exfoliation from bulk MoS_2 onto SiO_2 (90 nm) and Si (p^+) substrates. Monolayer (1L) regions are identified by optical contrast and confirmed with Raman and photoluminescence measurements (see supplementary figure S1 (stacks.iop.org/TDM/6/011004/mmedia)). We fabricate FETs with Au contacts (40 nm thick) using methods described previously (see section 3 for a discussion on the effect of different contact metals on hysteresis). An optical image of Device 4 (with dimensions W_4 = 15 μm and L_4 = 1 μm) can be seen in figure 1(b). Similar to the ML devices, we anneal these FETs in vacuum at 250 °C before the measurements. DC and pulsed measurements are then performed, without breaking vacuum, by forward and backward sweeps of V_{GS} from −30 V to 30 V with V_{DS} = 1 V. Again, pulse widths vary from t_{on} = 500 μs to 500 ms, with a t_{off} = 500 ms and $t_{R,F}$ = 10 μs.

The I_D–V_{GS} curves from the DC and pulsed measurements are shown in figure 3(a). While these transfer curves may exhibit little hysteresis at DC, our pulsed measurement technique nevertheless provides additional insight into charge trap states present in the system. To illustrate this, we extract ΔV_T from our I_D–V_{GS} curves, using the constant current method with I_D = 1

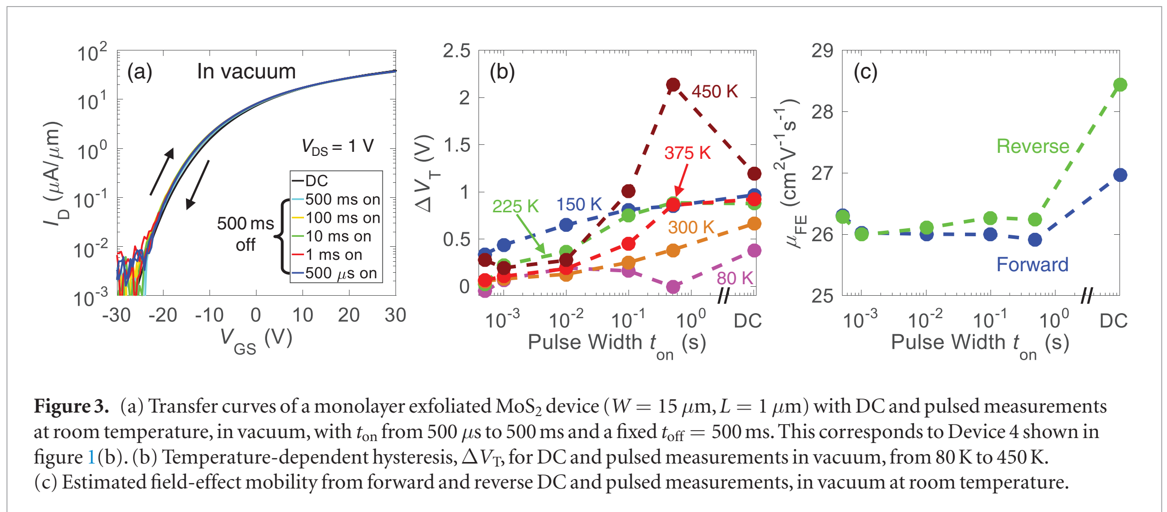

Figure 3. (a) Transfer curves of a monolayer exfoliated MoS_2 device ($W = 15$ µm, $L = 1$ µm) with DC and pulsed measurements at room temperature, in vacuum, with t_{on} from 500 µs to 500 ms and a fixed $t_{off} = 500$ ms. This corresponds to Device 4 shown in figure 1(b). (b) Temperature-dependent hysteresis, ΔV_T, for DC and pulsed measurements in vacuum, from 80 K to 450 K. (c) Estimated field-effect mobility from forward and reverse DC and pulsed measurements, in vacuum at room temperature.

µA µm^{-1}, for temperatures from 80 K to 450 K and plot them versus t_{on} in figure 3(b). Across all temperatures, we see that the hysteresis is reduced as t_{on} decreases. The substantial increase in ΔV_T at 450 K is indicative of the presence of thermally activated traps, as seen in the ML devices [9, 30]. For $t_{on} \leqslant 100$ ms, ΔV_T at 450 K is comparable to ΔV_T at lower temperatures, suggesting that most of the thermally activated traps have time constants >100 ms. The discrepancy of ΔV_T between $t_{on} = 500$ ms and DC also suggests that the thermally activated traps have de-trapping time constants >500 ms. This occurs because DC measurements take ~250 ms per voltage step (see Methods section), meaning that pulsed measurements with $t_{on} = 500$ ms bias the device for approximately twice as long as DC. If the thermally activated traps have de-trapping time constants greater than t_{off}, then we would expect more hysteresis at $t_{on} = 500$ ms.

In addition to the thermally activated traps, we note that hysteresis at 150 K and 450 K is not completely eliminated at the shortest pulse width of 500 µs. We expect a shorter t_{on} to eliminate this remaining hysteresis; however, $t_{on} < 500$ µs is not possible with our set-up because parasitic capacitances, stemming from the use of our probe station chuck as a global back-gate, cause a charging current on the same time scale as charge trapping, interfering with the drain current measurements. This highlights a limitation of the pulsed measurement technique when the substrate is used as a global back-gate. However, at 300 K, we find that hysteresis is reduced by ~88% at modest pulses of $t_{on} = 1$ ms with $\Delta V_T \sim 0.08$ V, corresponding to $N_{it} \approx 1.9 \times 10^{10}$ cm^{-2} and $\Delta V_T \sim 0.78$ mV at an EOT of 1 nm. For the best case ($t_{on} = 500$ µs), hysteresis is reduced by ~92% to $\Delta V_T \sim 0.05$ V. Additionally, we find that mobilities extracted from the forward and reverse sweeps converge to a single value at $t_{on} \leqslant 1$ ms, as shown in figure 3(c). Once again, the pulsed measurement technique yields a reliable mobility estimate, whereas using either the forward or reverse DC sweeps could yield inconsistent mobility values.

2.3. CVD MoS_2 devices (global back-gate)

We also investigate 1L MoS2 devices grown by CVD directly on SiO_2 (30 nm) and Si (p^+) substrates, probing FETs with Ag/Au (20 nm/20 nm) contacts [5, 19]. The MoS_2 channel width for Devices 5–9 is $W_{5–9} = 1.5$ µm, and the channel lengths are $L_{5–9} =$ 50 nm, 100 nm, 200 nm, 600 nm, and 1 µm, as shown in figure 1(c). As before, the devices are annealed in the vacuum probe station at 250 °C, and subsequent measurements are performed without breaking vacuum, at room temperature. We perform DC and pulsed measurements by sweeping V_{GS} from −5 V to 30 V with $V_{DS} = 1$ V. As before, t_{on} varies from 500 µs to 500 ms, with $t_{off} = 500$ ms and $t_{R,F} = 10$ µs.

Figure 4(a) shows the DC and pulsed I_D–V_{GS} curves of Device 5 ($L = 1$ µm) with the arrows indicating the forward and reverse sweeps. The reduction in hysteresis with decreasing pulse width is clearly illustrated in figure 4(b), where V_T was extracted at $I_D = 1$ µA µm^{-1}. The DC measurement for Device 5 has ΔV_T ~ 1.4 V, and hysteresis is reduced by ~89% at $t_{on} = 1$ ms with $\Delta V_T \sim 0.08$ V, corresponding to an active charge trap density of $N_{it} \sim 5.8 \times 10^{10}$ cm^{-2}. The difference in the estimated μ_{FE} between the forward and backward sweeps (figure 4(c)) for the DC measurement is ~5.7 cm^2 V^{-1} s^{-1} and reduces to just 0.24 cm^2 V^{-1} s^{-1} at $t_{on} = 1$ ms. The latter is <2% of the estimated mobility (~16 cm^2 V^{-1} s^{-1}), which thus converges to a unique value in the limit of these shortest pulses. As before, we note these mobility values include the contacts, and the intrinsic mobility of these films is higher, as discussed elsewhere [5, 19].

We compare ΔV_T for the different devices to determine the correlation between hysteresis and channel length, if any. Figure 4(b) reveals no clear trend of hysteresis with channel length, as all device lengths have the same trend in hysteresis versus pulse width. Given that shorter channel devices have stronger effect of contacts [3], this suggests that the hysteresis observed in our devices is *not* a contact effect, and is largely due to active charge traps distributed along the device channel lengths.

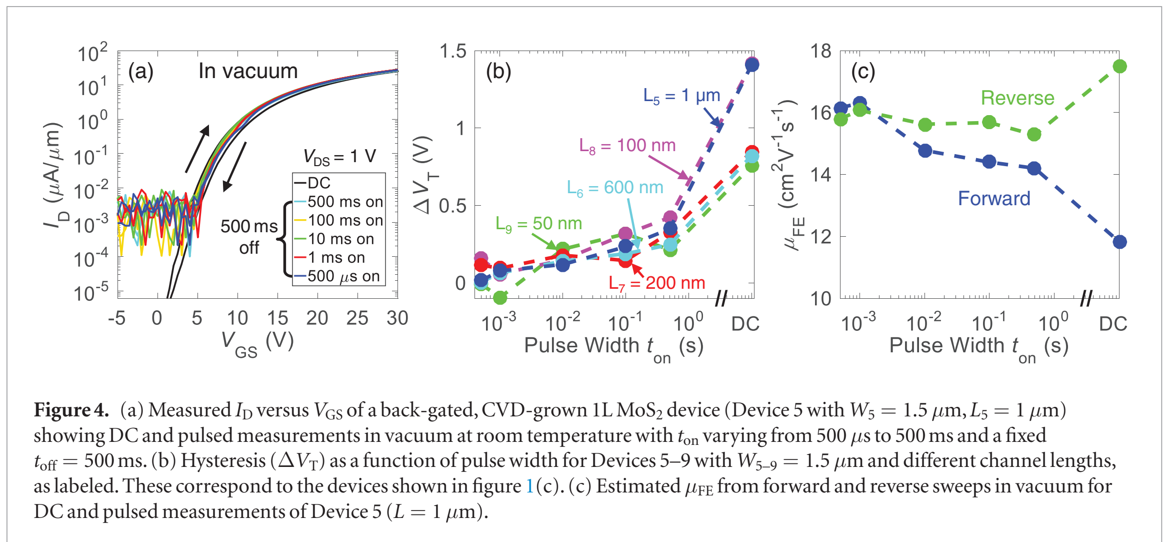

Figure 4. (a) Measured I_D versus V_{GS} of a back-gated, CVD-grown 1L MoS_2 device (Device 5 with $W_5 = 1.5\ \mu m$, $L_5 = 1\ \mu m$) showing DC and pulsed measurements in vacuum at room temperature with t_{on} varying from 500 μs to 500 ms and a fixed $t_{off} = 500$ ms. (b) Hysteresis (ΔV_T) as a function of pulse width for Devices 5–9 with $W_{5\text{–}9} = 1.5\ \mu m$ and different channel lengths, as labeled. These correspond to the devices shown in figure 1(c). (c) Estimated μ_{FE} from forward and reverse sweeps in vacuum for DC and pulsed measurements of Device 5 ($L = 1\ \mu m$).

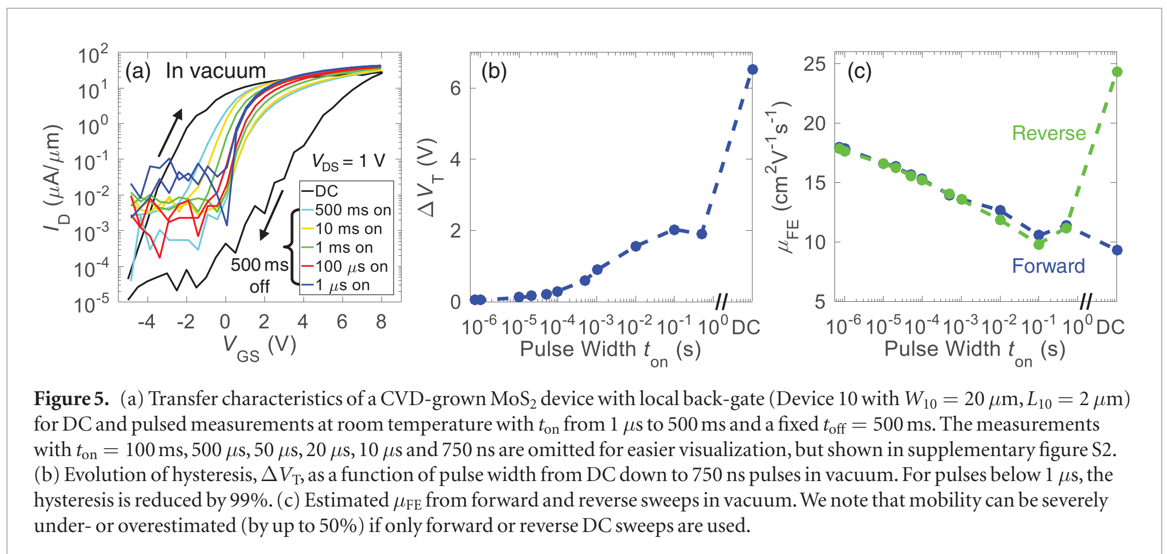

Figure 5. (a) Transfer characteristics of a CVD-grown MoS_2 device with local back-gate (Device 10 with $W_{10} = 20\ \mu m$, $L_{10} = 2\ \mu m$) for DC and pulsed measurements at room temperature with t_{on} from 1 μs to 500 ms and a fixed $t_{off} = 500$ ms. The measurements with $t_{on} = 100$ ms, 500 μs, 50 μs, 20 μs, 10 μs and 750 ns are omitted for easier visualization, but shown in supplementary figure S2. (b) Evolution of hysteresis, ΔV_T, as a function of pulse width from DC down to 750 ns pulses in vacuum. For pulses below 1 μs, the hysteresis is reduced by 99%. (c) Estimated μ_{FE} from forward and reverse sweeps in vacuum. We note that mobility can be severely under- or overestimated (by up to 50%) if only forward or reverse DC sweeps are used.

2.4. CVD MoS_2 devices (local back-gate)

Finally, we examine devices with CVD-grown 1L MoS_2 *transferred* onto 18 nm of HfO_2 above a local Au back-gate (the MoS_2 was previously synthesized onto a separate SiO_2/Si substrate [5]). Details of the MoS_2 transfer process are presented in supplementary section II. The source and drain contacts are patterned to overlap slightly with the local back-gate (figure 1(d)), meaning that the MoS_2 channel is only gated through the HfO_2 dielectric and electrical hysteresis is entirely due to the MoS_2/HfO_2 interface. We study these devices because they typically present a more extreme level of hysteresis compared to the earlier test cases. In addition, the physically smaller local back-gate lowers parasitic capacitances, allowing pulse widths down to 750 ns to be used for device characterization. Figure 1(d) shows a schematic and an optical image of Device 10 with dimensions $W_{10} = 20\ \mu m$, $L_{10} = 2\ \mu m$, and Ag/Au (25/25 nm) contacts [19]. DC and pulsed measurements are performed in vacuum (after the anneal step described earlier) by a forward and backward sweep of V_{GS} from −5 V to 8 V with $V_{DS} = 1$ V, and V_T extracted at $I_D = 1\ \mu A\ \mu m^{-1}$.

We record both the DC and pulsed measurement I_D–V_{GS} curves as seen in figure 5(a). We note that figure 5(a) omits some of the pulsed measurements for easier visualization, but supplementary figure S2 shows the transfer curves at all t_{on}. Similar to observations for the other devices, the forward and reverse I_D–V_{GS} sweeps converge to a single curve and ΔV_T decreases as the pulse width t_{on} is reduced (figure 5(b)). At $t_{on} = 1$ ms, hysteresis is reduced by ~86% with $\Delta V_T = 1$ V, which is still significant. The larger overall hysteresis in the *transferred* CVD-grown MoS_2 devices is attributed to traps introduced at the MoS_2/HfO_2 interface during the imperfect transfer process (supplementary section II), and use of the HfO_2 dielectric which typically has higher trap densities than thermally-grown SiO_2 [35–37]. Thus, shorter pulses are needed to achieve ΔV_T values comparable to those of the other types of devices. At $t_{on} = 1\ \mu s$, we have $\Delta V_T \sim 0.075$ V, corresponding to a ~99% reduction of hysteresis and an active charge trap density of ~3.7×10^{11} cm^{-2}. For an EOT of 1 nm, the equivalent hysteresis would be just ~17.1 mV. Thus, we demonstrate the elimination of hysteresis even for devices which suffer from higher trap densities (here due to the transfer process and the use of HfO_2 dielectric), proving the effectiveness of our measurement technique.

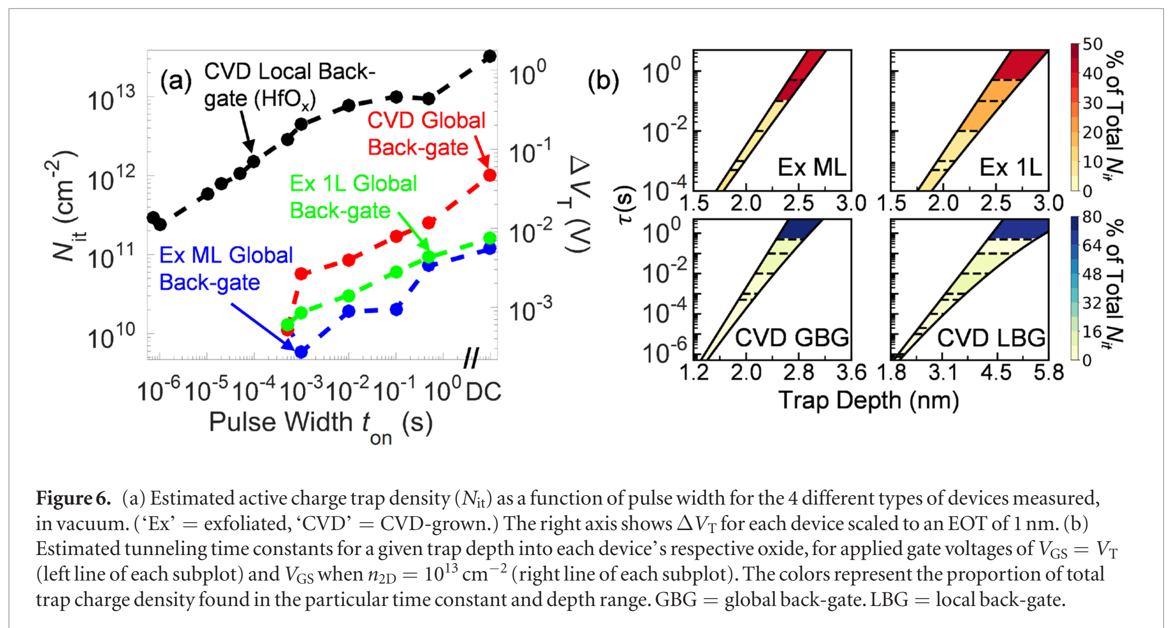

Figure 6. (a) Estimated active charge trap density (N_{it}) as a function of pulse width for the 4 different types of devices measured, in vacuum. ('Ex' = exfoliated, 'CVD' = CVD-grown.) The right axis shows ΔV_T for each device scaled to an EOT of 1 nm. (b) Estimated tunneling time constants for a given trap depth into each device's respective oxide, for applied gate voltages of $V_{GS} = V_T$ (left line of each subplot) and V_{GS} when $n_{2D} = 10^{13}$ cm^{-2} (right line of each subplot). The colors represent the proportion of total trap charge density found in the particular time constant and depth range. GBG = global back-gate. LBG = local back-gate.

We also extract μ_{FE} versus t_{on} as shown in figure 5(c). Once again, as the t_{on} is shortened, the mobility converges to a single value between the forward and reverse sweeps. As we use a wider t_{on} range for this device than for others, a clear trend of increasing μ_{FE} with decreasing t_{on} (particularly below 0.1 s) emerges. This trend could be the result of two competing phenomena affecting mobility: A transition from hopping transport to band transport (at shorter t_{on}), which increases mobility [4], and an increase in Coulomb scattering due to donor-like trap centers remaining positively charged during pulsed I_D–V_{GS} measurements (i.e. not capturing electrons), which decreases mobility [2, 38, 39]. For this device, it appears that a transition from hopping to band transport (with decreasing t_{on}) dominates. Perhaps more importantly, in such devices with larger hysteresis, the field-effect mobility can be significantly under- or overestimated (by as much as 50%) if only the forward or reverse DC sweep is used, also revealed in figure 5(c).

3. Comparison of devices

We now compare each device type to better understand the effects of the MoS_2 thickness, growth method and gate dielectric on charge trapping, all comparisons being for the measurements performed in vacuum after the anneal step. Figure 6(a) compares the estimated active charge trap density (N_{it}) as a function of pulse width t_{on} with t_{off} = 500 ms for all device types measured.

First, we compare the exfoliated devices, which all had 90 nm SiO_2/Si back-gates in common, but different contact metals (Au for 1L, Ni for ML). The different contact metals may account for the negative V_T shift of ~10 V for the 1L device due to different Schottky barrier heights and contact resistances, as shown in other studies [40, 41]. Because our measurements used pulsed V_{GS} with constant V_{DS} (not pulsed) and effectively eliminated hysteresis, we do not expect that the contacts play a large role in hysteresis, consistent with conclusions of the length-dependent measurements in figure 4(b). Despite this V_T difference, figure 6(a) shows that N_{it} is only marginally higher for 1L than ML exfoliated MoS_2 FETs, at all pulse widths. The 1L of MoS_2 may be more strongly influenced by surface charge traps, causing additional hysteresis [14, 42], although other studies contradict this by claiming that intrinsic charge traps between MoS_2 layers (within the ML devices) should be more influential [27, 29]. A further study comparing devices with several different MoS_2 thicknesses is necessary to draw conclusions about the relationship between hysteresis and MoS_2 thickness.

Next, we compare the local back-gated (LBG) and the global back-gated (GBG) CVD-grown MoS_2 devices. Here, the MoS_2 growth conditions and device contacts are the same, but the gate dielectrics are different (18 nm HfO_2 for LBG, 30 nm SiO_2 for GBG) and the LBG device fabrication included a MoS_2 transfer step. Figure 6(a) reveals that the LBG device has much larger N_{it} than the GBG device for all pulse widths. The contributing factors to this difference are the HfO_2 dielectric, which has an intrinsically higher trap density than SiO_2 (see section 2.4), and the imperfect MoS_2 transfer process (see supplementary section II), which can introduce defects and contaminants.

Finally, we can gain insight into the depths of active charge traps in our gate dielectric and the extent traps at those depths affect output characteristics by using a tunneling front model [43] (see supplementary section IV). Using these calculations, we obtain figure 6(b), which shows the tunneling time constants as a function of trap depth for two different biasing points. For each subplot, the left line is calculated for $V_{GS} = V_T$, and the right line is calculated for the V_{GS} corresponding to $n_{2D} = 10^{13}$ cm^{-2}. The bias range reflects the voltages we typically apply to our

devices and allows us to determine expected charge trap depths. We see from the exfoliated and GBG CVD devices that the average trap depths range from ~1.8 nm to ~2.5 nm for time constants between 500 μs and 500 ms, respectively. However, the trap depths for the LBG CVD devices (on HfO_2) may reach as deep as ~5 nm at high bias and time constants of 500 ms. This difference is due to a larger electron affinity and smaller effective tunneling mass for HfO_2 than SiO_2.

The shaded regions in figure 6(b) illustrate the percentage of total trap charge density found in a particular time constant range. There are notable differences between the exfoliated devices and CVD devices. For the CVD devices, we see that between 64%–80% of the total trap density has a time constant greater than 500 ms, meaning pulse widths of 500 ms would be sufficient to eliminate a majority of the hysteresis. In contrast, only between 40% and 50% of the total trap density has a time constant greater than 500 ms in the exfoliated devices. This distinction suggests that the MoS_2 growth method and device fabrication process (including the high-temperature sulfur-rich ambient that the SiO_2 is exposed to during CVD growth) strongly influence the percentage of total trap density found in different trap time constant ranges. Nevertheless, we note that extremely stable and low-hysteresis CVD-grown devices have been recently reported after a high-quality Al_2O_3 encapsulation step [18].

4. Conclusions

In this work, we have developed a simple pulsed measurement technique to reduce hysteresis in MoS_2 transistors by applying gate voltage pulses shorter than the time constants of trapped charge. We fabricate different types of MoS_2 devices (exfoliated and CVD-grown, as well as monolayer and multi-layer on different gate dielectrics) and measure I_D–V_{GS} curves using both DC and pulsed measurements to compare hysteresis and charge trapping. The pulse widths necessary to eliminate hysteresis range from 1 μs to 1 ms, depending on the type of device. We demonstrate that our measurement technique successfully reduces hysteresis even for the most hysteretic devices, which in our case are transferred MoS_2 devices with HfO_2 as the gate dielectric. Though there is variability among the different devices with SiO_2 as the dielectric, we demonstrate a reduction in active charge trap density to $<1.4 \times 10^{10}$ cm^{-2} across devices when $t_{on} = 500$ μs. We also show that while hysteresis in DC measurements hinders an accurate extraction of field-effect mobility, pulsed measurements allow extraction of the 'true' mobility of MoS_2, which converges to a single value regardless of the voltage sweep direction. Conversely, we caution that estimating device mobility from hysteretic measurements could lead to errors as large as ~50%, potentially explaining some of the wide range of MoS_2 mobilities reported in the literature. Finally, we use a tunneling front model to quantify the depths of active charge traps in our gate dielectrics. The reproducible pulsed measurement technique demonstrated here can also be used to study the intrinsic properties of other low-dimensional and emerging devices which suffer from charge-trapping phenomena.

5. Methods

We measure DC and pulsed transfer characteristics with the Keithley 4200-SCS and 4225-PMU using the Keithley interactive test environment (KITE) software. While specialized, impedance-matched test structures and equipment are generally used for high-speed measurements [44], we find that such precautions are not needed if specific measurement guidelines are followed, greatly simplifying the set-up. Our guidelines are as follows.

First, we measure DC transfer curves to identify the non-negligible hysteresis. Next, we switch our instrumentation to pulse-measure units (PMUs) for pulsed measurements. After enabling the waveform capture test mode for a transient measurement, we set the timing parameters. Since each typical DC sample takes >250 ms to acquire, we use a pulse width $t_{on} \leqslant 250$ ms to reduce hysteresis. In some cases, we find that $t_{on} > 250$ ms can also reduce hysteresis because of charge de-trapping during the off time, t_{off} (see figure 1(e)). Additionally, we keep our rise and fall times (t_R and t_F respectively) $<0.1t_{on}$. For each PMU, we set the current range to the smallest value greater than the peak DC currents to ensure proper measurement range, resolution, and timing. As a result, the noise floor is increased during pulsed measurements. To test the worst-case cable, chuck, and pad capacitive charging scenario, we set the gate bias to the maximum V_{GS} applied in our DC measurements. As seen in figure 1(f), immediately after the rise of the pulse, there is a decay in current caused by a combination of parasitic capacitances and trapped charges. Since I_D–V_{GS} sweeps with PMUs report spot means of current during the 75%–90% section of the pulse [45] (red region in figure 1(f)), if that portion of the transient appears to overlap with charging currents from parasitics, we select a larger t_{on}. Otherwise, if the parasitics do not interfere with the sampling region, we measure pulsed I_D–V_{GS} sweeps with the present timing parameters. This process is repeated with smaller t_{on} until hysteresis is eliminated.

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Notes

The authors declare no competing financial interests.

Supplementary information

Raman and photoluminescence (PL) of monolayer exfoliated MoS_2, the MoS_2 transfer process onto the local back-gates with HfO_2, transfer curves of devices from CVD-grown MoS_2 on local back-gates, and a description of the tunneling front model.

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Supplementary Information

Reduction of Hysteresis in MoS_2 Transistors Using Pulsed Voltage Measurements

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I. Raman and photoluminescence (PL) of monolayer (1L) exfoliated MoS_2

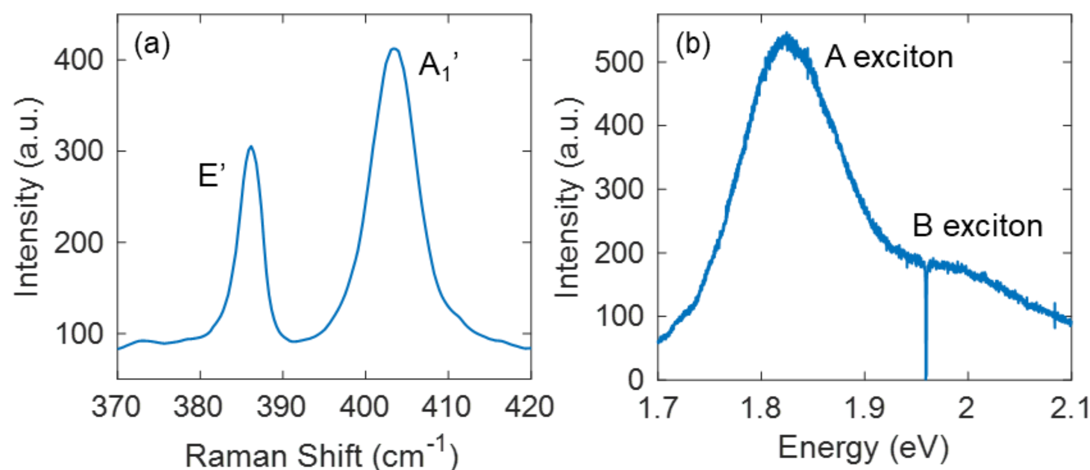

Figure S1. (a) Raman and (b) photoluminescence (PL) spectrum of the 1L exfoliated MoS_2 flake. The A exciton in the PL spectrum corresponds to the energy of the optical band gap of 1L MoS_2.

II. MoS_2 transfer process onto local back-gates

The process for transferring MoS_2 from the growth substrate onto local back-gates is as follows, similar to Ref. [1]:

1. Drop-cast PMMA A4 onto the growth substrate
2. Bake on a hot plate at 150 °C for 10 minutes
3. Place the chip in a glass petri dish with 1 M NaOH (aq.) solution heated to 80 °C
4. The NaOH will dissolve the SiO_2, causing the growth substrate to sink and the PMMA/MoS_2 to float on the surface
5. Use tweezers to transfer the PMMA/MoS_2 to a bath of deionized water and let it float on the surface for 30 minutes
6. Use tweezers to transfer the PMMA/MoS_2 to the HfO_2/Au local-back gated substrates
7. Point an N_2 gun directly on the PMMA to push out as much water as possible from beneath the PMMA/MoS_2
8. Place the new substrate on a room temperature hot plate and ramp up to 150 °C during a 20 minute time period
9. Soak in acetone for an hour to remove the PMMA
10. Perform a final rinse with methanol and dry with an N_2 gun

III. Transfer curves of local back-gated CVD MoS_2 devices

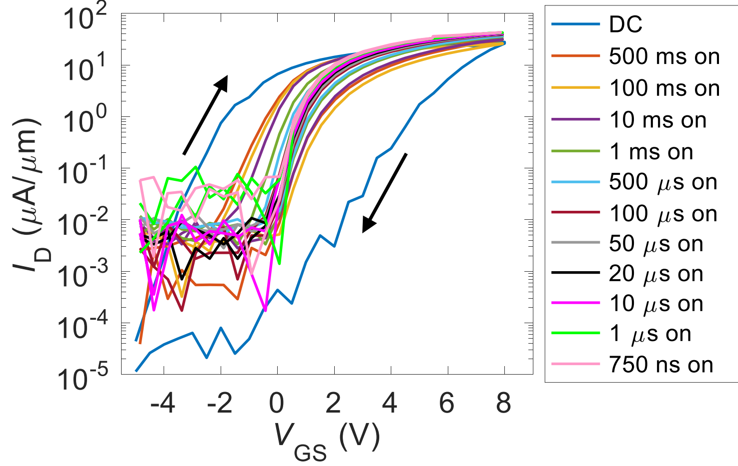

Figure S2. Extended version of Figure 5a showing transfer curves of the CVD-grown MoS_2 device with a local back-gate, including measurements at DC and all t_{on} pulses (500 ms, 100 ms, 10 ms, 1 ms, 500 µs, 100 µs, 50 µs, 20 µs, 10 µs, 1 µs, and 750 ns).

IV. Tunneling Front Model

The tunneling front model calculates the trap time constant as a function of depth, x, and is given by:

$$\tau(x) = \tau_0 \exp\left(2\int_0^x K(x')dx' \right)$$

where $\tau_{0,SiO_2} \approx 6.6\times10^{-14}$ s [2] and $\tau_{0,HfO_2} \approx 1\times10^{-11}$ s [3] are characteristic time constants for SiO_2 and HfO_2 respectively, and $K(x)$ is the effective barrier in the oxide. The barrier height can be written as $K(x) = \sqrt{2m_{ox}(\Phi_B - E(x))}/\eta$ where $\Phi_B = \chi_{MoS_2} - \chi_{ox}$ and $E(x) = qFx$ with F as the applied field and q as the electron charge. To extract barrier heights, we used $\chi_{MoS_2} = 4.4$ eV for multi-layer MoS_2, $\chi_{MoS_2} = 4.25$ eV for monolayer MoS_2 [4], $\chi_{SiO_2} = 0.95$ eV [5], and $\chi_{HfO_2} = 2.65$ eV [6]. The tunneling effective masses were $m_{SiO_2} = 0.42\,m_0$ [5] and $m_{HfO_2} = 0.2\,m_0$ [6] with m_0 as the electron mass. Lastly, the field, F, is given by $F = V_{ox}/t_{ox}$ where V_{ox} is calculated numerically with the transcendental equation from [7]:

$$V_{GS} = V_0 + V_{th} \ln\left[\exp\left(\frac{n_{ch}}{g_{2D}k_B T} \right) - 1 \right] + V_{ox}$$

where $V_0 = E_g/(2q)$, E_g is band gap energy, $V_{th} = k_B T / q$, n_{ch} is the electron density in the channel, k_B is the Boltzmann constant, T = 298 K, and $V_{ox} = qn_{ch} / C_{ox}$. The two-dimensional density of states is defined in [7] as $g_{2D} = g_s g_v m^* / 2\pi\hbar^2$ where $g_s = 2$ is the spin degeneracy and $g_v = 2$ is the valley degeneracy [8].

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