

# Memory Technology: Putting the “nano” in your iPod

**Eric Pop**

Dept. of Electrical & Computer Engineering  
<http://poplab.ece.uiuc.edu>



## Applications of Memory

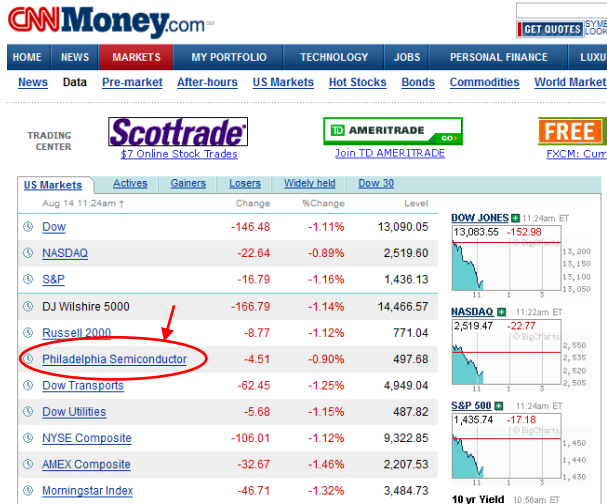
- 1 Gigabyte = 1 GB = 1 billion bytes  $\approx 1024^3$  bytes (!)
- 1 byte = 8 bits (1/0 state)
- 1 Human genome  $\approx 0.8$  GB
- 1 DVD  $\approx 4.7$  GB
- 1 iPod nano = 4 or 8 GB of Flash memory
- 1 laptop  $\approx 2$  GB DRAM memory



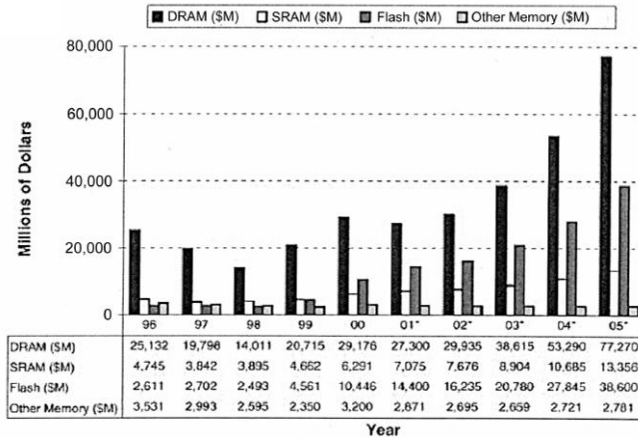
Google™



# This Is Science, Technology, and Business



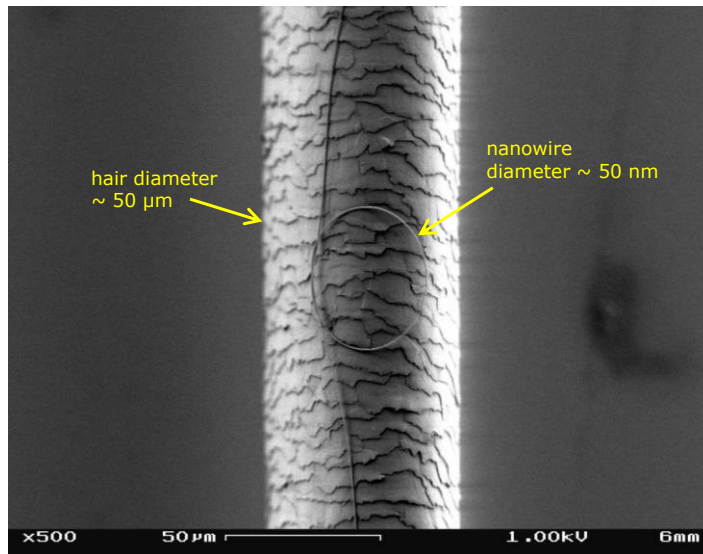
# Giga-Bytes and Giga-Dollars



Over the same period, memory market accounted for 25-35% of total semiconductor market. PS: **cost matters!!!**



## The Size of a Nanowire

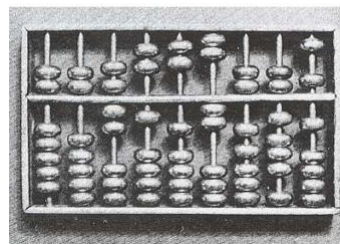


Source: L. Tong, <http://www.nsf.gov/od/lpa/news/03/pr03147.htm>

## The Abacus, Ancient *Digital* Memory



Roman Abacus (ca. 200BC)



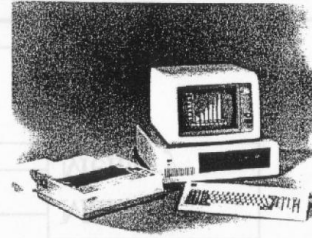
Chinese Abacus (ca. 190AD)

- Information represented in digital form
- Each rod is a decimal digit (units, tens, etc.)
- Finite number of states for each bead
- A bead in the abacus is a memory device, not a logic gate

Sources: R. Cavin (SRC), Wikipedia

## More on Ancient History

### First PC



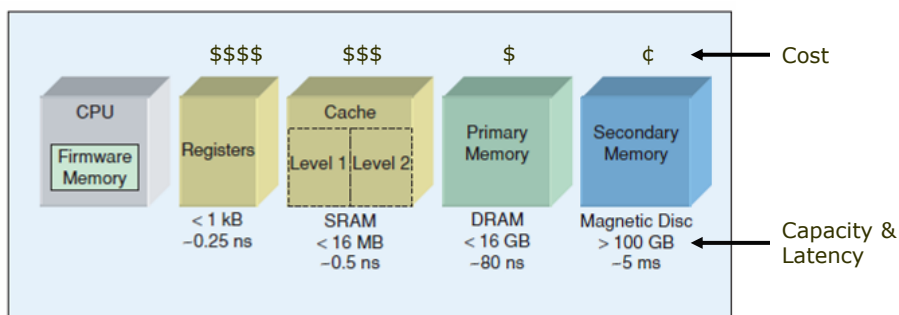
- IBM 5150 PC Stock Specifications

- System Unit w/84-Key Keyboard
- 8088 processor running at 4.77mhz (209ns) 8 bit data bus
- 0,1 or twin Full-Height 160k Floppy Drives (Depending on model)
- 64-256k RAM (Depending on model)

- Memory had no problem keeping up with 209ns processor

Source: C. Webb, IEDM 2001

## Memory in a Modern Computer

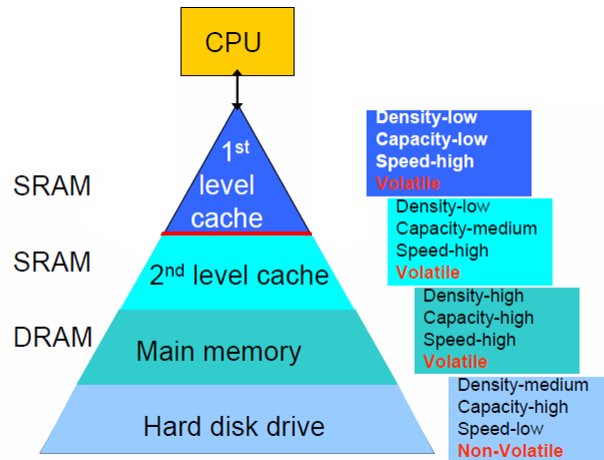


Source: Brewer, *IEEE Circuits and Devices Mag.*, Apr. 2005

### Modern CPU:

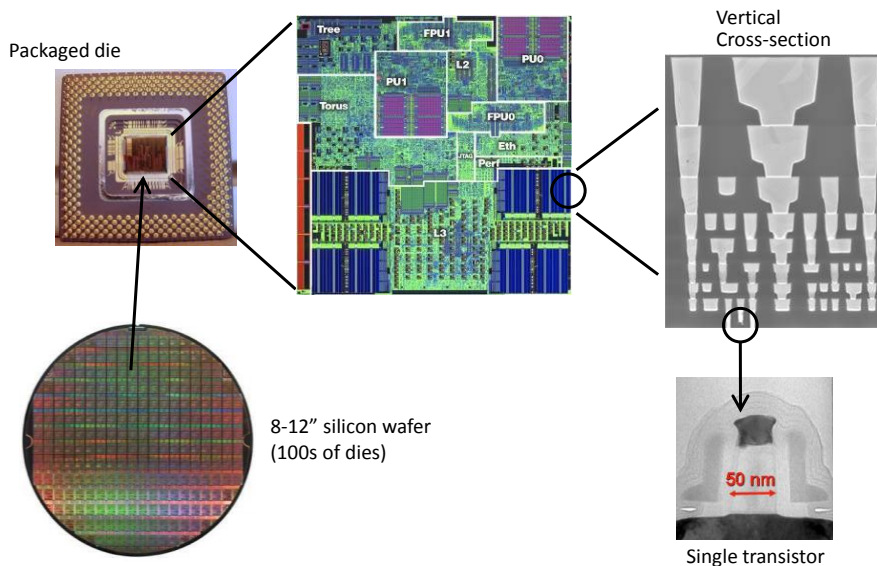
- Operate at GHz (nanosecond access times)
- Modern memory vary from ~1 ns access times (SRAM) to 1 ms access times (hard disk)

# Another Look at the Memory Hierarchy

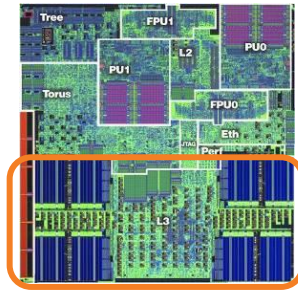


Source: R. Cavin (SRC)

# From Silicon to Bits



# On-Chip SRAM Cache Memory

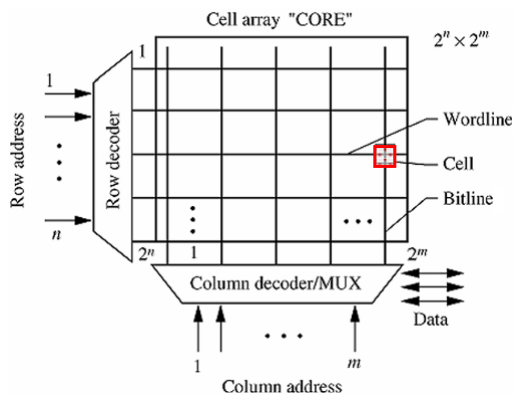


**Lots of SRAM cache  
(static random-access memory)**

# Managing Billions of Bits

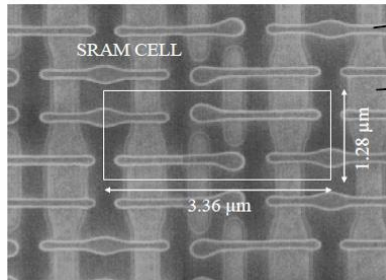
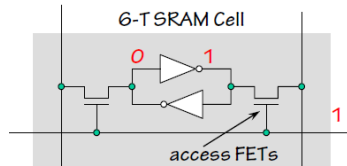
## Memory:

- Volatile vs. Non-volatile (charge stored when power is off)
- Read-only vs. Read-write
- Charge based vs. ???
- Fast vs. Slow
- Large bit vs. Small bit area
- Cheap vs. Expensive



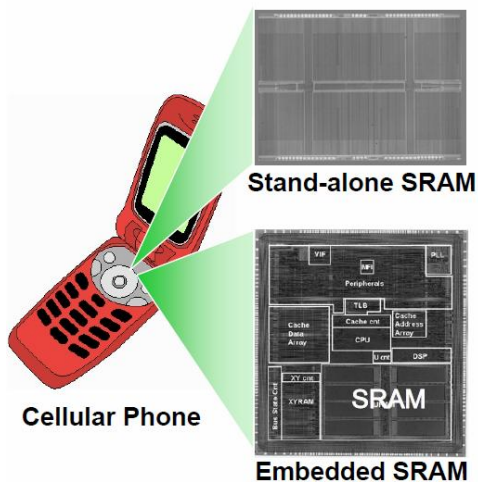
Source: Stanford EE313 Notes  
<http://www.stanford.edu/class/ee313/>

## SRAM = Fastest, Largest, Volatile (6T)



- Two inverters in series ("stuck" in either 1 or 0 stable states) + two access transistors
- Six transistors total (6T)
- Volatile! Bit state (0/1) maintained only while power is ON
- Constant leakage current must be replenished → power dissipation ( $\sim 10 \mu\text{A}$  standby for 1 Mb cell array)
- 6T SRAM is **BIG**:  $\sim 100 \text{ F}^2$
- Fast:  $< 1 \text{ ns}$  access time!

## SRAM = Fastest, Largest, Volatile (6T)

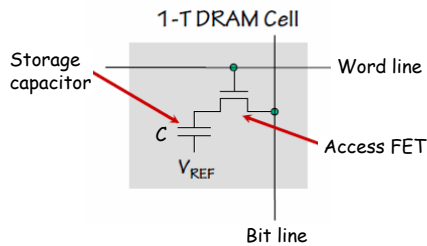


Almost all SRAM is embedded within micro-processors these days (why?)

- Fast:  $< 1 \text{ ns}$  access time!

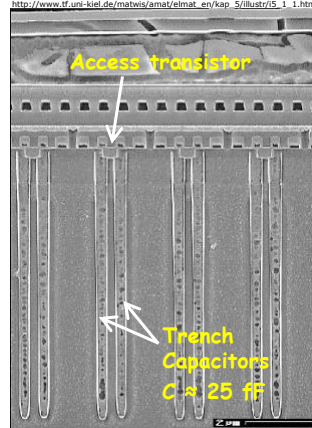


# DRAM = Fast, Small, Volatile (1T-1C)



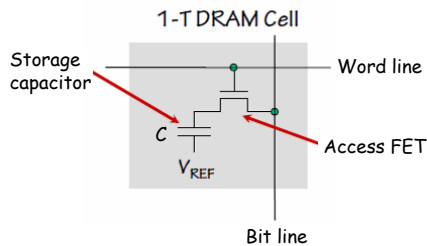
- Bit 1/0: Charge stored on capacitor
- Access ( $\sim 10$  ns) with one transistor
- "1T-1C" configuration
- Read is destructive: charge spills out of capacitor, must be recharged
- Refresh charge every 64 msec

64 Mbit DRAM from 1996



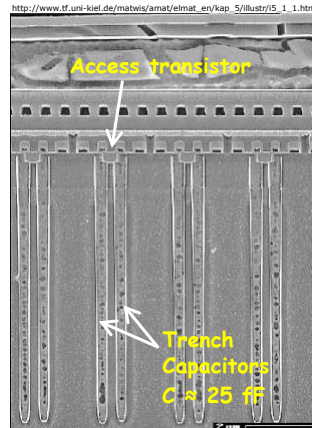
Area: 8-10 F<sup>2</sup>

# DRAM = Fast, Small, Volatile (1T-1C)



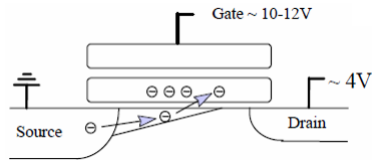
Trivia: DRAM capacitance cannot be miniaturized further due to cosmic ray damage!

64 Mbit DRAM from 1996

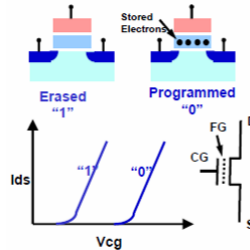


Area: 8-10 F<sup>2</sup>

# FLASH = Slow, Small, Non-Volatile (1T)



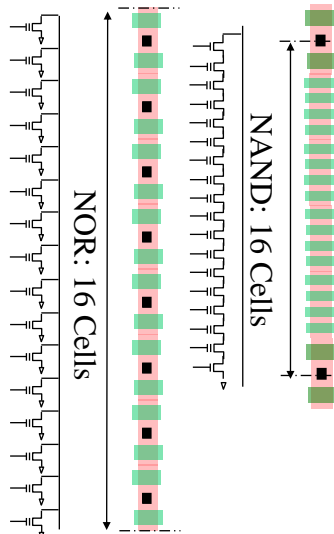
**NOR:** "Lucky" electron programming  
Drain current  $\sim 50 \mu\text{A}$



- Charge stored by "tunneling" within single transistor (1T)  
*(yes, this is quantum mechanics storing the Maroon 5 song bits on your iPod nano)*
- Non-volatile, but relatively slow ( $\sim 100 \text{ ns} - 1 \mu\text{s}$ )
- A single bit  $\sim 100$  stored electrons today (2008)
- Very, very hard to make this smaller, or charge will leak out!

# Flash Layout: NOR vs. NAND

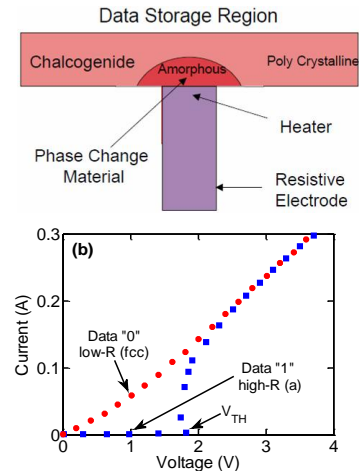
- How do you get more speed out of Flash?
- Data access speed also depends on the bit (cell) layout
- "NOR" layout is faster but 2x larger (less dense)  $\rightarrow$  used in cell phones, code storage
- "NAND" layout is slower but denser  $\rightarrow$  used for data storage (iPod nano, USB drives, etc.)
- NOR read  $\sim 10\text{s of ns}$
- NAND read  $\sim 1 \mu\text{s}$



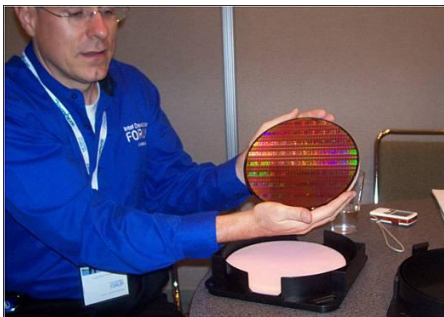
Source: Al Fazio, Intel

## Phase-Change = Fast, Small, Non-Volatile

- Can we store memory without storing electron charge?
- Think about CD/DVDs, magnetic hard drives, even vinyl records
- DVDs: "phase-change material" layer changes from crystalline to amorphous when heated by laser beam
- Same material (GeSbTe) may be used for very small and fast electrical memory
- 10 ns access time, very small footprint



## Intel, Samsung, UIUC Hard at Work...



### DATA STORAGE NEWS

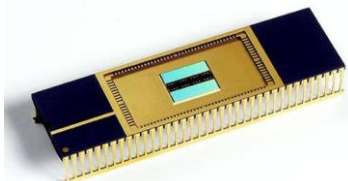
16 April 2007

#### Intel set for first public demo of PRAM

By Sumner Lemon, IDG news service

Intel's chief technology officer Justin Rattner is set to give the first public demonstration of the company's PRAM (phase-change RAM) technology at this week's Intel Developer Forum (IDF) conference.

**Put in perspective:  
NAND Flash chips of  
8+ Gb in production**



"Samsung completed the first working prototype of what is expected to be the main memory device to replace high density Flash in the next decade – a Phase-change Random Access Memory (PRAM). The company unveiled the 512 Mb device at its sixth annual press conference in Seoul today." (September 2006)

Questions?