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ARTICLE OPEN

Thermal transport in layer-by-layer assembled polycrystalline graphene films

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New technologies are emerging which allow us to manipulate and assemble 2-dimensional (2D) building blocks, such as graphene, into synthetic van der Waals (vdW) solids. Assembly of such vdW solids has enabled novel electronic devices and could lead to control over anisotropic thermal properties through tuning of inter-layer coupling and phonon scattering. Here we report the systematic control of heat flow in graphene-based vdW solids assembled in a layer-by-layer (LBL) fashion. In-plane thermal measurements (between 100 K and 400 K) reveal substrate and grain boundary scattering limit thermal transport in vdW solids composed of one to four transferred layers of graphene grown by chemical vapor deposition (CVD). Such films have room temperature in-plane thermal conductivity of ~400 $Wm^{-1} K^{-1}$. Cross-plane thermal conductance approaches 15 $MWm^{-2} K^{-1}$ for graphene-based vdW solids composed of seven layers of graphene films grown by CVD, likely limited by rotational mismatch between layers and trapped particulates remnant from graphene transfer processes. Our results provide fundamental insight into the in-plane and cross-plane heat carrying properties of substrate-supported synthetic vdW solids, with important implications for emerging devices made from artificially stacked 2D materials.

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INTRODUCTION

The past decade of graphene research has accelerated scientific discovery of 2D transition metal dichalcogenides,[1,2] phosphorene,[3] silicene,[4] and 2D hexagonal boron nitride.[5] These materials have unique electrical, thermal, optical, and mechanical properties as compared to their 3-dimensional (3D) counterparts. Electrically, such 2D building blocks exhibit metallic, semiconducting, and insulating behavior, providing novel material combinations for electronic device design.[1,6] For example, LBL assembly of graphene with other 2D materials has resulted in ultrathin heterostructures suitable for tunneling field effect transistors[7–9] and ultrathin optoelectronic devices.[10,11] However, the thermal properties of LBL assembled artificial vdW solids have received less attention. Similar to naturally occurring vdW solids, artificial vdW solids are expected to have strong in-plane bonds and weak inter-layer vdW interactions, resulting in anisotropic thermal properties between the in-plane and cross-plane directions.[12–14]

In this work, we use a combination of suspended-bridge electrical thermometry and time-domain thermoreflectance (TDTR) to probe heat flow in LBL assembled graphene-based vdW solids. We pay particular attention to the role of external influences on thermal transport in such films, e.g., grain size and the role of the substrate. We find the in-plane thermal conductivity ($k_{||}$) of our substrate-supported CVD-grown polycrystalline graphene is approximately equal to that of substrate-supported *exfoliated* graphene[15] at low temperatures (≈120 $Wm^{-1} K^{-1}$ at 100 K). The $k_{||}$ peaks at around room temperature between 300 and 400 $Wm^{-1} K^{-1}$, depending on the grain size (L_g), but independent of the number of transferred graphene films grown by CVD which we denote as *N*. Importantly, we find the $k_{||}$ of substrate-supported polycrystalline graphene with L_g ~140 nm is approximately 70% of substrate-supported exfoliated graphene, consistent with our previous theoretical study.[16] This is an order of magnitude less than freely suspended graphene (2000–4000 $Wm^{-1} K^{-1}$),[13,14,17–19] and consistent with previous electrical thermometry[15] and Raman thermometry[20] measurements of SiO_2-supported graphene. Our results highlight the important roles that substrate and grain boundary scattering play for in-plane thermal transport properties of ultra-thin LBL assembled graphene vdW solids ($N = 1–4$).

We also probe the cross-plane thermal conductance ($G_\perp$) of LBL assembled graphene vdW solids and find that it is consistently below that of A-B stacked few-layer graphene. These findings present data for the grain size effect on in-plane thermal transport,

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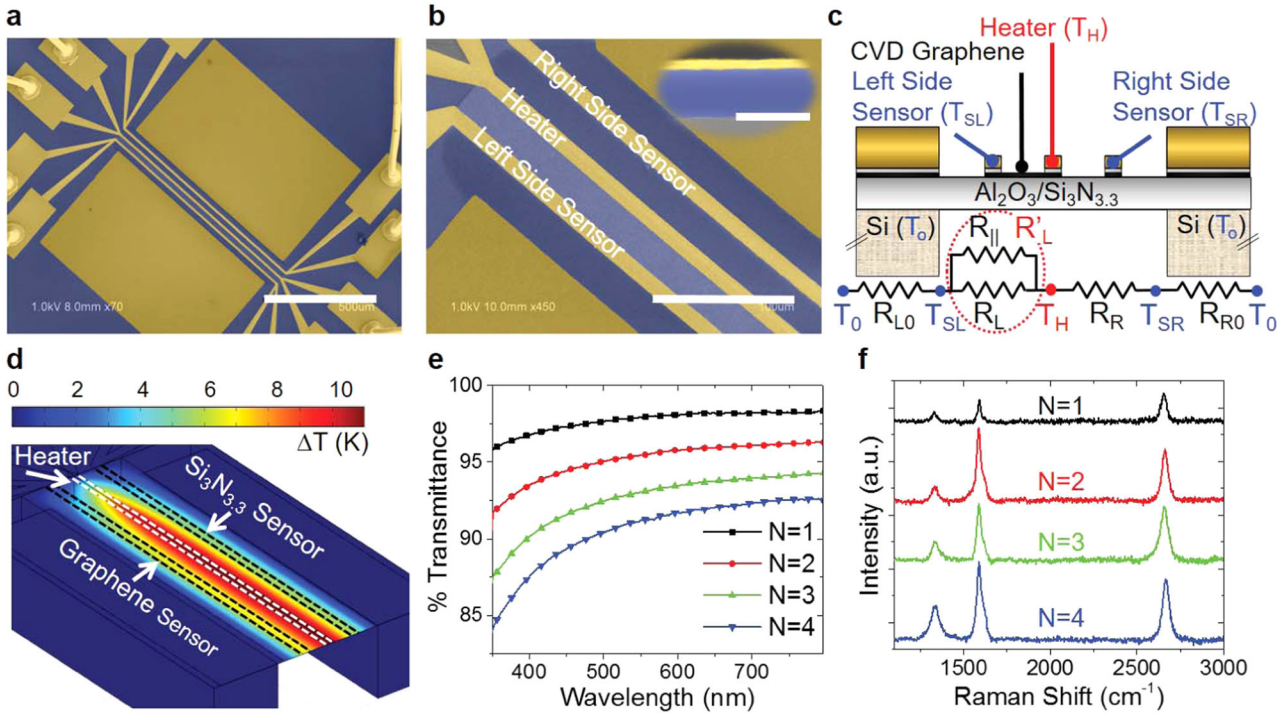

Fig. 1 In-plane thermal measurement platform and graphene characterization. **a** SEM image of differential electrical thermometry platform showing wire bonds for electrical access to heater and sensors. Scale bar is 500 μm. **b** Higher magnification SEM image showing suspended region of the platform with graphene patterned between the center heater and left sensor. Scale bar is 100 μm. The inset shows a cross-section SEM image of the membrane thickness (purple color) capped by a thin metal layer (gold color). Scale bar is 300 nm. **c** Schematic of suspended thermometry platform. The thermal circuit is shown below. The left side sensor measures the heat flow through the graphene side of the sample while the right side sensor measures the heat flow through the right side silicon nitride membrane. **d** Temperature distribution in a 3D finite element simulation of the experimental test structure with a single transferred layer of polycrystalline graphene and power applied to the center heater. **e**, **f** Transmittance and Raman characteristics of layer-by-layer assembled graphene films

as well as data probing cross-plane thermal transport in polycrystalline LBL assembled graphene vdW solids supported by dielectric substrates. Our results are highly relevant for future LBL assembled devices and interconnects, highlighting an approach which may be used to tune the heat flow properties of LBL assembled 2D heterostructures.

RESULTS

In-plane thermal measurements

Figure 1a-c shows scanning electron microcroscopy (SEM) images and a schematic cross-section of the suspended thermometry bridges used in this study. The layered graphene samples are supported by a thin silicon nitride bridge to provide thermal isolation and mechanical robustness. X-ray photoelectron spectroscopy reveals a $Si_3N_{3.3}$ stochiometry of the supporting bridges (Supplementary Information) and their thickness varies between 150 and 300 nm depending on the fabrication run (measured by ellipsometry and compared to cross-sectional SEM, inset of Fig. 1b). Polycrystalline graphene is grown on copper foils purchased from Alfa Aesar (CAS 7440-50-8) and then transferred to the $Si_3N_{3.3}$, (initially supported on Si) through a wet-transfer process using a polymer scaffold.[21–24] The polymer is removed in organic solvents followed by annealing in Ar/H_2 to remove residual contaminants (see Methods). For samples with more than a single transferred layer of CVD graphene the wet-transfer and anneal process is repeated in a LBL fashion to achieve artificial graphene vdW solids with up to $N = 4$ CVD layers. Metal heater and sensor strips are then patterned on top by photolithography, separated from the graphene by a thin evaporated SiO_2 layer which serves as electrical insulation (see Methods and Supplement). The wafer is back-etched to suspend the supporting $Si_3N_{3.3}$ membrane (Fig. 1c). Our device yield is enhanced by utilizing a thin Al_2O_3 layer as a through-wafer etch stop for the BOSCH 2 process. The contrast of the graphene and the suspended region of the membrane are easily distinguishable in the final test structure (Fig. 1b).

We use optical transmittance measurements and Raman spectroscopy to characterize the assembled graphene stacks. We find the optical transmittance at 550 nm decreases by ~2.8% with each new layer, in good agreement with previous work (Fig. 1e).[25] Raman analysis of LBL assembled graphene stacks shows a decreasing intensity ratio of 2D-peak to G-peak (I_{2D}/I_G), and increasing D-peak intensity with increasing transfers (Fig. 1f). From the D-peak in the Raman spectra we can estimate the grain size of a single transferred graphene film ($N = 1$) as L_g (nm) $= 2 \times 10^{-10}$ $\lambda^4 (I_D/I_G)^{-1}$, where λ is the excitation laser wavelength and (I_D/I_G) is the D-peak to G-peak integrated intensity ratio.[26,27] The CVD graphene used in the LBL assembly of graphene vdW solids has an average grain size of $L_g \sim 140 \pm 80$ nm (Supplementary Information). We note this is not necessarily a crystallite size defined by the distance between graphene grain boundaries, but rather the distance between Raman-active defects, including graphene wrinkles,[28] grain boundaries,[29] transitions between single layer to bilayer thickness,[30] and regions of polymer residue.[31] Our measured L_g is also in good agreement with previous scanning transmission electron microscopy (STEM) imaging of polycrystalline graphene films grown by random nucleation using CVD on copper foils.[32]

Electrical thermometry measurements proceed as follows. A heating power (~5 to 175 μW) is passed through the heater

electrode, while the temperature is sensed by monitoring calibrated changes in the electrical resistance of the heater and two sensors. One side of the measurement platform provides the total in-plane thermal conductance (G_L') of the graphene and silicon nitride film, while the other measures only the supporting silicon nitride film (G_R) (Fig. 1c and Fig. S9). The in-plane thermal conductance of the graphene layer(s) ($G_{||}$) is thus obtained by subtraction. Heat flow measurements are performed from 100 to 400 K under vacuum (~10^{-5} Torr) where heat loss due to convection is neglible. The maximum heat loss due to radiation is $Q_{rad} \approx$ 1% at 400 K, where $Q_{rad} = \sigma\epsilon A_s(T^4 - T_0^4)$. Here, σ is the Stefan-Boltzmann constant, ϵ is the membrane emmissivity (assumed to be 1 to provide an upper bound), A_s is the area of the suspended membrane, T_0 is the background temperature, and T is the average temperature of the suspended membrane. We do not notice a significant temperature hysteresis in our measurements with increasing and decreasing ambient temperature sweeps. In addition, we have also compared a single transferred layer of CVD graphene to LBL assembled stacks of CVD graphene, and to non-equilibrium Green's function (NEGF) calculations,[16] in order to elucidate the role of the supporting substrate and that of graphene grain boundaries on the films' thermal properties.

Similar to previous work from our group, we use a commercial software package (COMSOL Multiphysics) to extract the thermal properties of graphene from the electrical thermometry data.[33,34] Figure 1d shows our optimized 3D finite element method (FEM) model of the suspended thermometry platform and a typical extracted steady-state temperature profile when a graphene film is placed on one side of the platform (also see Supplementary Information). The simulation is performed using isothermal boundary conditions at the bottom and side surfaces of the platform (i.e., at the Si heat sink), while the symmetry plane and the surfaces of the supporting membrane, electrodes, and graphene are given adiabatic boundary conditions. Importantly, the 3D simulations include thermal contact resistance effects of all interfaces[33] (Supplementary Information), although these have a minimal effect on the extracted values of $k_{||}$. A constant power is applied to the center heater electrode, consistent with the Joule heating (P_H) induced in the measurements, and the structure is allowed to come to steady state. We then fit the simulated temperature rises in the heater and two sensors to the measured experimental data (ΔT_H, ΔT_{SL}, ΔT_{SR}), using the thermal conductivity of the membrane (k_{SiN}) and graphene ($k_{||}$) as fitting parameters. We find that although our suspended membrane geometry allows us to approximate 1-dimensional heat flow, approximately 10% of the heat flows in a 2D manner near the membrane edges. This is also in good agreement with our analytical model described below.

Analytically, the $k_{||}$ can be written as

$$k_{||} = G_{||}\frac{L_{HL}}{Wh_g}, \quad (1)$$

where $G_{||}$ is the thermal conductance of the graphene, L_{HL} is the distance between the heater and graphene-side sensor, W is the width of graphene, and h_g is the thickness of the graphene sample which is assumed to be 0.34 nm per transferred layer. This assumption provides an upper bound on the extracted thermal conductivity, and small thickness fluctuations (e.g., bilayer regions) are not expected to affect heat flow in otherwise continuous single layer graphene.[35] $G_{||}$ is calculated by subtracting the $Si_3N_{3.3}$ thermal conductance (G_L) from the combined thermal conductance of the $Si_3N_{3.3}$ and graphene (G_L') measured in our differential setup as follows:

$$G_{||} = G_L' - G_L = \frac{P_H(1-\alpha)\beta}{\Delta T_H - \Delta T_{SL}} - \frac{P_H\alpha\beta}{\Delta T_H - \Delta T_{SR}}\frac{L_{HR}}{L_{HL}} \quad (2)$$

Here, P_H is the heater power, α and β are dimensionless parameters which account for the asymmetry in heat flow perpendicular to the electrodes and heat loss parallel to the electrodes, respectively. ΔT_H, ΔT_{SL}, and ΔT_{SR}, are the measured temperature rises in the heater, graphene-side (left), and $Si_3N_{3.3}$-side (right) sensors, respectively. The distance between the heater and the $Si_3N_{3.3}$-side sensor is L_{HR}. We find the analytical model results are within 5% of the values obtained by the more computationally expensive FEM model (Fig. 2a, b, and Supplementary Figs. S10 and S11), highlighting the advantage of our differential electrical thermometry platform in simplifying the thermal analysis (see Supplementary Information for additional details of the analytical model).

We find the thermal conductivity of our $Si_3N_{3.3}$ films, deposited by plasma enhanced CVD is ~1.3 $Wm^{-1}K^{-1}$ at 300 K and exhibits excellent agreement with data from the literature over the full temperature range of our measurements (Supplementary Figs. S11 e-h), providing a good control on our methods. The extracted in-plane thermal conductance values for our $N = 1$ sample are shown in Fig. 2a. It is easily seen that the G_L' is significantly higher than G_L due to the addition of a single layer of CVD graphene. We find the $G_{||}$ of substrate-supported polycrystalline graphene films increases almost linearly with each additional layer added to the stack (Fig. 2b). When the $G_{||}$ of the LBL graphene vdW solids are converted to $k_{||}$ (Fig. 2c), however, we do not find a significant dependence on layer number up to $N = 4$, consistent with previous measurements on supported exfoliated few-layer graphene.[36]

We then compare single-layer graphene with different average grain sizes obtained arbitrarily from two different CVD growths in order to elucidate the role of line defects on thermal transport in substrate-supported graphene. In Fig. 2d, we plot the thermal conductivity of our two $N = 1$ CVD graphene samples (one with larger L_g is from Fig. 2c; the other with smaller L_g is from Supplementary Fig. S12) vs. their average grain sizes at different temperatures, as well as $k_{||}$ of monocrystalline exfoliated graphene (limited by the sample width ~2 μm).[15] It is shown that the thermal conductivity increases with increasing grain size, reaching ≈70% of the $k_{||}$ for substrate-supported monocrystalline exfoliated graphene and similar to that of bulk copper when $L_g \approx 140$ nm. Importantly, the measured dependence of $k_{||}$ (symbols) on the grain size shows good agreement with our NEGF calculations[16] for $k_{||}$ vs. L_g (Fig. 2d), where the calculated $k_{||}$ is the sum of the individual transverse (TA), longitudinal (LA), and flexural acoustic (ZA) phonon modes (Supplementary Fig. S12c). Furthermore, as shown in Supplementary Fig. S12d, the best fits to the experimental data of $k_{||}$ vs. T are obtained using grain sizes (L_g) of 140 and 60 nm, which are in excellent agreement with the grain sizes extracted by Raman spectroscopy (Supplementary Figs. S2 and S3).

Figure 2f shows a comparison of our data to the selected data from the literature. It illustrates the dominate role of the substrate scattering (Fig. 2e—left) in suppressing the thermal conductivity of substrate-supported graphene as compared to freely suspended graphene. Additional phonon scattering by graphene grain boundaries (Fig. 2e—right) can further reduce its thermal conductivity, and our data provide the temperature-dependent thermal conductivity for substrate-supported polycrystalline graphene. We notice that polycrystalline graphene with small domain sizes still greatly exceeds the thermal conductivity of narrow graphene nanoribbons,[33] suggesting such films may be a viable technology for flexible and transparent heat spreaders with potential applications in the field of transparent and flexible electronics.

Cross-plane thermal measurements

We now turn our attention to cross-plane heat flow in LBL assembled graphene vdW solids (Fig. 3). We assemble artificial graphene vdW solids with the number of transferred CVD

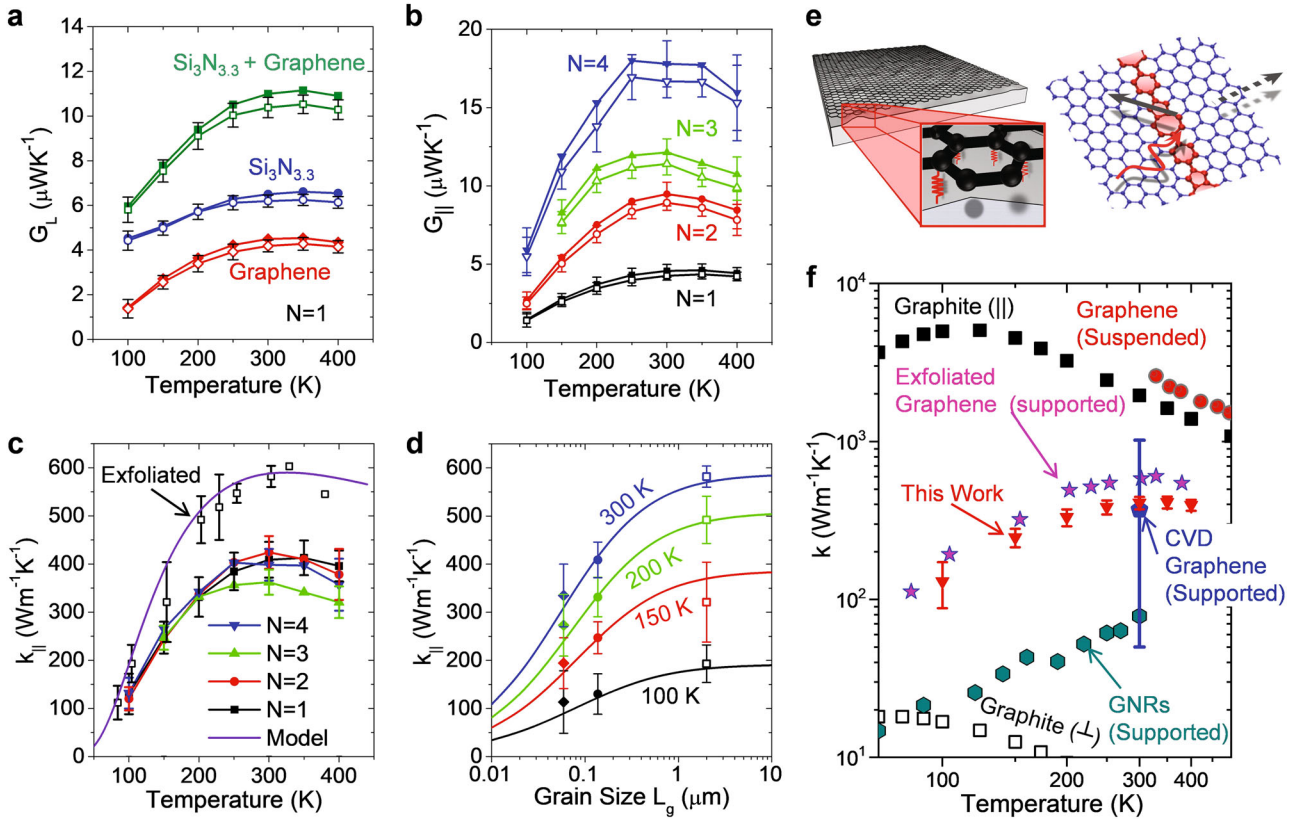

Fig. 2 In-plane thermal properties of layer-by-layer assembled graphene films. **a** Extracted thermal conductance of graphene and supporting silicon nitride membrane. **b** Thermal conductance of layer-by-layer assembled graphene films, adjusted to account for variations in sample length. In **a**, **b** solid-symbols are data extracted by 3D finite element modeling while open symbols are extracted using a simplified analytical model. **c** Calculated thermal conductivity from conductance in **b** compared to data for monocrystalline exfoliated graphene.[15] The solid line through the exfoliated data is our calibrated NEGF model[16] for monocrystalline graphene.[15] **d** Thermal conductivity of two $N = 1$ polycrystalline graphene samples with different average grain sizes of 60 ± 30 nm and 140 ± 80 nm by different growths (solid symbols) and data for exfoliated monocrystalline graphene (open squares),[15] showing clear grain size dependences at different temperatures. Solid lines are obtained from NEGF calculations and show excellent agreement with the experimental data. **e** Schematic representation of substrate dampening and grain boundary scattering of graphene phonons. **f** Comparison of our polycrystalline graphene thermal conductivity to previous reports of suspended graphene,[19] substrate-supported exfoliated graphene,[15] metal-supported CVD graphene,[43] graphene nanoribbons,[33] and natural graphite.[44] This work adds a "missing piece" to the literature highlighting the role of the substrate and grain boundary scattering in suppressing thermal conductivity in supported polycrystalline graphene over a wide temperature range. Error bars are the estimated experimental uncertainty (Supplementary Information)

graphene layers as $1 \le N \le 7$ on SiO_2 substrates (Fig. 3d). We then deposit ≈80 nm of Al by shadow-mask evaporation in an electron-beam evaporator, and measure $G_\perp$ of the Al/N layers of graphene/SiO_2 stack by TDTR, similar to previous work on exfoliated graphene samples.[37] Figure 3b shows TDTR results (symbols) and numerical solutions of our thermal model (solid lines) taking the measurements of the Al/SiO_2 interface as a reference. We find a reduction in $G_\perp$ with increasing layer number N. $G_\perp$ varies from ≈25 to 15 MWm^{-2}K^{-1} for $N = 1$–7 (Fig. 3c). These values are consistently below those of A-B stacked exfoliated samples and approach a factor of two reduction in $G_\perp$ as compared to exfoliated graphene samples[37] as N approaches 7 transfers.

Figures 3d–f show the schematic representation of our stacked layers, a cross-sectional bright field STEM (BF-STEM) image with trapped particulates indicated in the dark contrast regions, and a line profile of image intensity across the stack, respectively. The peak intensities in Fig. 3f illustrate the layered structure of our graphene stacks (Supplementary Fig. S13). High angle annular dark field STEM (HAADF-STEM) images and electron energy loss spectroscopy (EELS) analysis indicates the large trapped particulates are likely trapped copper particles, remnant from the etching and transfer process[38,39] (Supplementary Fig. S13).

DISCUSSION

These measurements highlight the importance of material processing techniques on the structure–property correlations of thermal transport in LBL assembled graphene vdW solids. Our electrical thermometry measurements reveal the $k_{||}$ of LBL assembled graphene vdW solids is independent of the number of transferred graphene layers, up to $N = 4$ transfers, with a value of ~400 Wm^{-1}K^{-1} at $T = 300$ K (Fig. 2c). Similar to mechanically exfoliated graphene supported by SiO_2 substrates,[15] we find the $k_{||}$ of polycrystalline graphene films grown by CVD is greatly reduced by the supporting $Si_3N_{3.3}$ substrates, due to suppression of the out-of-plane flexural mode (ZA) phonons. Residual polymer residue remnant from our microfabrication process could also contribute to scattering of ZA phonons and a further reduction of our polycrystalline graphene $k_{||}$,[40] however it appears this effect is less than that of grain boundaries or the substrate here. Our results are also in good agreement with studies of encased graphene and ultra-thin graphite which indicated greater than 34 layers are needed to recover the $k_{||}$ of bulk graphite.[36] Using Raman spectroscopy we correlated a reduction in $k_{||}$ to a reduction in the extracted L_g, a conclusion further supported by the study of Yasaei et al. which reported the detrimental effect of grain

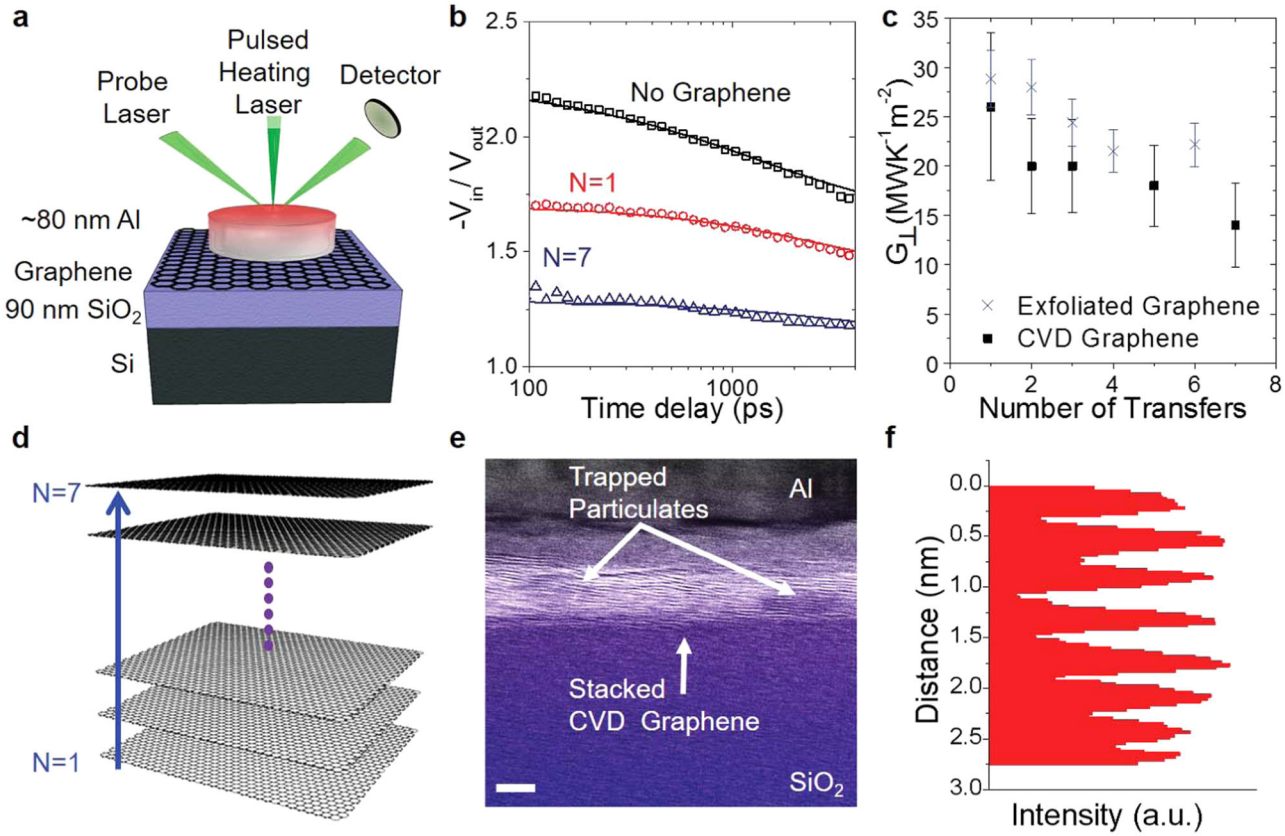

Fig. 3 Cross-plane thermal properties of layer-by-layer assembled graphene films. **a** Schematic representation of experimental setup for TDTR measurements on layer-by-layer assembled graphene films. **b** Ratio of the in-phase to out-of-phase signals as a function of delay time between pump and probe pulses. Representative measurements for Al/SiO_2/Si (no graphene), Al/graphene ($N = 1$)/SiO_2/Si, and Al/graphene ($N = 7$)/SiO_2/Si are shown. The solid lines are best fits to the experimental data (open symbols). **c** Thermal conductance per unit area $G_\perp$ of Al capped layer-by-layer assembled graphene films (filled squares) compared to single and few layer exfoliated graphene (x symbols).[37] Error bars are the estimated experimental uncertainty. **d**, **e** Schematic representation and cross-section BF-STEM image of layer-by-layer assembled graphene films, respectively. The dark regions in **e** are trapped particulates believed to be Cu residues from the graphene transfer process. Scale bar is 5 nm. **f** Intensity profile (BF-STEM) across the stack of a layer-by-layer assembled graphene film ($N = 7$) showing the carbon peak intensity correlating to different graphene layers in the stack. The additional eighth peak is attributed to a bilayer region in one of the CVD transferred films

boundaries on thermal transport depending on the grain boundary angle and morphology.[41]

Our cross-plane thermal conductance ($G_\perp$) measurements of such LBL graphene films show a reduction in $G_\perp$ with increasing layer number (N) from $G_\perp \approx 25$ to 15 $MWm^{-2}K^{-1}$ for $N = 1$ to 7. We attribute this reduction to a weakening of vdW coupling between layers, possibly induced by trapped particulates and a rotational mismatch in the lattices of the stacked graphene layers. However, we cannot exclude the possibility that $G_\perp$is reduced due to reduced mechanical coupling to the underlying SiO_2 resulting from a potential increase in sample stiffness or changes in the vibrational spectra as additional graphene layers are added to the stack. Importantly, as revealed by AFM and cross-section TEM analysis, residual contaminants from the polymer assisted transfer method remain on the surface and in between the CVD graphene layers even after annealing. When such CVD graphene films are assembled in a LBL fashion this can lead to reduced sample quality which must be taken into account when analyzing data for such LBL vdW solids. Hence, additional advancements in the synthesis of 2D based heterostructures and vdW solids are needed in order to probe truly fundamental thermal transport properties across pristine interfaces in such emerging materials.

In conclusion, we have probed the thermal transport of LBL assembled vdW solids constructed from individual graphene layers grown by CVD. Using electrical thermometry on suspended membrane platforms we measure the $k_\parallel$ of such structures and find it varies between 120 and 425 $Wm^{-1}K^{-1}$ over the temperature range of 100–400 K. This is nearly an order of magnitude lower than that of freely suspended CVD-grown graphene films and approximately 30% lower than monocrystalline graphene supported on SiO_2. Technologically, this represents an ultrathin transparent heat spreader with a thermal conductivity similar to bulk copper. However, if copper films were scaled to the thickness of our LBL graphene stacks[45] the increased boundary scattering would likely reduce the thermal conductivity by more than an order of magnitude, indicating graphene vdW solids have superior performance at the single-nanometer thicknesses we report here.

METHODS

Graphene growth, transfer, and characterization

Polycrystalline graphene films are grown on 1.4 mil copper foils using a 1-inch quartz tube low-pressure CVD system. The copper foils are annealed under Ar/H_2 flow for 60 min at 1000 °C prior to graphene growth, which occurs under CH_4 and H_2 flow at 1000 °C for 20 min at a pressure of ~500 mTorr. Transfer of the graphene films is performed by coating one side of the copper foil with a bilayer of 495 K and 950 K PMMA. Graphene films on the opposite side of the copper foil are removed by O_2 plasma etching and the copper foil is etched overnight in CE-100 purchased from Transene Corporation. The PMMA-graphene film is cleaned in a 10% HCl in DI water solution to remove residual metal particles and rinsed again in DI water

prior to transferring the film to the receiving substrates. The PMMA is removed in a 1:1 mixture of methylene chloride to methanol for 20 min and the samples are then annealed in the quartz tube furnace at 400 °C under Ar and H_2 flow to remove residual PMMA. Transmittance measurements are performed using a Varian CARY 5G system photospectrometer. Raman measurements are performed using a scanning confocal Renishaw Raman microsope (inVia and WiRE 3.2 software).

Thermometry platforms

Suspended thermometry platforms were fabricated on a dual-side polished silicon wafer (~300 μm thick). A thin layer of Al_2O_3 (~5 nm) is deposited by atomic layer deposition followed by deposition of low-stress $Si_3N_{3.3}$ films by plasma enhanced CVD in a mixed frequency mode. The Al_2O_3 layer acts as an etch stop for a BOSCH 2 through-wafer etch. Graphene is transferred to the $Si_3N_{3.3}/Al_2O_3/Si$ substrates as previously described, and standard photolithographic techniques are used to pattern the metal electrodes and graphene samples. The graphene is etched from underneath the electrode patterns using an O_2 plasma, followed by electron-beam evaporation of 20 nm SiO_2, 5 nm of Ti, and 30 nm of Pd. The thickness of metal contact pads and metal spacers are further increased to ~100 nm by photolithography and e-beam evaporation, in order to allow for easier wire bonding and to provide a spacer between the device active area and the carrier wafer (Supplementary Information). A final photolithography step is used to align backside etch windows to topside features and through-wafer etching is accomplished using a BOSCH 2 process in an induced coupled plasma reactive ion etcher. Photoresists are removed in Remover PG at 80 °C following through-wafer etching. Importantly, graphene films are protected throughout all photolithography process steps by a thin layer of PMGI SF5, a PMMA derivative. Samples for cross-plane thermal measurements are fabricated by transferring graphene films as described above, to SiO_2/Si (~90 nm/0.5 mm) substrates followed by shadow mask evaporation of ~80 nm thick Al disks with varying radii between 40 and 125 μm. Graphene thickness and effective grain size are evaluated with Raman spectroscopy using a 633 nm laser. The $Si_3N_{3.3}$ stoichiometry is measured by X-ray photoelectron spectroscopy.

Electrical and thermal measurement

In-plane: The heater and sensors of the suspended membrane devices are wirebonded to a KYOCERA leaded ceramic chip carrier, prior to being placed in a Janis vacuum probe station for measurements. The probe station is capable of reaching vacuum levels down to 10^{-6} Torr and the ambient temperature is controlled with a Lakeshore model 377 temperature controller and liquid nitrogen cooling. Prior to all measurements the device is annealed for ≈8 h in vacuum at 450 K to stabilize the resistance of all the metal electrodes. The heater and sensor resistances are calibrated as a function of temperature from 80 K to 450 K. This is done using a 4-point Delta Mode technique and the Keithley 6221/2182A current source and nanovoltmeter combo. Current is applied to the heater using a Keithley 4200-SCS and heater power and resistance are monitored with a 4-point current-voltage measurement. The dependence of the sensor resistance as a function of heater power is monitored by a 4-point Delta Mode technique.

Cross plane: The cross-plane thermal measurement is done by time-domain thermoreflectance (TDTR) using a Ti-sapphire laser that operates at a wavelength near 785 nm. All measurements are performed at room temperature. We use a double modulation technique with the pump beam modulated at 9.8 MHz and the probe beam modulated at 200 Hz to improve the signal-to-noise and suppress background created by a diffusely scattered pump light. To a good approximation at high modulation frequencies, the in-phase signal of the lock-in amplifier $V_{in}(t)$ is proportional to the time-domain response of the sample, i.e., the temperature excursion created by each pump optical pulse. The out-of-phase signal $V_{out}(t)$ is mostly determined by the imaginary part of the frequency domain response at the modulation frequency and is approximately independent of delay time. Comparing V_{in}/V_{out} of measurement and of thermal modeling, we determine the cross-plane thermal conductance of the Al/*N* layers of graphene/SiO_2 stack ($G_\perp$). A complete description of the analysis of TDTR data and the interpretation of V_{in} and V_{out} can be found in ref. [42].

STEM characterization

The cross-section sample was prepared by lift-out technique using a FEI DB-235 focused-ion beam (FIB). The STEM images and EELS spectra were recorded using a JEOL 2200FS equipped with a CEOS probe corrector at 200 kV. Both BF and HAADF detectors were used for recording.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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AUTHOR CONTRIBUTIONS

D.E. and E.P. conceived the experimental design. D.E. fabricated and measured in-plane thermal measurement samples with assistance from S.N.D., J.L., W.P.K., and J.A. R. Z.L. performed finite element modeling, analytical modeling, and uncertainty analysis. G.-M.C. and D.G.C. performed cross-plane thermal measurements and analysis. Y.M. and J.-M.Z. performed TEM imaging and analysis. A.S. performed NEGF calculations. F.L., N.C.W., R.T.H. aided in sample fabrication and materials characterization. All authors made substantial contributions to data acquisition, analysis, and interpretation. All authors discussed results and co-wrote the final manuscript.

ADDITIONAL INFORMATION

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Supplementary Information

Thermal Transport in Layer-by-Layer Assembled Polycrystalline Graphene Films

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Table of Contents:

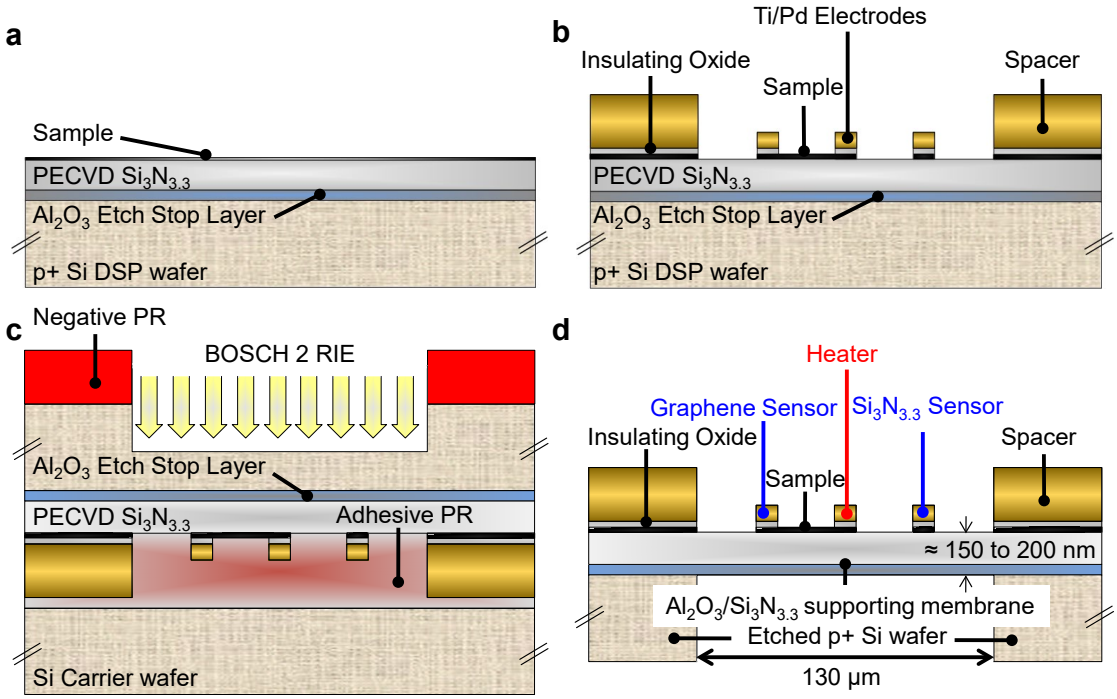
1. Suspended Platform Fabrication

Step 1 - Wafer preparation, etch stop layer, and low stress SiN deposition: 275 ± 25 μm dual side polished Si wafers were cleaned in a Piranha solution (5:1 H_2O_2 to H_2SO_4) at 120 °C for 15 minutes followed by a 5 minute rinse in deionized water. The wafers were then dried under N_2 flow and the native oxide etched in a 10:1 buffered oxide etch (BOE) just prior to atomic layer deposition (ALD) of a thin Al_2O_3 etch stop layer. 5 nm of Al_2O_3 were deposited using a Cambridge Nanotech ALD system. The silicon wafer was heated to 250 °C in the reaction chamber, and trimethyl aluminum (TMA) and water vapor were pulsed into the chamber to deposit Al_2O_3 with atomic layer precision. Next, approximately 150 to 200 nm of silicon nitride ($Si_3N_{3.3}$) was deposited using an STS Multiplex PECVD system in a mixed frequency mode (Fig. S1a).

Step 2 - Graphene growth and transfer: Graphene was grown using low pressure chemical vapor deposition (LPCVD) on 1.4 mil Cu foils purchased from Alfa Aesar (CAS 7440-50-8). We annealed the copper foils at 1000 °C under Ar/H_2 flow for 60 minutes, at a base pressure of ≈ 4.5 Torr. Graphene was grown for 20 minutes at 1000 °C under CH_4 and H_2 flows at ≈0.5 Torr. The resulting graphene and Cu substrates were cooled to 150 °C under the same CH_4 and H_2 flow at a rate of ≈10 °C/minute, followed by cooling to room temperature under Ar flow. One side of the Cu foil was coated with a bilayer of PMMA (495K and 950K), with each layer being deposited at 3000 rpm for 30 seconds followed by a 200 °C bake for 2 minutes. The unprotected graphene on the opposite side of the Cu foil was removed by O_2 plasma etching, and the copper foil was etched in Transcene CE-100 overnight. The resultant PMMA/graphene film was then rinsed in a series of dilute HCl and deionized water baths before being wicked onto the receiving substrates, prepared as described in Step 1 (Fig. S1a). PMMA was removed in a 1:1 methylene chloride/methanol solution for 30 min followed by a 400 °C anneal under Ar and H_2 flow. The transfer process was repeated in a layer-by-layer manner to fabricate graphene based van der Waals solids.

Step 3 - Lithographic patterning and electrode deposition: The heater and sensor electrodes were patterned using standard photolithographic techniques. A thin layer of polydimethylglutarimide (PMGI-SF5) lift-off resist was spun onto the graphene/silicon nitride samples at 3000 RPM for 30 seconds, followed by a 5 minute bake at 150 °C. The sample is then coated with ≈1.5 μm of Shipley 1813 photoresist and baked at 110 °C for 75 seconds. Exposure was done

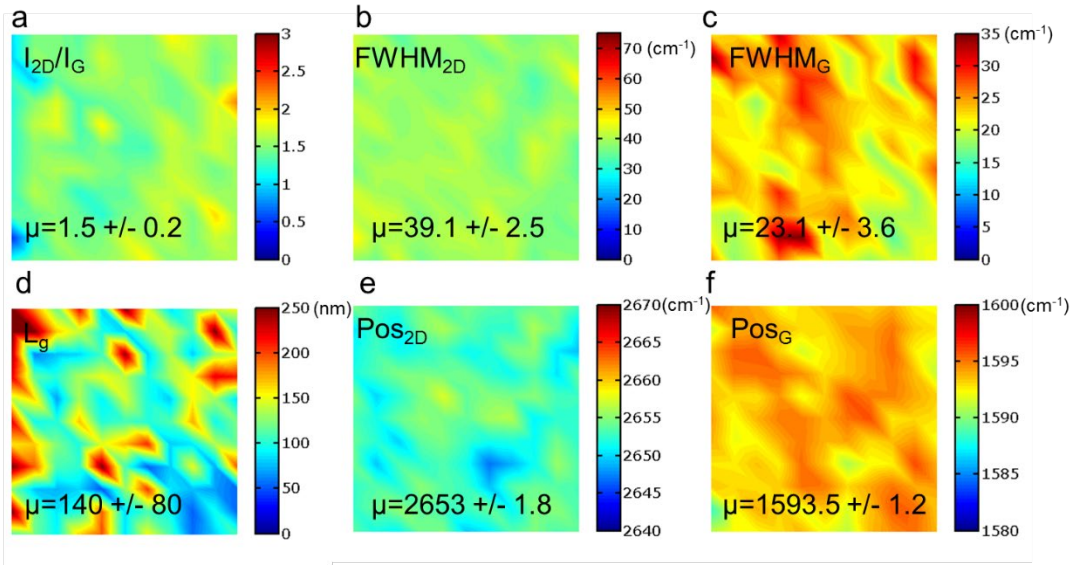
through a dark field mask (≈ 40 mJ/cm^2), and the patterns were developed using MF 319 developer. The sample is then placed in electron-beam evaporators for deposition of 20 nm of SiO_2, 5 nm titanium (Ti), and 30 nm of palladium (Pd). Evaporators were evacuated to a base pressure of ≈8×10^{-7} Torr before deposition. Lift-off is performed by placing the sample in Remover PG at 80 °C. Similar lithographic processes are performed to pattern the graphene films between the center and an edge electrode, as well as to increase the metal thickness of the metal pads to 100 nm. Graphene patterning is performed by O_2 plasma etching for 45 seconds at 100 Watts at a background pressure of 100 mTorr (Fig. S1b). The extra thickness of the metal pads aids in wirebonding, but also serves as a spacer for the device active region during backside processing. Importantly, the graphene must be removed from underneath the metal pads in order to perform the wirebonding needed for thermometry measurements.



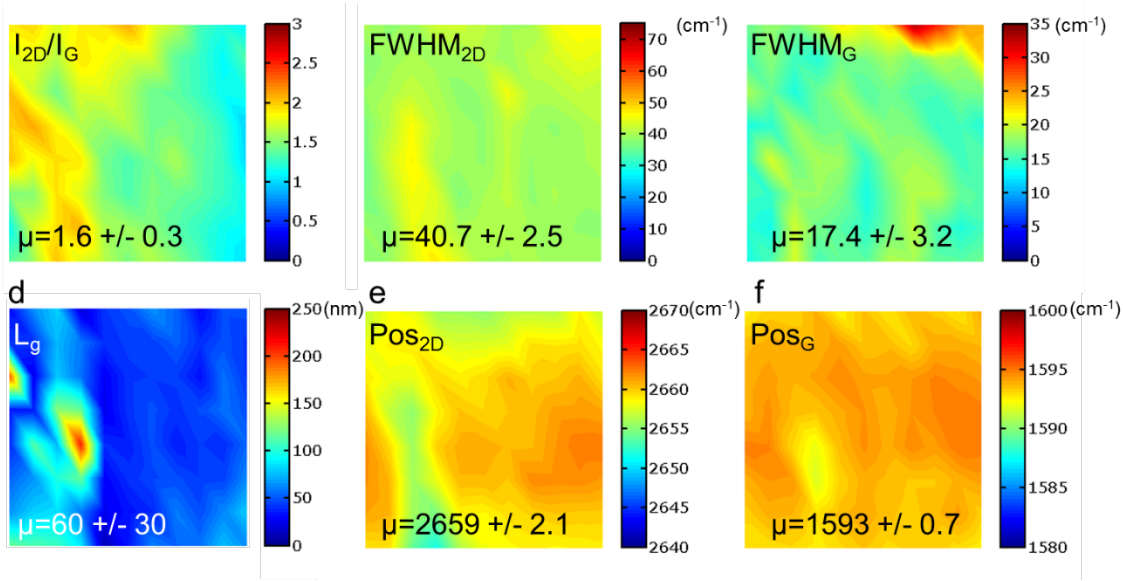
Supplementary Figure S1 | Fabrication process of suspended electrical thermometry platform. (a) Al_2O_3, PECVD $Si_3N_{3.3}$, and the graphene sample are deposited on a dual-side polished Si wafer. (**b)** Electrodes, spacers, and graphene sample are patterned with standard photolithographic techniques. **(c)** Backside features are aligned to topside features and the sample is mounted to a carrier wafer for through wafer etching with a BOSCH 2 reactive ion etching (RIE) process. **(d)** Final schematic of suspended thermometry platform. The insulating oxide prevents electrically conducting samples (e.g. graphene) from shorting the heater and sensor. The spacer adds a gap between the suspended membrane and the carrier wafer during the release step.

Step 4 - Backside patterning and membrane suspension: Prior to back side processing the topside structures of the wafer are protected by applying a bilayer of PMGI-SF 5 and S1813 photoresist as previously described. The PMGI under layer is essential to prevent the "hard baking" of the S1813 photoresist from contaminating the topside features. The back side of the sample is patterned by spin coating NR5-8000 at 3000 RPM for 40 seconds (≈ 8 to 9 μm). The photoresist is baked at 150 °C for 60 seconds. Alignment to topside features is done using a Quintel UL 7000 series mask aligner with an infrared (IR) through wafer backside alignment tool. Exposure is performed through a bright field mask (≈ 125 mJ/cm^2). The sample is then baked at 100 °C for 60 seconds and backside patterns are developed using RD6 developer. The wafer is attached to a carrier wafer for backside etching in an anisotropic deep silicon etching system. A BOSCH 2 process is used to etch completely through the wafer (Fig. S1c). The high selectivity of the BOSCH 2 process to Si over Al_2O_3 facilitates increased yield in the process. The Al_2O_3 prevents any etching of the PECVD SiN membrane, which could occur due to variance in the wafer thickness or non-uniform etch rates across the platen area of the deep silicon etching system. After verifying through wafer etching by optical microscopy, the carrier wafer and samples are immersed in Remover PG, releasing the sample and suspending the thermometry platform membrane. Residual polymer is removed via annealing at 400 °C anneal under Ar and H_2 flow.

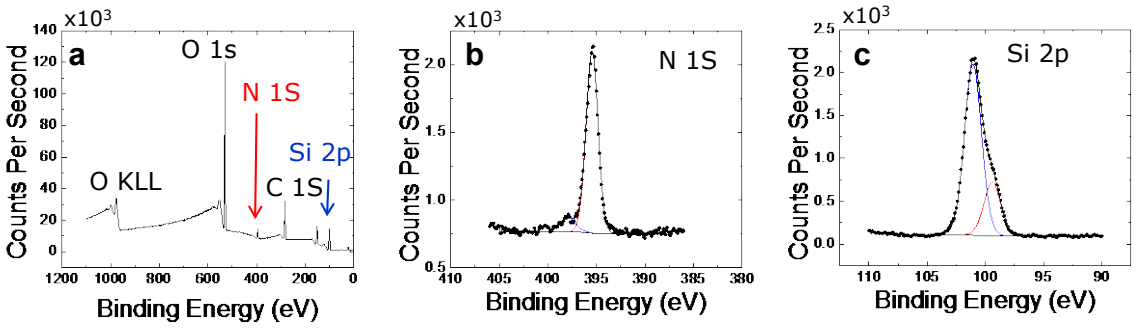
2. Graphene and Supporting Membrane Characterization



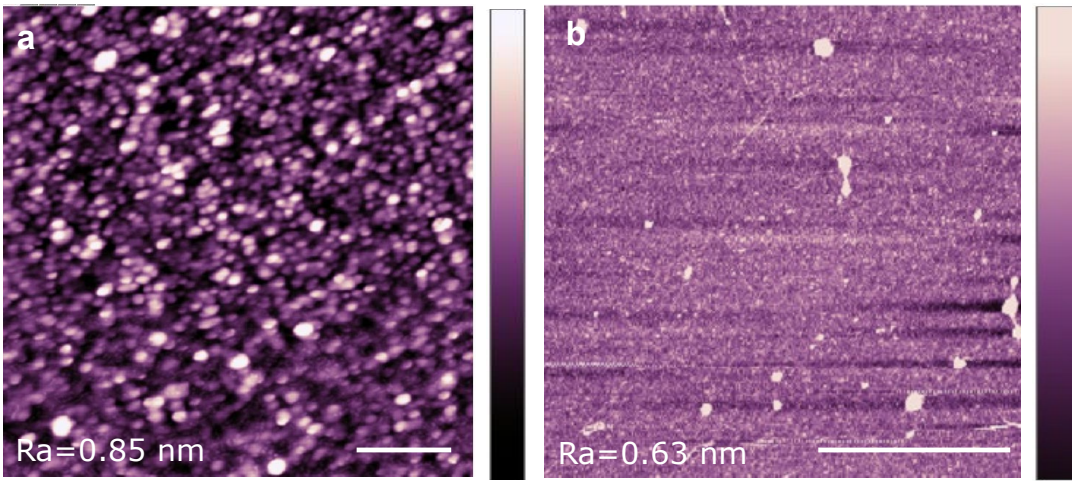
Supplementary Figure S2 | 22 μm × 22 μm Raman spectroscopy maps of *N*=1 graphene with larger grain. (a) Raman map of the intensity ratio of the 2D to G bands. **(b,c)** Full-width half maximum value for the 2D and G bands, respectively. **(d)** Extracted crystallite size from the data in (a). **(e,f)** Peak position of the 2D and G bands. Raman data were collected with a 2 μm step using a 633 nm excitation wavelength after all processing and thermal transport measurements were complete. Average values for each map are denoted as μ on the lower left of the map.



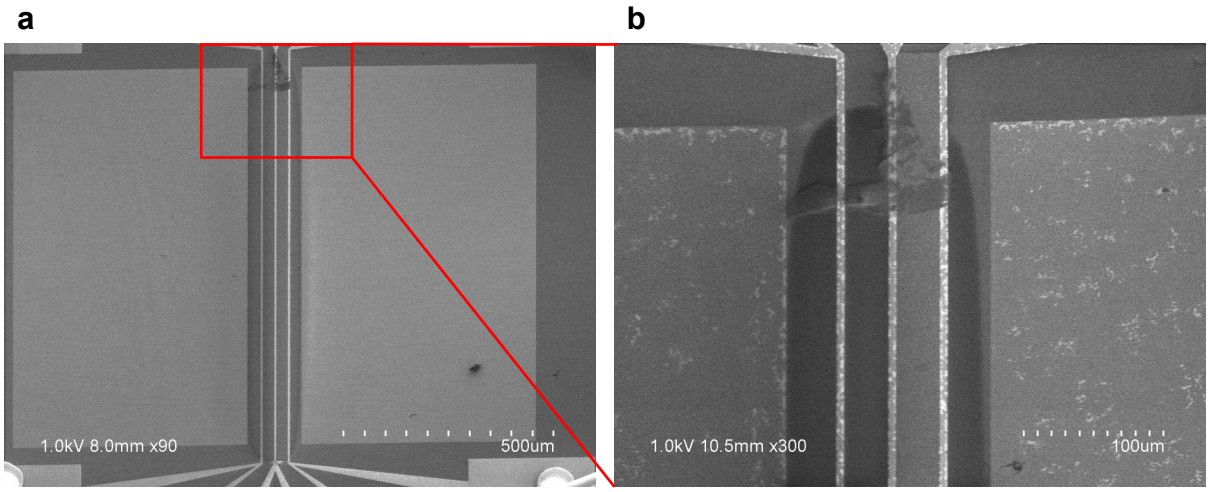
Supplementary Figure S3 | 22 µm × 22 µm Raman spectroscopy maps of *N*=1 graphene with smaller grain. (a) Map of the intensity ratio of the 2D to G bands. **(b,c)** Full-width half maximum value for the 2D and G bands, respectively. **(d)** Extracted crystallite size from the data in (a). **(e,f)** Peak position of the 2D and G bands. Raman data were collected with a 2 µm step using a 633 nm excitation wavelength after all processing and thermal transport measurements were complete. Average values for each map are denoted as µ on the lower left of the map.



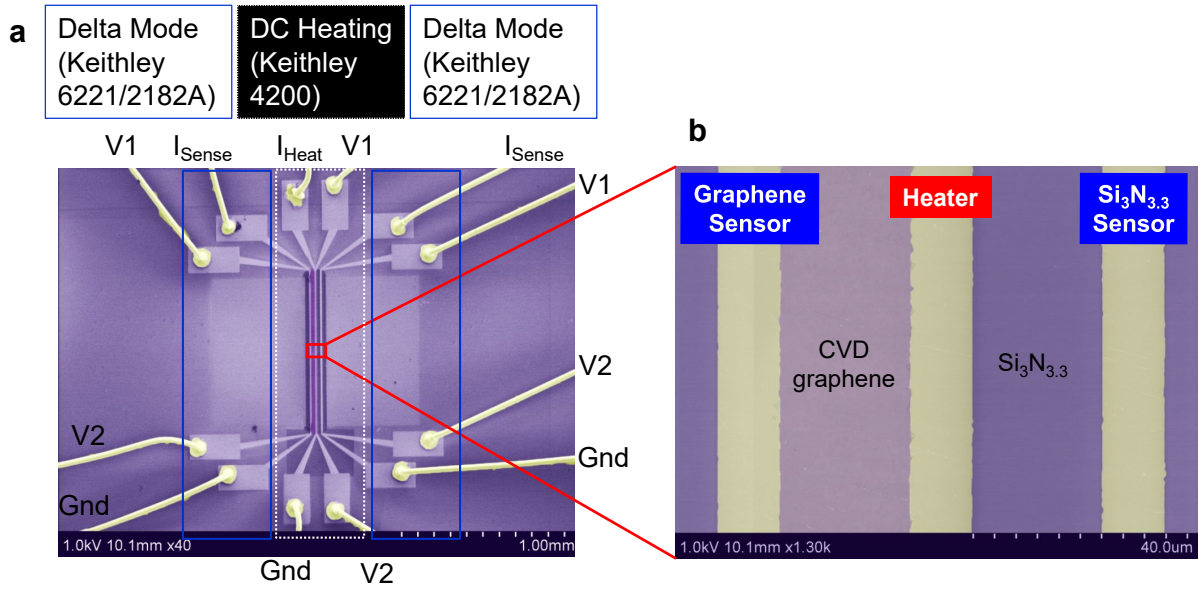
Supplementary Figure S4 | XPS analysis of PECVD silicon nitride. Typical XPS results of counts per second (CPS) vs. binding energy for our silicon nitride samples deposited via PECVD on Al_2O_3/Si substrates; **(a)** survey, **(b)** N 1s, **(c)** Si-2p peaks. In (b,c) symbols are raw data and solid lines are fits.



Supplementary Figure S5 | AFM analysis of PECVD silicon nitride and *N*=1 CVD graphene layers. (a) $Si_3N_{3.3}$ surface without and **(b)** with transferred CVD graphene. Scale bars are 200 nm and 2 μm, respectively. The height color bar is 6.5 nm.

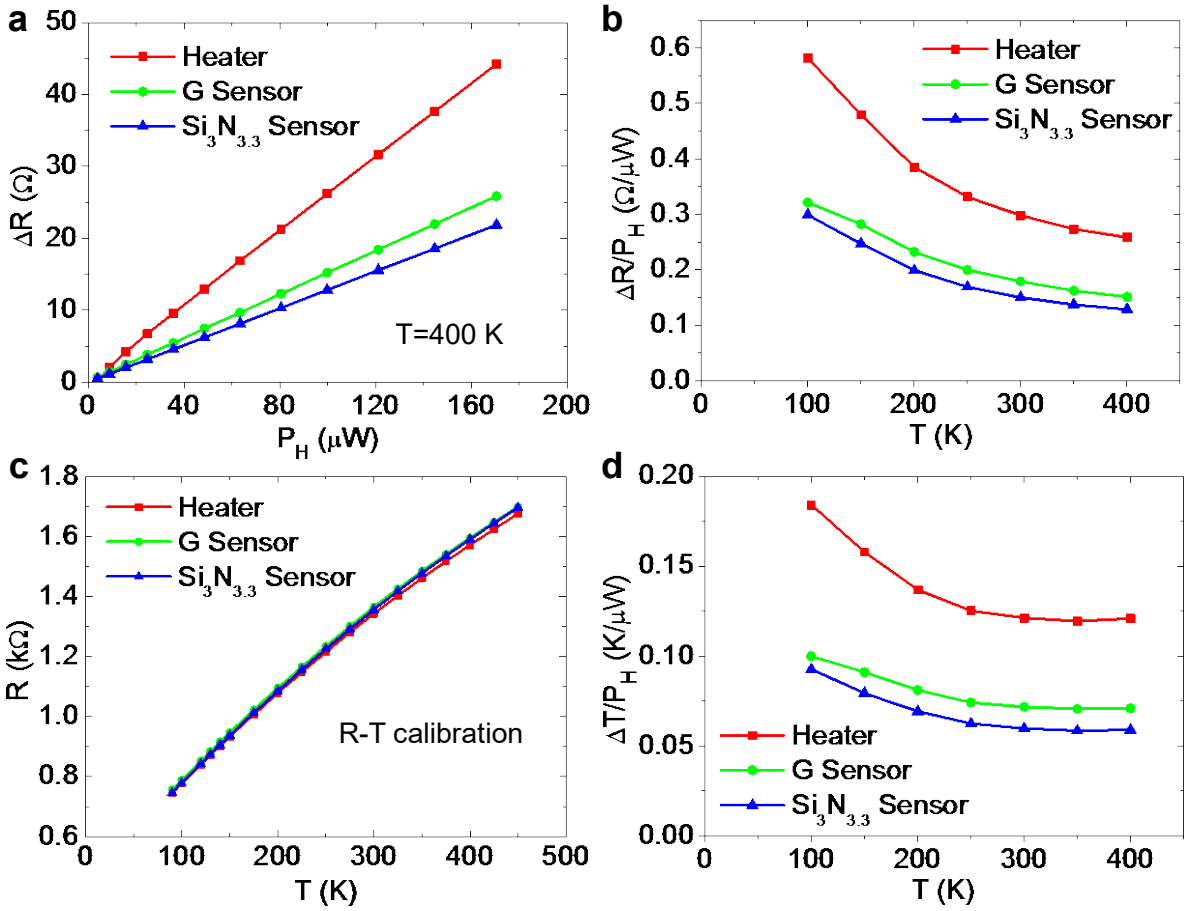


Supplementary Figure S6 | SEM analysis of *N*=3 electrical thermometry sample. (a). SEM image of suspended thermometry platform with *N*=3 transfers of CVD grown graphene. **(b)** Zoom-in of the highlighted region in (a). Residual polymeric residue from the fabrication process is located at one edge of the platform resulting in a slightly reduced thermal conductivity of graphene as compared to the *N*=1, 2, and 4 samples (see Fig. 2c and Fig. S11).



Supplementary Figure S7 | Electrical thermometry setup. (a) Scanning electron microscopy image of a wirebonded suspended electrical thermometry platform showing the voltage and current source/measurement equipment setup. **(b)** Higher magnification SEM image of the device in (a) highlighting the contrast of the supporting $Si_3N_{3.3}$ membrane and the graphene coated membrane.

3. Experimental Set-Up and Data Analysis



Supplementary Figure S8 | In-plane thermal measurement process. (a) Measured resistance change vs. heater power at ambient $T = 400$ K for the heater, the graphene sensor and the $Si_3N_{3.3}$ sensor. The fitted slopes give the resistance change per unit heater power $\Delta R/P_H$. **(b)** Measured $\Delta R/P_H$ at different ambient T for the heater and two sensors. **(c)** Resistance calibration vs. temperature for the heater, graphene sensor, and $Si_3N_{3.3}$ sensor. **(d)** Converted temperature rise per unit heater power $\Delta T/P_H$ from $\Delta R/P_H$ in (b) based on R-T calibration in (c).

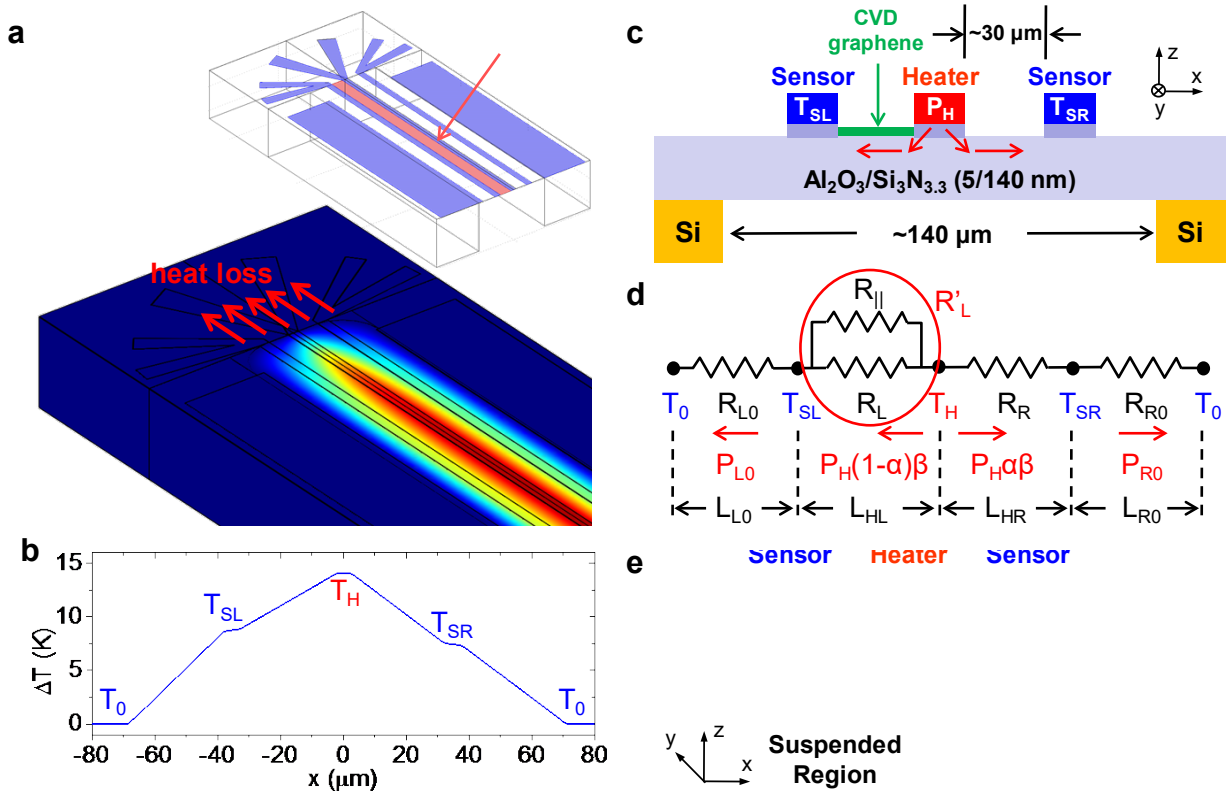
4. 3D Finite Element and Analytical Modeling

Finite Element Model

We use COMSOL software to extract the thermal properties of our layer-by-layer assembled graphene vdW solids and the supporting $Si_3N_{3.3}$ substrate from the measured ΔT vs. P_H. To do so we set up a three-dimensional (3D) finite element method (FEM) model of the structure as shown in Fig. S9a, where only a half of the sample is included due to its symmetry. All the device dimensions are set according to physical characterization such as SEM and ellipsometry. We perform the simulation by setting isothermal boundary conditions along the bottom surface and three side surfaces (except the symmetry plane) of the substrate. The remaining outer surfaces of the structure are given an adiabatic boundary condition. We apply a constant power density to the center electrode (heater) in order to simulate Joule heating in the heater. A stationary calculation is performed to obtain the steady-state temperature distribution as shown in Fig. S9a. We adjust the thermal conductivities of the sample (k_g) and $Si_3N_{3.3}$ layer (k_{SiN}) in order to simultaneously fit the experimental values of the temperature rises in the heater and two sensors ($\Delta T_H/P_H$, $\Delta T_{SL}/P_H$, $\Delta T_{SR}/P_H$). We use a single desktop computer to implement the fitting process by using MATLAB to interface directly with COMSOL. We optimized the mesh prior to our calculations, and each calculation (i.e. data at each ambient temperature) takes ~1 hour to converge to a best-fit. Importantly, we included thermal contact resistance effects of all interfaces in FEM calculations, and verified the thermal contact resistances did not play a significant role in the data extraction. For example, using the simple estimate of $\Delta T_H = P_H \times R_c/A_c$, where R_c is thermal contact resistance, and A_c is the area of the heater electrode across the membrane and graphene films, we estimate that only ~0.2 mK is dropped at the contacts with a ΔT of 10K. Additionally, changing R_c by a factor of 2 only leads to <0.4% change of extracted k_g. The R_c contributions to the error bars of extracted thermal conductivity were also included in the uncertainty analysis described in Section 5.

Analytical Model

Besides using the accurate finite element simulations described above to extract measured thermal conductivity, we emphasize that our suspended platform has an advantage to simply estimate measured thermal conductance/conductivity in an analytical way. Figure S9c shows the schematic of the cross-section of our suspended platform, and the simulated temperature profile across the suspended $Si_3N_{3.3}$ membrane is shown in Fig. S9b. The suspended part is so thin that it can be regarded as a 2D piece hanging on a big 3D heat sink, so the temperature always drops to the background temperature T_0 at the edges of the Si trench (see Figs. S9a,b). This means the platform can be approximated as a thermal circuit, only including the thermal resistances of the suspended



Supplementary Figure S9 | Heat flow analysis for FEM and analytic model. (a) Structure of the 3D FEM model (top) and simulated temperature distribution with highlighted heat loss along y-direction (bottom). **(b)** Temperature profile along the x-direction in the middle of suspended $Si_3N_{3.3}$ membrane, showing asymmetric heat flows. **(c)** Schematic of the cross-section of our suspended platform. **(d)** Approximated thermal circuit of our platform. **(e)** Schematic of the suspended part with colored cross-sections for heat loss estimation.

$Si_3N_{3.3}$ membrane (R_{L0}, R_L, R_R, R_{R0}) and graphene ($R_{||}$), as shown in Fig. S9d. The measured average temperature rises of the heater and two sensors are $\Delta T_H = T_H - T_0$, $\Delta T_{SL} = T_{SL} - T_0$, and $\Delta T_{SR} = T_{SR} - T_0$, respectively, at a given total heating power P_H. To calculate thermal conductance from the measured temperature rises, we need to carefully estimate the heat flow along the left and right directions. First, since one side has graphene and the other does not, the heat flow is not symmetric in the two directions. Thus, we assume the percent of the total power P_H which goes to the $Si_3N_{3.3}$ (right) side as α, and consequently $(1-\alpha)$ percent goes to the graphene (left) side. Second, as heat flows from the heater to two sensors (x direction), a portion will be lost in the perpendicular (y) direction, as shown in Fig. S9a. We assume the effective portion that reaches two sensors is β percent. Overall, the effective heat flow from the heater to two sensors are $P_H(1-\alpha)\beta$ and $P_H\alpha\beta$, respectively, as shown in Fig. S9d. If we know α and β, combining the measured T rises, we can calculate the total thermal conductance between the heater and $Si_3N_{3.3}$ side sensor (G_R), and between the heater and graphene side sensor ($G_L^{'}$):

$$G_R = \frac{P_H \alpha \beta}{\Delta T_H - \Delta T_{SR}}, \tag{S1}$$

$$G_L' = \frac{P_H (1-\alpha)\beta}{\Delta T_H - \Delta T_{SL}} = G_{||} + G_L, \tag{S2}$$

where G_L is the thermal conductance of $Si_3N_{3.3}$ right under graphene, and it can be obtained from G_R by dimension scaling because they have slightly different conduction lengths in real samples (dimensions are labeled in Fig. S9c):

$$G_L = G_R \frac{L_{HR}}{L_{HL}} = \frac{P_H \alpha \beta}{\Delta T_H - \Delta T_{SR}} \frac{L_{HR}}{L_{HL}} \tag{S3}$$

Thus, the thermal conductance of graphene is

$$G_{||} = G_L^{'} - G_L = \frac{P_H (1-\alpha)\beta}{\Delta T_H - \Delta T_{SL}} - \frac{P_H \alpha \beta}{\Delta T_H - \Delta T_{SR}} \frac{L_{HR}}{L_{HL}} \tag{S4}$$

Correspondingly, the thermal conductivity of graphene and $Si_3N_{3.3}$ can be obtained as:

$$k_{||} = G_{||} \frac{L_{HL}}{W h_g} \tag{S5}$$

$$k_{SiN} = G_R \frac{L_{HR}}{W h_{SiN}} \tag{S6}$$

where W is the width of graphene, the same as the length of heater/sensor electrodes, and h_g and h_{SiN} are the thickness of graphene and $Si_3N_{3.3}$ membrane, respectively.

To obtain the thermal conductance of graphene and $Si_3N_{3.3}$ from Eq. S4 and S1, α and β should be calculated. As shown in Fig. S9d, the effective heat flow from the left (right) sensor to left (right) edge is P_{L0} (P_{R0}). P_{L0} and P_{R0} are not equal to $P_H(1-\alpha)\beta$ and $P_H\alpha\beta$, respectively, due to continuous loss as heat flows from the heater to two edges. As a first-order approximation, however, we can assume the ratio of the left heat flow to the right heat flow is always kept constant, that is,

$$\frac{1-\alpha}{\alpha} = \frac{P_{L0}}{P_{R0}} = \frac{(T_{SL}-T_0)/R_{L0}}{(T_{SR}-T_0)/R_{R0}} = \frac{\Delta T_{SL} L_{R0}}{\Delta T_{SR} L_{L0}} = \gamma \tag{S7}$$

where ΔT_{SL}, ΔT_{SR}, L_{R0}, and L_{L0} are all known quantities. Thus, α can be obtained by

$$\alpha = \frac{1}{1+\gamma} = \frac{1}{1+(\Delta T_{SL} L_{R0})/(\Delta T_{SR} L_{L0})} \tag{S8}$$

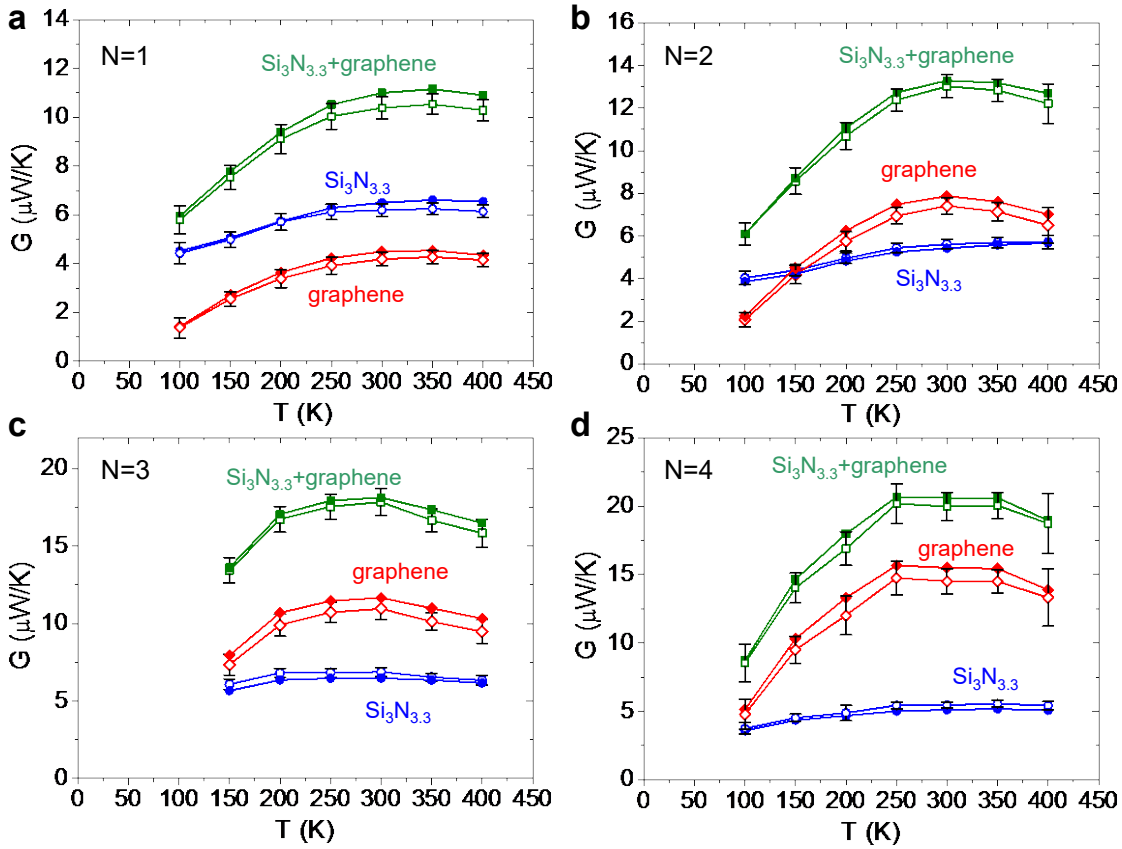
The calculated α for $N = 1$ to 4 layer graphene is from 43% to 36%, indicating the thicker graphene (larger conductance), the more asymmetric heat flows in two directions.

To estimate β, we consider the suspended part of the platform, as shown in Fig. S9e. To the first-order approximation, we assume that the heat flow through a cross-section is proportional to its area and thermal conductivity. Then, as heat flows from the heater to the two sensors, the percentage of power loss in the y-direction is

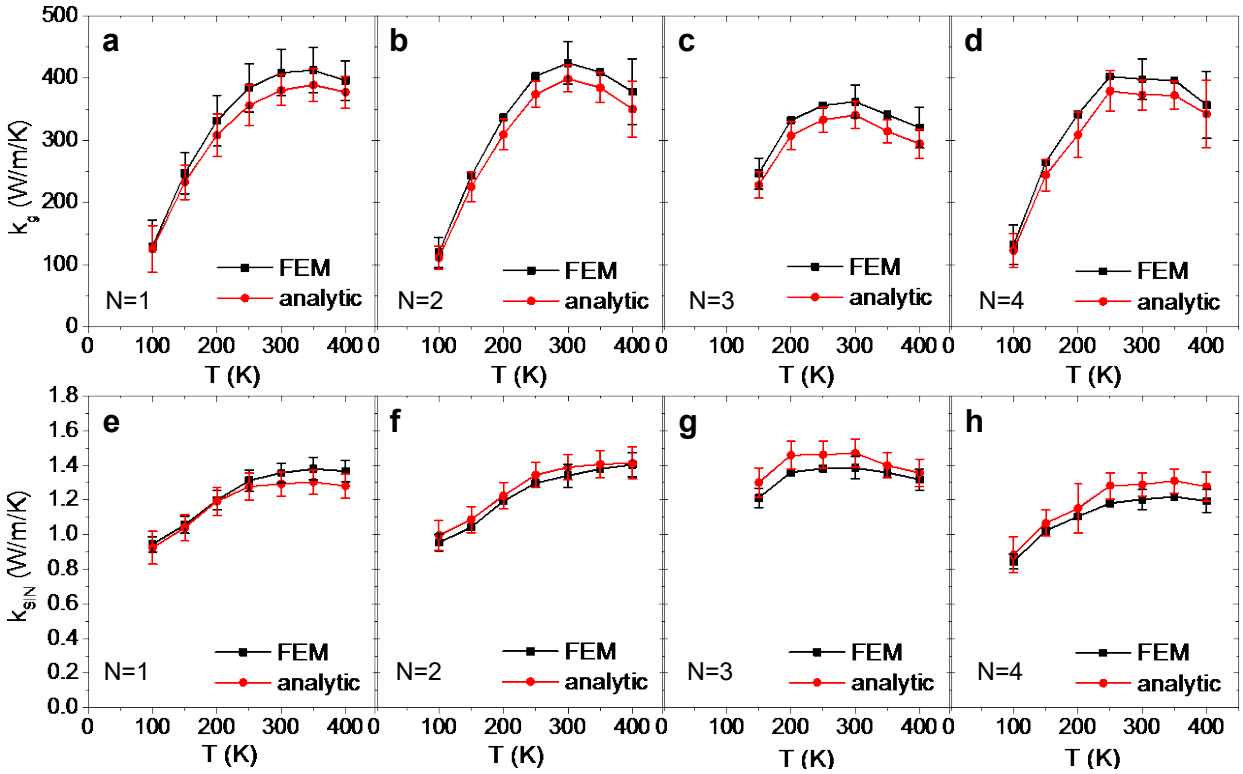
$$1-\beta = \frac{A_{red} k_{electrode} + A_{purple} k_{SiN}}{(A_{red} + A_{blue}) k_{electrode} + (A_{purple} + A_{green}) k_{SiN}} \tag{S9}$$

where A's are the areas with corresponding colors in Fig. S9e, and k's are thermal conductivities of corresponding materials. The estimated β by this method is about (90±3)%. A detailed check by analyzing heat flux from the finite element results is consistent with this range. Since Eq. S9 is a very rough estimation, it cannot be considered as an accurate expression like Eq. S8. Therefore, for simplicity we use a constant β = 90% in our analytic model, and treat it as an independent parameter, rather than a function of other parameters, in the uncertainty analysis.

Plugging the obtained α and β into Eq. S2-S3, we can calculate the total thermal conductance of "graphene+$Si_3N_{3.3}$" part and that of $Si_3N_{3.3}$ under graphene, then their difference gives graphene thermal conductance (Eq. S4). The results are shown by open symbols in Fig. S10 for N = 1 to 4 layer(s) of graphene. Correspondingly, the calculated thermal conductivities of graphene and $Si_3N_{3.3}$ from Eq. S5-S6 are shown by red dots in Fig. S11. Compared with finite element results (solid symbols in Fig. S10 and black squares in Fig. S11), the simple analytic model gives consistent results; the differences are around 5%, which is a systematic error of this extraction method due to the simplified 1D circuit model (Fig. S9d) and approximations made for the estimated α and β. Therefore, for quick extractions of thermal conductance/conductivity, this simple analytic model can be used, which is an advantage of our suspended thermometry platform.



Supplementary Figure S10 | Extracted thermal conductance from FEM simulations and analytic model. (a-d), Extracted thermal conductance of the combined $Si_3N_{3.3}$ and graphene part (green), $Si_3N_{3.3}$ under graphene (blue), and graphene (red) for N=1 to 4 layer samples. Solid symbols are from finite element simulations, and open symbols are from the simple analytic model.



Supplementary Figure S11 | Extracted thermal conductivity from FEM simulations and analytic model. (a-d), Extracted thermal conductivity of graphene with *N*=1 to 4 layers. **(e-h)**, Extracted thermal conductivity of $Si_3N_{3.3}$ for *N*=1 to 4 layer samples. Black squares are from finite element simulations, and red circles are from the simple analytic model.

5. Uncertainty Analysis

For both finite element model and simple analytic model, the uncertainty of extracted thermal conductance (or conductivity) can be estimated by the classical partial derivative method:

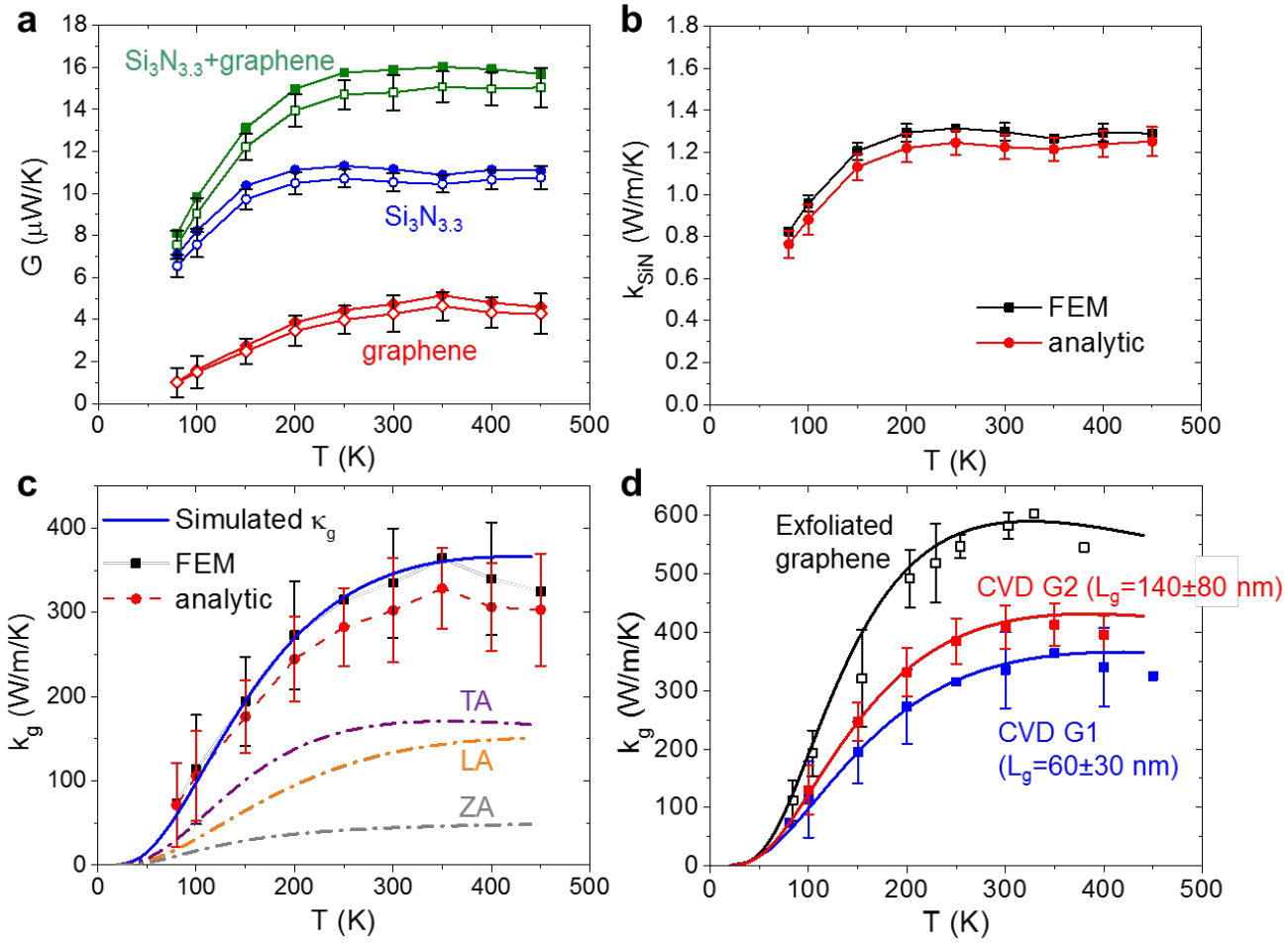
$$\frac{U_G}{G} = \sqrt{\sum_i \left(S_i \times \frac{U_{x_i}}{x_i} \right)^2} \quad \text{or} \quad \frac{U_k}{k} = \sqrt{\sum_i \left(S_i \times \frac{U_{x_i}}{x_i} \right)^2} \tag{S10}$$

where U_G (or U_k) is the total uncertainty in the extracted thermal conductance G (or conductivity k), U_{xi} is the uncertainty of the i-th independent input parameter x_i, and the dimensionless sensitivity S_i is defined by

$$S_i = \frac{x_i}{G}\frac{\partial G}{\partial x_i} \quad \text{or} \quad S_i = \frac{x_i}{k}\frac{\partial k}{\partial x_i} \ . \tag{S11}$$

To highlight the relative importance of each input parameter, we define their absolute contributions as $c_i = |S_i| \times (U_{xi}/x_i)$, and relative contributions as $c_i^2/\Sigma c_i^2$. For the finite element simulation, the partial derivative in S_i is evaluated numerically by giving small perturbation of each parameter x_i around its typical value and redoing the extraction simulation to obtain the change of k. For the simple analytic model, the partial derivative in S_i is derived analytically. We note that for thermal conductance of Eq. S1-S4, α is not an independent input parameter; it is a function of ΔT_{SL}, ΔT_{SR}, L_{R0}, and L_{L0} (Eq. S8), so S_i should be calculated directly with respect to these parameters, rather than α. The evaluated uncertainties from both models are plotted in Figs. S10 and S11, and their values are quite similar.

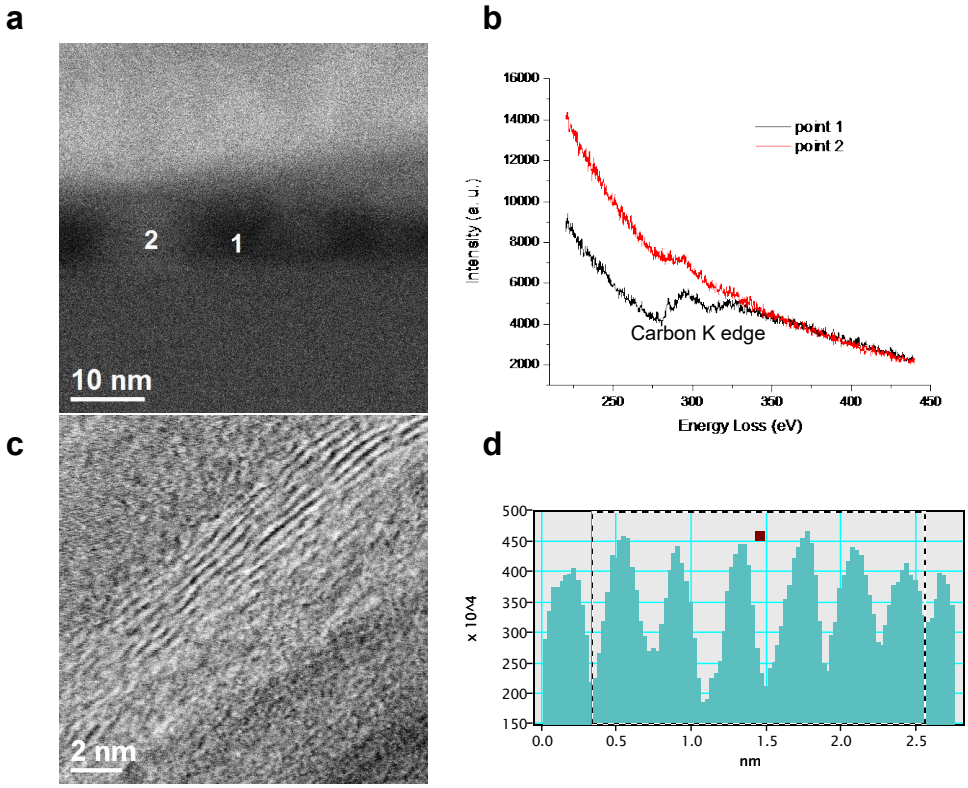
6. Grain Size Effects



Supplementary Figure S12 | Comparison of CVD grown graphene with different grain sizes (L_g). (a) Extracted thermal conductance values of sample with N=1 graphene layers and L_g = 60 ± 30 nm. **(b)** Extracted thermal conductivity values for the supporting $Si_3N_{3.3}$ membrane for the sample in (a). **(c)** Comparison of NEGF simulations with L_g = 60 nm to extracted thermal conductivity values from FEM (black squares) and analytical (red circles) models. The dashed-dot lines are the calculated contributions from the ZA, LA, and TA phonons. **(d)** Comparison of NEGF simulations with best-fitted L_g = 60 nm (blue line), 140 nm (red line) and exfoliated graphene (black line) to experimental data (symbols). The listed L_g in (d) are extracted from Raman Spectroscopy, and they are in excellent agreement with best-fitted L_g in NEGF simulations.

7. STEM and EELS Characterization

The bright contrast of trapped particulates in Fig S13 indicates they are composed of elements with larger atomic number than carbon. The EELS spectra demonstrate the trapped particulates (point 2) contain less carbon compared with multi-layered graphene (point 1). Thus, they are likely to be metal residues. TEM energy analysis was applied on the residue area and signals of Si, Al, C, O, Pt and Cu were observed. Signal of Fe was not observed in EELS or TEM EDX. There is high possibility that the particulates are Cu residues left after etching.



Supplementary Figure S13 | STEM and EELS characterization. (a) HAADF-STEM images of *N*=7 sample. **(b)** carbon EELS spectra of point 1 and 2 in (a). **(c)** Cross-section BF-STEM image of layer-by-layer assembled graphene *N*=7 film. Scale bar is 2 nm. **(d)** Data of intensity profile (BF-STEM) across the stack of a layer-by-layer assembled graphene film (*N*=7) showing the carbon peak intensity correlating to different graphene layers in the stack. Data was plotted in Fig. 3f for clarity.