Self-Aligned Cu Etch Mask for Individually Addressable Metallic and Semiconducting Carbon Nanotubes

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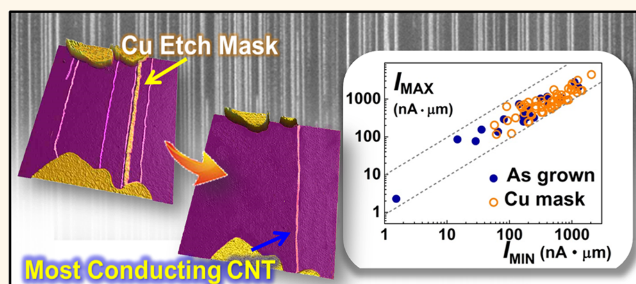
ABSTRACT Two means to achieve high yield of individually addressable single-walled carbon nanotubes (CNTs) are developed and examined. The first approach matches the effective channel width and the density of horizontally aligned CNTs. This method can provide single CNT devices and also allows control over the average number of CNTs per channel. The second and a more deterministic approach uses self-aligned Cu-filled trenches formed in a photoresist (after Joule heating of the underlying CNT) to protect and obtain a large number of single CNT devices. Unlike electrical breakdown methods, which preserve the least conducting CNT and can leave behind CNT fragments, our approach allows the selection of the single most conducting metallic CNT from an array of as-grown CNTs with average resistance ∼14 times lower than that of as-fabricated single metallic CNTs. This method can also be used to select the best semiconducting CNT from an array and yields, on average, devices that are 15 times more conductive with 40 times higher ON/OFF ratio than those selected through electrical breakdown alone.



KEYWORDS: carbon nanotubes · aligned · electronic selection · individually addressable

High current density and high carrier mobilities[1,2] along with exceptional thermal[3,4] and mechanical[5−7] properties make single-walled carbon nanotubes (CNTs) attractive as both active[8] and passive[9] components of next-generation high-performance electronics. Among many envisioned applications, field-effect transistors (FETs),[10,11] nonvolatile memories,[12,13] and even integrated circuits[14−16] have been achieved with CNTs. However, despite their promise, challenges remain for developing CNT-based electronics, including achieving aligned arrays with predetermined periodicity, minimizing effects of variations in the surrounding environment,[17] and selecting the desired metallic or semiconducting electronic type.[18−20] While much progress addressing these issues has been made (*e.g.*, nearly perfect horizontal alignment *via* growth on quartz[21,22] and encapsulation to reduce surrounding induced electronic noise[23]), the presence of both metallic and semiconducting CNTs still remains one of the biggest roadblocks to electronics that take advantage of the nanometer dimension and high performance of individual CNTs. Progress in chirality-selective growth is being made but with limited success thus far.[24−28] Hence, most efforts currently focus on systems that utilize large arrays of CNTs as the active medium to reduce device-to-device variations that arise from the electronic heterogeneity,[29,30] despite the compromise in the ultimate performance and size limits. However, individually addressable CNTs are an attractive choice especially as molecular-scale electrical wires, switches, memories, and sensors at the limits of physical scaling.[31−33]

Electrical breakdown, when carefully performed, can reduce the number of CNTs spanning a pair of electrodes down to one, typically semiconducting with the largest band gap. However, this method selects the least conductive CNT in the channel, which leads to poor device performance. Preferentially selecting *metallic* CNTs by electrical

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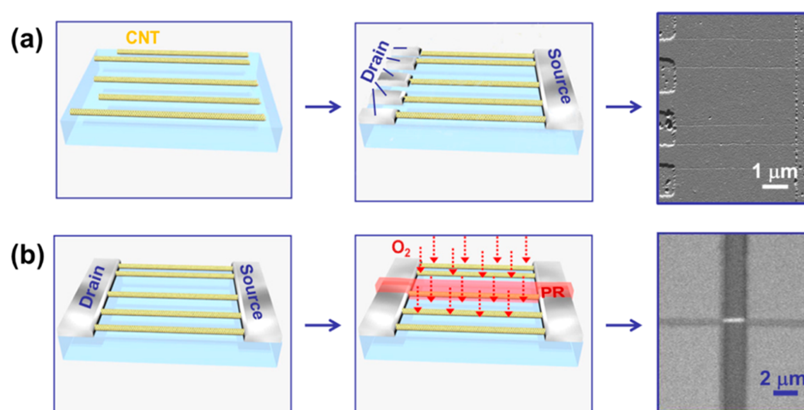

Figure 1. Schematics of controlling the average number of CNTs that span a pair of electrodes by (a) varying the width of the electrodes and (b) varying the width of photoresist strips for isolation *via* reactive ion etching. The right-most panel is an AFM (SEM) image of the fabricated devices for electrode width matching (isolation width matching).

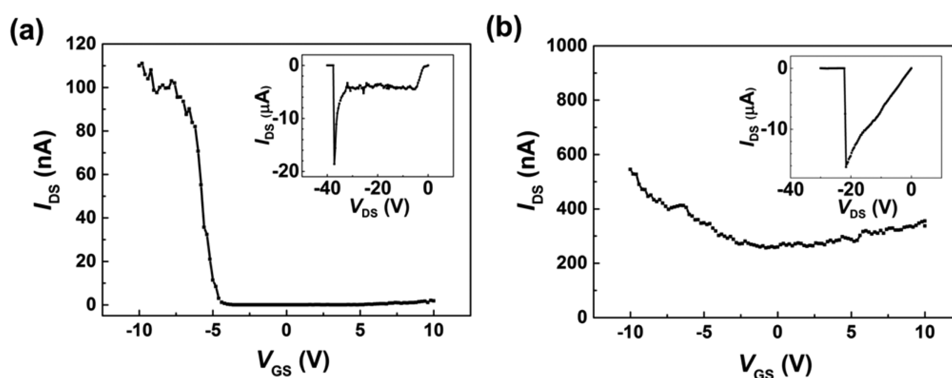

Figure 2. Gate dependence of the drain current of single semiconducting (a) and metallic (b) CNT devices. Insets show single breakdown events confirming that both devices had only one CNT connection. The semiconducting CNT shows a sharp current increase before breakdown, consistent with avalanche carrier multiplication.[37]

breakdown is, at the very least, difficult if not impossible since it is usually a semiconducting CNT in its OFF state that is the least conducting. Dielectrophoretic deposition[34−36] from a presorted CNT suspension is another method to achieve individually contacted CNTs, but the AC electric field frequency requirements, applicability to only short (less than ~1 μm) CNTs and the presence of surfactants and solvents, pose difficulties.

Here, we first examine the degree of control over the number of CNTs spanning a pair of electrodes simply by controlling the effective width of the metal contacts to match the average spacing of horizontally aligned CNTs. We then demonstrate a new approach to obtaining individually addressable CNTs through a self-aligned Cu etch mask process that takes advantage of Joule heating to form a trench[31] in the photoresist along the length of the most conducting CNT. A channel initially consisting of multiple CNTs with random electronic distribution can be converted to one metallic or one semiconducting CNT with the highest ON current.

RESULTS AND DISCUSSION

Controlling the Average Number of CNTs *via* Effective Channel Width. Since devices with multiple CNTs in parallel can be easily fabricated using horizontally aligned CNTs,[22] a high-yield approach that selects a desired number of CNTs within such a device could be a useful stepping stone to architectures that exploit unique aspects of individual or limited number of CNTs. Hence, we first consider the degree of control over the number of CNTs that span a pair of electrodes by optimizing the effective channel width by either electrode width or an additional isolation step as detailed in the Methods section. Figure 1 shows the schematic of the two equivalent processes along with postfabrication atomic force microscope/scanning electron microscope (AFM/SEM) images. Figure 2 shows examples of current *versus* gate voltage ($I_{DS}-V_{GS}$) characteristics of single CNT devices exhibiting semiconducting and metallic characteristics. The gate of our devices is the conducting Si substrate (see Methods section). Here and throughout this paper, we define a CNT or a device consisting of multiple CNTs to be metallic if the ON/OFF current ratio, $I_{MAX}/I_{MIN} < 10$, and the minimum current, $I_{MIN} > 100$ pA, at drain voltage $V_{DS} = 50$ mV within the gate voltage range of −15 V to +15 V. The ON/OFF ratio of the semiconducting CNT shown in Figure 2a is 1.13×10^5, and the field-effect mobility is ~1900 $cm^2/V \cdot s$. The resistance per unit length of the metallic CNT in Figure 2b is 333 kΩ/μm. The channel

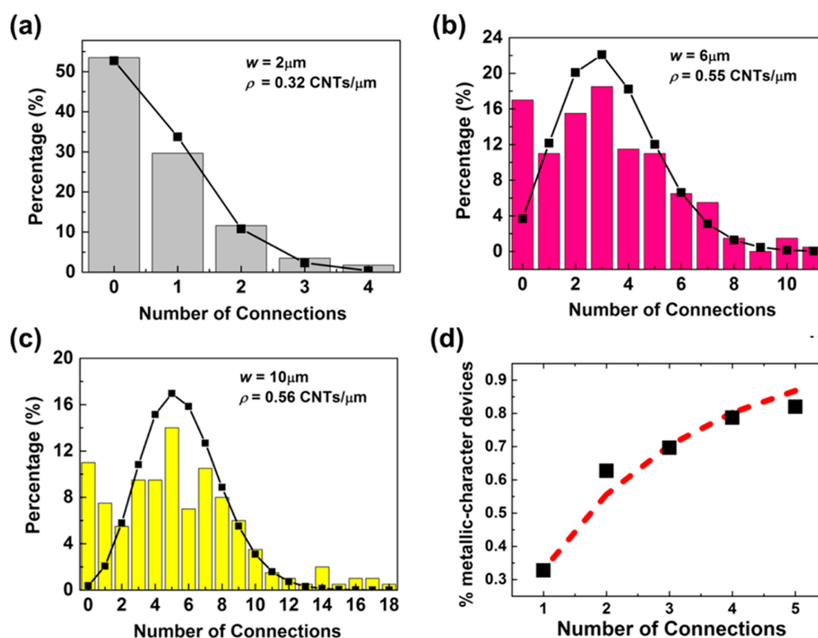

Figure 3. (a−c) Histograms of the number of connections of CNTs obtained by controlling the effective channel width as indicated. Fitting results using Poisson distribution (eq 1) with fixed channel width, *w*, and fitting parameter of CNT density, *ρ*, as indicated are also shown (experimental average *ρ* ∼ 0.5 CNT/*μ*m for all three cases). (d) Scaling of the percentage of devices exhibiting metallic behavior with the number of CNTs in the channel. The filled squares represent experimental values, and the dashed line represents the expected values based on the assumption that 1/3 of CNTs are metallic and that any metallic CNT in a channel makes the overall device behavior metallic.

length of the device examined here varies from 3 to 7 *μ*m. These characteristics are similar to individual CNT transistors that are fabricated without effective channel width control to optimize the average number of CNTs. Also shown in Figure 2 insets are the corresponding current *versus* drain voltage ($I_{DS}-V_{DS}$) measured up to electrical breakdown to ensure that the correct number of CNTs has been accounted for. For the metallic and semiconducting CNTs shown in Figure 2, each case shows a single breakdown event, indicating that a single CNT has been measured.

Even for CNTs grown on quartz that show nearly perfect horizontal alignment (*e.g.*, see Supporting Information, Figure S1), the control over the separation distance between CNTs is still lacking. When we assume random spacing between CNTs for a given average linear density *ρ*, the probability *P* of obtaining a certain number *N* of CNTs spanning a channel of controlled width *w* (either by fixing the electrode width or the isolation strip width) can be described by a Poisson distribution

$$P = \frac{e^{-\rho w}(\rho w)^N}{N!} \qquad (1)$$

Figure 3a−c shows that our experimental distributions for the cases optimized for $N = 1$, 3, and 5 connections follow this distribution very closely, and simply matching the effective channel width allows ∼30% yield of individually connected CNT devices (cf. 37% maximum statistical expectation).

In addition to the predictability of the average number of CNTs spanning a channel, controlling the effective channel width allows one to examine how maximum current and ON/OFF current ratio (*i.e.*, the semiconducting *vs* metallic character of the devices) scale with *N*. Assuming 1/3 of the CNTs to be metallic and that one or more metallic CNTs will cause the device to behave metallic, the percentage of devices with metallic behavior scales as $1 - (2/3)^N$. Figure 3d compares the expected percentage of devices exhibiting metallic character with experimental results. I_{MAX} *versus* I_{MIN} plots for 1, 3, and 5 CNT connections from which the experimental percentages are obtained are shown in the Supporting Information (Figure S2). The devices quickly exhibit metallic behavior with increasing number of CNTs. Even with only two CNTs per channel, over 50% of the devices behave metallic. At five CNTs per channel, 78% of the devices exhibit metallic behavior. These results should provide useful scaling trends in developing few-CNT-based FETs, interconnects, sensors, and related applications, especially for variation-tolerant architectures.[16]

Self-Aligned Cu Etch Mask for Selecting the Most Conductive Individual CNTs. The next challenge addressed here, which is perhaps one of the most difficult ones yet to be tackled, is the selection of the single most conducting CNT (often metallic or large-diameter semiconducting) from an array of multiple CNTs of both metallic and semiconducting character that span a pair of electrodes. Obviously, the above method of controlling the effective

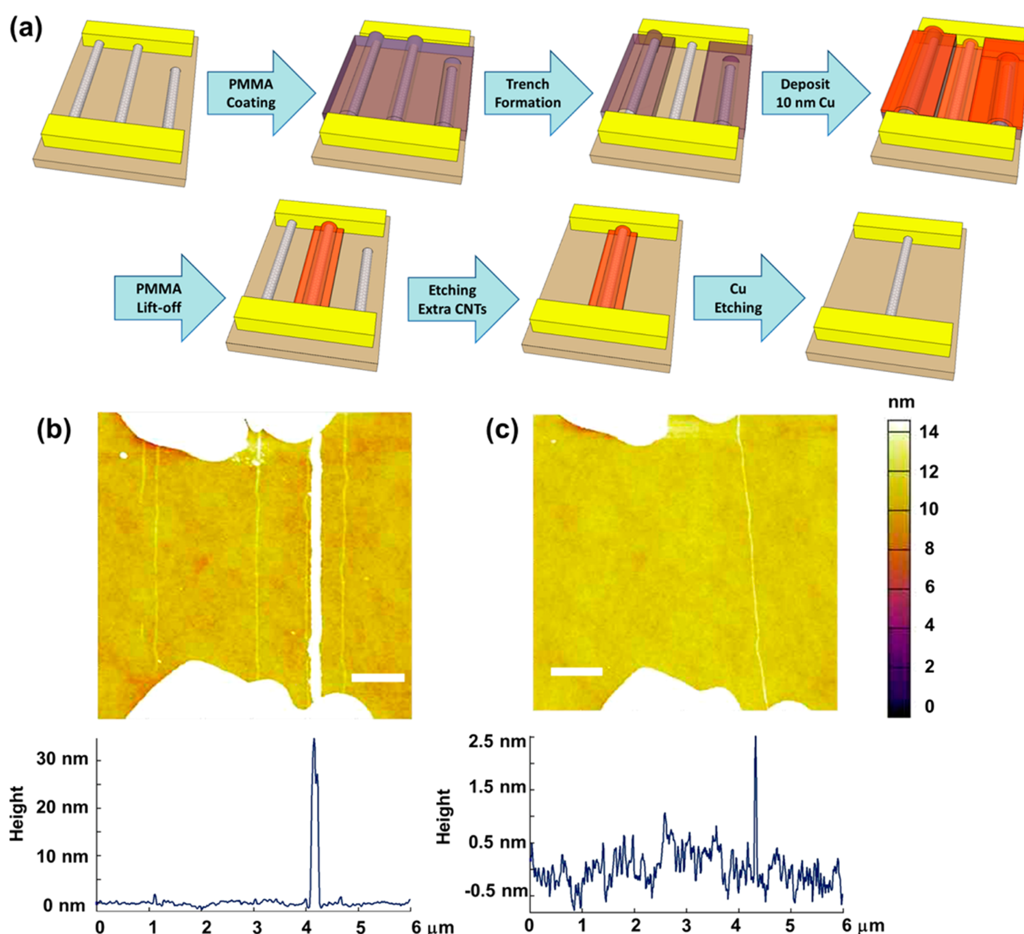

Figure 4. (a) Schematic describing the fabrication process leading to a single CNT device *via* self-aligned Cu etch mask. AFM images and the corresponding height profiles of the Cu nanowire covering the selected CNT after lift-off (b) and the one remaining CNT after reactive ion etching and Cu etching (c). The scale bars are 1 μm.

channel width to match CNT density leads to a random distribution of characteristics, and therefore a more deterministic approach is needed. Electrical breakdown, by design, removes the most conducting CNTs first and therefore cannot be used to select metallic CNTs let alone the most conducting ones. Dielectrophoretic deposition has limitations including the need for surfactants that can increase contact resistance and has been shown to be applicable mostly to relatively short CNTs.[38] The latter problem can be significant if considering the use of metallic CNTs for applications such as interconnects.

Our new approach exploits the ability to thermally form a "trench" within a thin film of poly(methyl methacrylate) (PMMA) by Joule heating the underlying CNTs,[31,39] as shown in Figure 4. When current is passed through a device with multiple CNTs, the most conducting CNT reaches the highest temperature first, opening a trench in the PMMA surrounding it and therefore providing physical access for further manipulation. Unless otherwise noted, the devices were kept in vacuum during the trench formation process. Subsequent deposition of Cu and PMMA lift-off led to a Cu nanowire that self-aligns with the most conducting CNT within the array. The exposed and less conducting CNTs are etched by an O_2 plasma, while the Cu nanowire protects the most conductive CNT. The AFM height profiles in Figure 4b,c show that the Cu mask is ~30 nm in height and the remaining CNT (after Cu etching) is ~2 nm in diameter, suggesting there is no significant Cu residue after its removal. Note that in Figure 4b there is a CNT very close to the Cu nanowire (within ~100 nm), indicating that our self-aligned Cu etch mask approach can be effective with high spatial resolution and high density of CNTs. While the choice of Cu here is due to simple and well-known solution chemistry for its removal and for it being the primary choice for interconnects in electronics, our approach is applicable to other materials, as well (*e.g.*, in a previous study,[31] $Ge_2Sb_2Te_5$, Au, and HfO_2 nanowires were also formed self-aligned with CNTs).

The electrical characteristics of a metallic CNT device before and after the self-aligned Cu nanowire etch mask process are shown in Figure 5. The transfer characteristics of the original multiple CNT device exhibits slight gate voltage dependence, indicating the presence of some semiconducting CNTs in the channel. During Joule heating, the most conductive CNT forms a

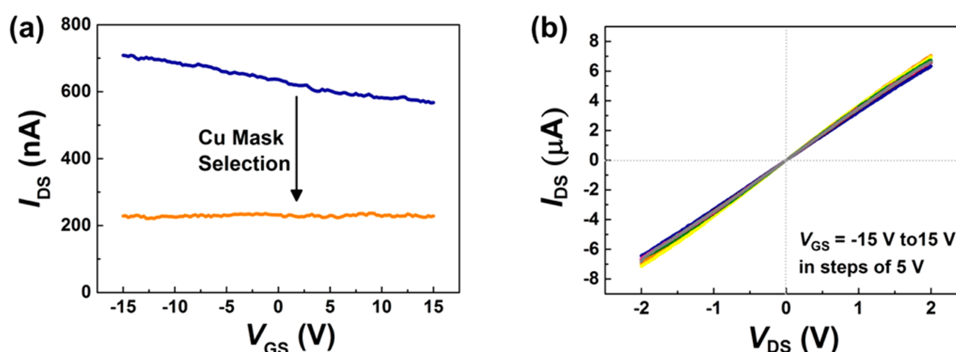

Figure 5. (a) Gate dependence of drain current of a device (channel length = 4 μm) before and after the self-aligned Cu etch mask process to select the most conductive individual metallic CNT (V_{DS} = 50 mV). (b) Current *vs* voltage characteristics of the selected single metallic CNT at various gate voltages.

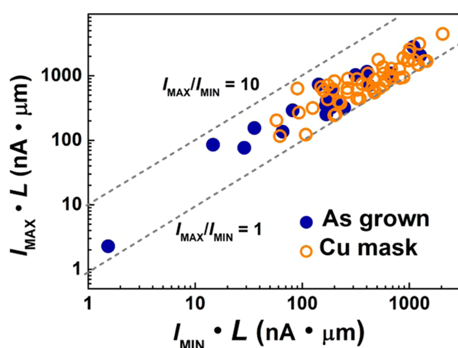

Figure 6. Comparison between single-connection metallic CNT devices selected by the self-aligned Cu etch mask approach and those as-fabricated (current is normalized to channel length L = 3, 4, or 7 μm). For all data points, V_{DS} = 50 mV. The self-aligned Cu etch mask process leads to the selection of the most conducting metallic CNT in a given channel.

trench in the PMMA first due to the highest current flow. By controlling the applied bias across the channel while applying positive gate voltage to turn off semiconducting CNTs, the trench formation can be limited to a single metallic CNT. Then Cu is only selectively deposited on the most conductive metallic CNT. Figure 5a shows the gate dependence of the device before and after the selection process, and Figure 5b depicts the $I_{DS}-V_{DS}$ characteristics of the selected single metallic CNT. Gate voltage dependence is eliminated, while the current remains reasonably high.

Figure 6 compares the distribution of I_{MAX} and I_{MIN} of 54 metallic CNTs selected by the self-aligned Cu mask process with those of 22 as-fabricated metallic CNTs (without going through the Cu etch mask selection process) that were identified as having a single CNT connection. Our single metallic CNT selection process leads to a significantly higher percentage of CNTs with larger I_{MAX} and I_{MIN}. The average resistance normalized by length (corresponding to I_{MAX}) of Cu etch-mask-selected metallic CNT devices is 98 kΩ/μm, whereas that of the as-fabricated CNTs is 1379 kΩ/μm. Furthermore, the unchanging Raman D/G band intensity ratio (Supporting Information, Figure S3) and the similar current level of a singly connected CNT (Supporting Information, Figure S4) before and after the Cu etch mask process verify that no noticeable damage was induced. These results demonstrate not only that the most conducting metallic CNTs can be selected but also that their performance can be preserved by our new self-aligned Cu etch mask process.

Comparison to Finite Element Model. In order to investigate the temperature profile in our devices and the minimum power required for the trench formation process, we have developed a finite element model (FEM) using a commercial package (COMSOL Multiphysics). Our three-dimensional (3D) simulation platform is consistent with the experimental setup and self-consistently takes into account the electrical, thermal, and Joule heating interactions. Simulation parameters including electrical resistivities, thermal conductivities, thermal boundary resistances, and electrical contact resistances have been reported in detail elsewhere.[31] Figure 7a shows a typical cross-sectional temperature profile of the plane that bisects the CNT in the middle. The trench is formed at locations where the PMMA temperature reaches beyond its boiling point (~523 K), as shown in the void region in Figure 7a. Figure 7b shows the sharp temperature profile along the lateral direction with a peak temperature gradient of ~1.6 K/nm. This confirms that the CNT heater could provide highly localized temperature profile and form a nanoscale trench. Our electro-thermal simulation indicates that, for a 2.5 μm long CNT device, the input power (excluding power dissipation at the contacts) should be >410 μW (>163 μW/μm) to facilitate trench formation at 110 °C, which is the substrate temperature used in the experiments and close to the glass transition temperature of PMMA.

In order to compare to this expected power requirement, we have monitored the trench formation under an optical microscope with a 100× objective. For convenience, a blanket of Ar gas was flown over the samples (to limit CNT oxidation) instead of conducting the experiments in vacuum. The voltage across a device with multiple parallel CNTs was swept from 0 V at a

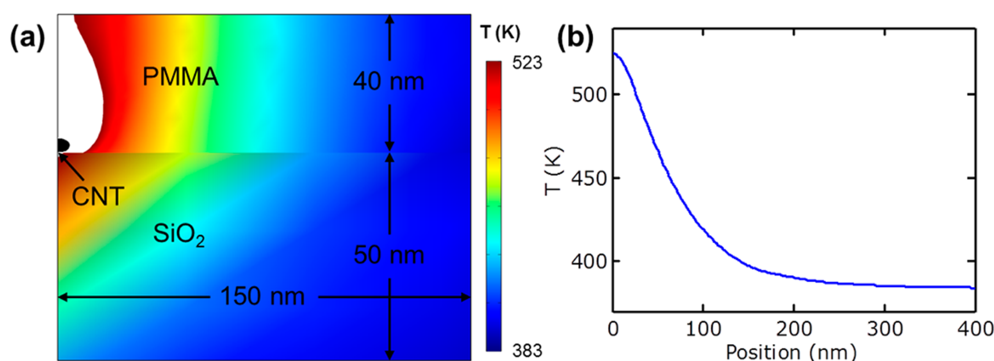

Figure 7. Simulation results from finite element model. (a) Cross-sectional temperature profile in the middle of the CNT channel with input power 163 μW/μm. The void region on the left corresponds to the trench in PMMA, set as the domain where the PMMA boiling temperature is exceeded. The CNT is drawn disproportionally large for clarity. (b) Temperature profile of the PMMA top surface shows that heating is highly localized near the CNT with a temperature gradient of ~1.6 K/nm. The substrate temperature was set to 383 K (=110 °C).

rate of 62 mV/s and removed once a complete trench was observed to form under the microscope. The measured voltage and current at this stage provide total input power. We note that although trench widths are on the order ~50 nm, they are conveniently visible under an optical microscope due to sufficient light interference.[31] After the trench formation, electrical breakdown of the exposed CNTs was performed in order to estimate the resistance of the CNT that formed the PMMA trench (*i.e.*, by measuring the resistance of the remaining CNTs). Assuming the ratio of the resistance of the CNT that formed the trench to that of other CNTs in the channel remains the same in the linear and the saturation regimes, we can separate out the power dissipation from the particular CNT that formed the trench (*i.e.*, the power necessary for evaporating the surrounding PMMA) from the measured total input power. The power needed for trench formation calculated from these experiments ranges from 400 to 800 μW for CNTs with 2.5 μm channel length (160 to 320 μW/μm) which agrees very well with the FEM results.

Extension of Self-Aligned Etch Mask Approach To Selecting Most Conductive Individual Semiconducting CNTs. By combining our self-aligned Cu nanowire etch mask process and electrical breakdown, individual semiconducting CNTs of the highest ON currents can also be obtained. First, the metallic CNTs can be eliminated by electrical breakdown under a large positive gate voltage (which turns off the semiconducting CNTs). Then, the self-aligned Cu etch mask can be applied in the same manner as the metallic CNT case to select the most conductive semiconducting CNT in each channel. The transfer characteristics of a semiconducting CNT device before and after the selection process are shown in Figure 8. The former curve is before Cu etch mask selection but after electrical breakdown to remove metallic CNTs. While the I_{MAX} decreases only by ~15% (from 71.1 to 60.3 nA), the ON/OFF ratio increases by 2 orders of magnitude (from ~2 × 10^3 to ~2 × 10^5).

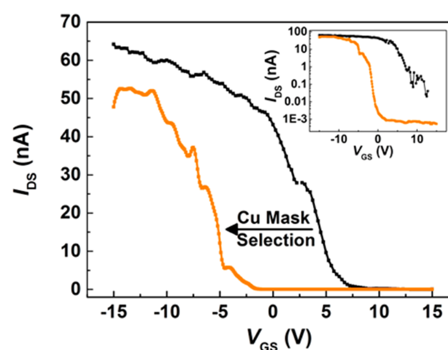

Figure 8. Transfer characteristics of a semiconducting CNT device (channel length = 4 μm) before and after the self-aligned Cu etch mask selection process. The resulting individual semiconducting CNT is the most conducting one in its ON state.

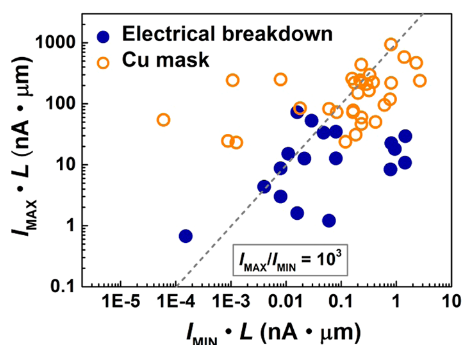

Figure 9. Comparison of ON and OFF currents of single CNT devices obtained by electrical breakdown and by the self-aligned Cu mask process. For all data shown, V_{DS} = 50 mV and channel length L = 3 or 4 μm.

While single-connection semiconducting CNTs can be obtained by electrical breakdown alone, that is, breakdown until there is only one CNT left in the channel, the combination of electrical breakdown and self-aligned Cu mask process leads to much improved characteristics as exemplified by the I_{MAX} *versus* I_{MIN} distribution in Figure 9. Compared to the single-connection devices obtained from electrical

breakdown alone, which preserves the least conductive CNT in the channel, individual semiconducting CNTs selected by our self-aligned Cu etch mask process have ~15 times higher I_{MAX} on average, while maintaining similar range of minimum currents. The average ON/OFF ratio of the devices selected from the self-aligned Cu etch mask is ~2.2×10^5, which is ~40 times higher than that of the CNTs obtained from electrical breakdown alone (~5.6×10^3). Furthermore, our self-aligned Cu etch mask process physically removes the entirety of undesired CNTs (after the etching step), whereas electrical breakdown leaves large CNT fragments in the channel, typically connected to one of the source or drain electrodes. The latter can limit applicability in transistors, sensors, or memory devices.[11,12,16,32,40,41]

CONCLUSIONS

We have demonstrated a simple and efficient method for obtaining a large number of high-performance single-connection CNT devices *via* a self-aligned Cu nanowire etch mask process, applied to as-grown parallel CNT arrays. This method can be performed to fabricate individual CNT devices of desired metallic or semiconducting character. In addition to the selectivity for single metallic CNTs, which is difficult to achieve by any other process, our approach leads to the selection of the most conducting CNTs for both metallic and semiconducting cases. We have also shown that optimizing the effective electrode width with respect to the CNT density can provide single CNT devices with yields approaching the statistical limit for random CNT separation distances, and as the number of CNTs per channel increases, net metallic behavior quickly dominates. The two approaches to controlling the number of CNTs examined here provide complementary insights that can facilitate the development of deterministic means to obtaining the highest performance semiconducting and metallic CNTs with single CNT precision.

METHODS

Horizontally aligned CNTs were grown by chemical vapor deposition on ST-cut quartz (Hoffman Materials) using ferritin (Sigma-Aldrich) as catalyst and CH_4 as carbon source.[42] Aligned CNTs grown on quartz were transferred onto SiO_2 (300 nm)/p^{++} Si substrates (resistivity = 0.005 Ω·cm) in order to characterize the electrical properties using the back gate.[43] Lithographically patterned metal pads (2 nm Ti and 25 nm Pd) were deposited by electron beam evaporation to define the contact electrodes (channel lengths were 2, 3, 4, or 7 μm). The CNTs in the channel areas were then covered by a photoresist (AZ 5214), and CNTs outside this region were etched by O_2 plasma to isolate the devices. After removing the photoresist in acetone, rinsing with acetone/isopropyl alcohol, and drying under N_2 flow, devices were annealed at 400 °C under 500 cm^3/min each of Ar and H_2 flow for 1 h to ensure good contact between the metal pads and the CNTs. The resulting devices had multiple CNTs in the channel.

In order to obtain, on average, a desired number of CNTs per channel, isolation patterns that matched the CNT density were lithographically introduced and reactive ion etching was carried out. For example, for a desired average of 1 CNT per channel for a substrate having an average CNT density of ~0.5 CNTs/μm, isolation stripes of 2 μm width were used. Similarly, for other desired average number of CNTs per channel, larger strip widths were used (*e.g.*, 6 μm for average of 3 CNTs, 10 μm for average of 5 CNTs per channel for CNT density of ~0.5 CNTs/μm). Equivalently, the width of the metal electrodes can be optimized to obtain a controlled average number of CNTs (*e.g.*, 2, 6, and 10 μm electrode widths for 1, 3, and 5 CNT connections on average per channel for same density of CNTs as striping method).

For a more deterministic approach to achieving individually contacted metallic CNTs, the following self-patterning and etching steps were carried out. Multi-CNT devices were first fabricated from substrates with CNT density between ~0.5 and 1.5 CNTs/μm, similar to the electrode width optimization described above using 4 μm channel width. This channel width then leads to, on average, ~4 CNTs/device, but the actual number varies from 0 to a little over 10 CNTs/device. Self-aligned nanotrenches were then formed by spin-casting ~50 nm of PMMA (495A2MicroChem) onto the multi-CNT devices at 4500 rpm for 30 s and baking at 200 °C in air on a hot plate for 2 min. Subsequent Joule heating of the CNTs[31] was carried out in vacuum (4×10^{-5} Torr) using Keithley 4200 semiconductor characterization system with substrate temperature of 90 °C for metallic CNT devices and 110 °C for semiconducting CNT devices. A gate voltage (V_{GS} = 40 V for selecting metallic CNTs and V_{GS} = −40 V for selecting semiconducting CNTs) was applied to assist the formation of nanotrenches. For visual inspection, trench formation was carried out under a blanket of Ar under an optical microscope with a 100× objective. Without observing trench formation process to optimize the power during the experiment, 78 of 96 devices examined formed at least one trench and 70% of those formed a single trench in the PMMA when V_{DS} was ramped up until 500 μW/μm was reached. Cu thin film with thickness of 10 nm was then deposited by electron beam evaporation with ~0.1 Å/s deposition rate. Lift-off was performed by placing the sample in a 60 °C acetone bath overnight, which led to Cu nanowires surrounding the CNTs. O_2 plasma (10 mTorr, 1 cm^3/min O_2, 25 W, 20 s) was used to remove all CNTs not protected by the Cu nanowires. Subsequently, the Cu nanowires were etched away using 0.1 M ammonium persulfate solution.[44] Individual semiconducting CNT devices were obtained by the same process with an additional electrical breakdown step to first remove the metallic CNTs. Postmeasurement electrical breakdown was carried out to ensure the number of CNTs for a given pair of metal contact pads.

All postfabrication electrical measurements were carried out in air with an Agilent 4156C semiconductor parameter analyzer. Raman spectra were collected on Jobin-Yvon Labram HR800 using a 100× air objective with 633 nm laser excitation source. The laser spot size was ~1 μm, and the power was kept under 1 mW. AFM images were obtained with Asylum Research MFP-3D AFM. SEM images were obtained with Hitachi S4800 high-resolution SEM.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: SEM image of aligned CNTs, statistics of maximum current *vs* minimum current for 1, 3, and 5 CNTs per channel, Raman spectra of a CNT before and after the Cu etch mask process, and gate dependence of drain current of a device with only one CNT before and after the Cu etch mask process. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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Supporting Information for

Self-Aligned Cu Etch Mask for Individually Addressable Metallic and Semiconducting Carbon Nanotubes

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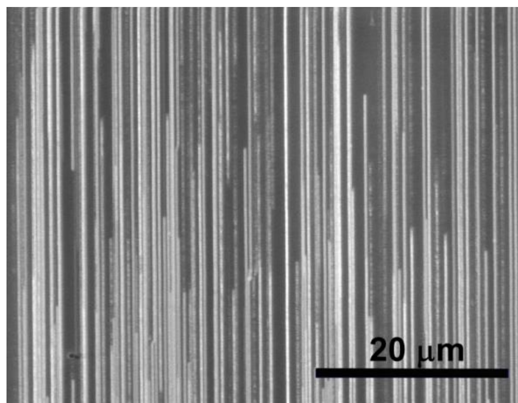

Figure S1. SEM image of aligned CNTs grown on a single crystal quartz substrate.

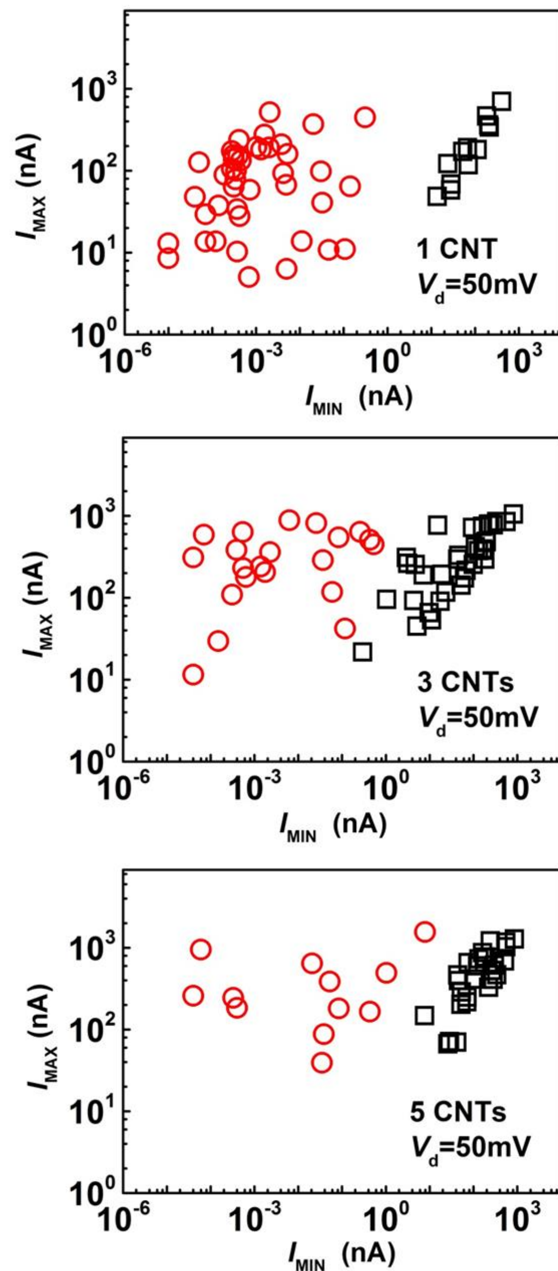

Figure S2. Maximum current *vs.* minimum current for 1, 3 and 5 CNTs per channel as indicated. The red circles represent semiconducting CNTs, and black squares represent metallic CNTs as defined in the main text.

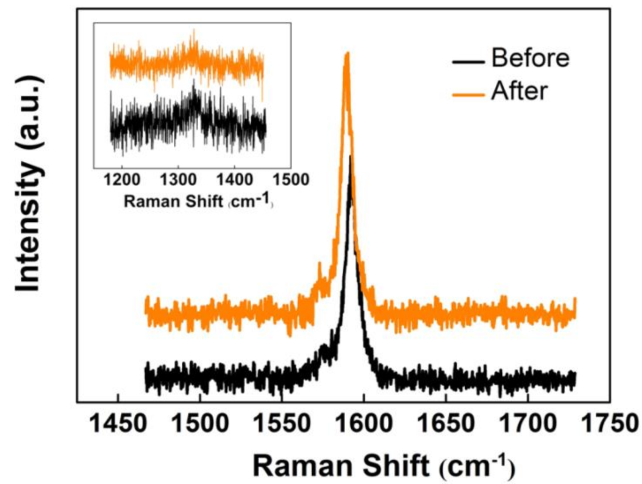

Figure S3. Raman spectra of a CNT before and after the Cu mask process for selecting the most conductive metallic CNT. Inset is the D-band region indicating that there is no significant change in the degree of disorder.

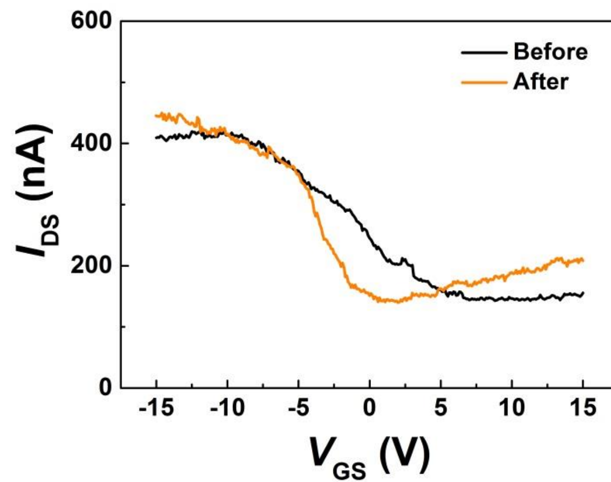

Figure S4. Gate dependence of drain current of a device with only one CNT before and after the self-aligned Cu etch mask process.