Electro-Thermal Confinement Enables Improved Superlattice Phase Change Memory

Asir Intisar Khan, *Graduate Student Member, IEEE*, Heungdong Kwon, Michelle E. Chen, Mehdi Asheghi, *Member, IEEE*, H.-S. Philip Wong, *Fellow, IEEE*, Kenneth E. Goodson, *Fellow, IEEE*, and Eric Pop, *Fellow, IEEE*

***Abstract*— Large switching current density and resistance drift remain challenges for phase change memory (PCM) in data storage and neuromorphic computing applications. Here, we address these by electro-thermal and structural confinement in a GeTe/Sb_2Te_3 superlattice PCM (SL-PCM) with thermally-induced phase change, while observing scalability with bottom electrode diameter. We demonstrate ~8-10× reduction of reset current density (J_{reset}) and ~25-30× reduction of power (P_{reset}) in our mushroom cell SL-PCM compared to control $Ge_2Sb_2Te_5$ (GST) PCM with the same device structure. The SL-PCM devices also exhibit multi-level states with ~10× lower resistance drift compared to control GST PCM. Material characterization and electro-thermal simulations confirm the role of heat confinement in SL-PCM, paving the way towards low-power, high-density memory and data storage.**

***Index Terms*— Phase change memory, electro-thermal confinement, reset current density, low resistance drift.**

I. Introduction

PHASE change memory (PCM) is a non-volatile data storage technology for both digital memory [1] and brain-inspired computing [2], [3]. PCM encodes data within the resistance of a phase change material, like $Ge_2Sb_2Te_5$ (GST), between a top and bottom electrode (TE and BE). Reversible phase change between amorphous (high-resistance state, HRS) and crystalline (low-resistance state, LRS) states is realized using resistive heating induced by the BE. However, a challenge of PCM is its large switching current density [1] and its resistance drift due to structural relaxation [4] or atomic diffusion [5], [6] in the phase change material.

To address these challenges, researchers have proposed so-called interfacial or superlattice (SL) PCM, which rely on alternating thin layers of chalcogenide films. Earlier efforts [7]–[9] suggested that Ge atom movement leads to resistance change in GeTe/Sb_2Te_3 SL-PCM and the switching current is lowered due to a crystalline-to-crystalline phase transition, unlike the thermally-driven phase transition in conventional PCM. However recent efforts [10]–[13] pointed to the possibility of thermally-driven switching, due at least in part to electro-thermal confinement in SL-PCM being enhanced compared to conventional (e.g. GST-based) PCM. In this context, high-resolution imaging of well-cycled GeTe/Sb_2Te_3 SL-PCM in both LRS and HRS is required. Moreover, the resistance drift, multi-level capability, and scalability of such SL-PCM devices have not been explored yet. Additionally, electrical and thermal measurements of SL films and subsequent electro-thermal modeling of the memory cells can shed insight into the switching mechanism of such SL-PCM.

Here we show that reset current density (J_{reset}) and resistance drift are simultaneously reduced by controlling vertical heat loss and atomic diffusion (or structural relaxation) within a GeTe/Sb_2Te_3 superlattice. We achieve large reduction of both J_{reset} and P_{reset} in our mushroom cell SL-PCM vs. control GST devices, demonstrating multi-level memory with four stable resistance states and low drift. We also obtain high resolution scanning transmission electron microscopy (HR-STEM) images of well-cycled SL-PCM devices, both in LRS and HRS. These reveal van der Waals (vdW) interfaces in the SL, which facilitate electro-thermal and structural confinement, enhancing the heating efficiency in our SL-PCM. This is further supported by our separate electro-thermal measurements in such SLs [14] and electro-thermal simulations described below. Taken together, these unique findings and analysis confirm a strong electro-thermal component in our SL-PCM, driving its energy-efficient switching.

II. Device Fabrication and Characterization

Fig. 1(a) shows the schematic of a mushroom-cell SL-PCM device with the superlattice phase change material [7] made of 12 periods of alternating Sb_2Te_3 (4 nm) and GeTe (1 nm) layers on a TiN BE. Prior to the deposition of the SL, the BE surface was cleaned *in situ* by Ar etching to remove any native oxide. Then a ~3 nm thick Sb_2Te_3 layer was sputtered at room temperature (RT) followed by *in situ* annealing at ~180°C. Next, alternating layers of GeTe and Sb_2Te_3 were sputtered at ~180°C, total thickness of the phase change stack being ~60 nm. Then we capped the stack *in situ* with 10 nm TiN to protect it from oxidation. Next, we patterned and etched the device region followed by the top electrode (additional 20 nm TiN and 50 nm Pt).

Fig. 1(a) also embeds an HR-STEM cross-section of the SL taken on a Si substrate, deposited with the same process conditions as for the fabricated SL-PCM

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Asir Intisar Khan, H.-S. Philip Wong, and Eric Pop are with the Department of Electrical Engineering, Stanford University, Stanford, CA 94305 USA (e-mail: epop@stanford.edu).

Heungdong Kwon, Mehdi Asheghi, and Kenneth E. Goodson are with the Department of Mechanical Engineering, Stanford University, Stanford, CA 94305 USA.

Michelle E. Chen is with the Department of Materials Science and Engineering, Stanford University, Stanford, CA 94305 USA.

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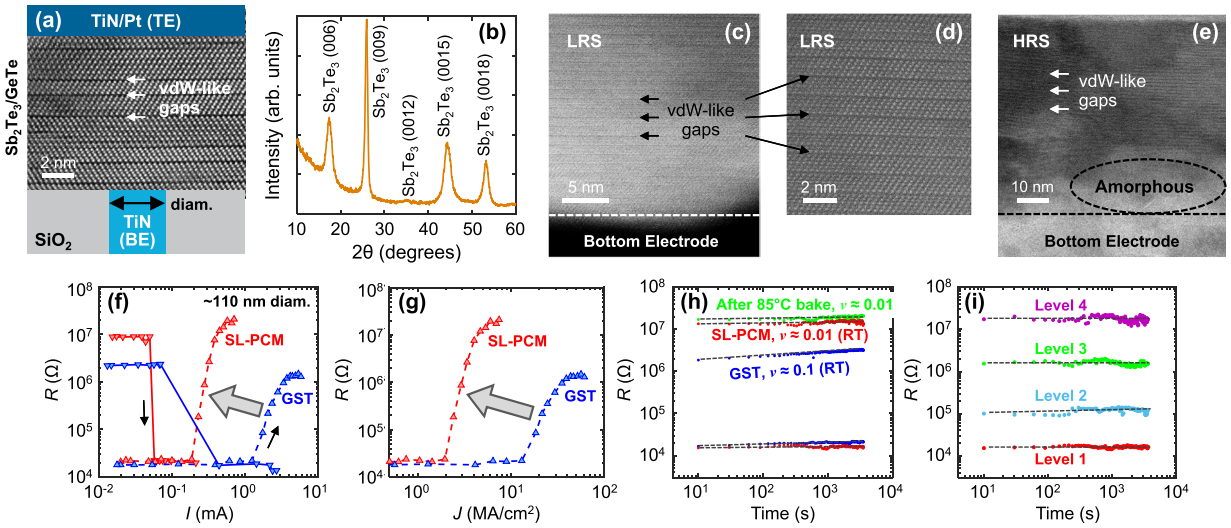

Fig. 1. **Device Structure and Characterization:** **(a)** Schematic of mushroom PCM with Sb_2Te_3 and GeTe superlattice (SL), inset with HR-STEM cross-section of the SL. **(b)** X-ray diffraction of the SL stack. **(c)** STEM of region near BE of SL-PCM device in the low-resistance state (LRS), after 8000 cycles. **(d)** Higher-resolution zoomed-in version of (c). **(e)** STEM of representative region showing SL layers near the BE in the high-resistance state (HRS), after 10^6 cycles. DC read resistance vs. **(f)** current and **(g)** current density showing up to ~10× reduction of the reset current and current density in SL-PCM devices vs. control devices with conventional GST (both ~110 nm BE diameter). Small arrows show measurement direction, from HRS to LRS and from LRS to HRS. **(h)** Resistance drift at room temperature (RT) in well-cycled SL-PCM (red) and control GST devices (blue). Drift measurement is repeated after 85°C bake for 30 min, followed by one more set/reset (green). v is the resistance drift coefficient fit with dashed lines using $R \propto t^v$, where t is time. **(i)** Four stable resistance states in our SL-PCM devices showing multi-level capability.

devices. The image shows a representative region of the SL layers revealing vdW-like gaps. Some mixed $Ge_xSb_yTe_z$ phase is observed due to stacking faults and local diffusion of Ge atoms into Sb_2Te_3. The x-ray diffraction data in **Fig. 1(b)** show sharp (poly)crystalline peaks from the same SL stack. HR-STEM images of representative regions of SLs near the BE in our devices at LRS after 8000 cycles [**Fig. 1(c)** and **1(d)**] and at HRS after 10^6 cycles [**Fig. 1(e)**] also reveal vdW-like interfaces. Additionally, the appearance of an amorphous region in the HRS indicates a thermally-driven phase change within our SL-PCM devices.

For set and reset programming of SL-PCM devices, we use 1/20/200 ns and 1/20/1 ns rise/width/fall pulses, respectively, with a setup previously described [15]. The set programming of the SL-PCM requires longer (>70 ns) fall times, also suggesting a thermally-driven phase change [10].

III. Results and Discussion

Fig. 1(f) displays resistance (R) vs. current (I) measurements for devices with ~110 nm BE diameter, showing nearly an order of magnitude lower I_{reset} for SL-PCM vs. our control GST devices. The estimated J_{reset} [**Fig. 1(g)**] for our mushroom SL-PCM devices is ~2.5–3 MA/cm^2, ~8-10× lower than control GST devices (~20 to 25 MA/cm^2) (also see the benchmarking below).

The J_{reset} reduction in our SL-PCM devices is attributed to electro-thermal confinement due to the presence of vdW interfaces. Our separate transport measurements of SL films [14] revealed low cross-plane thermal conductivity and highly anisotropic electrical resistivity of the SL stack. These properties enhance heating efficiency in SL-PCM devices by limiting heat loss into the BE and enable electro-thermal confinement [12] which is further explored through simulation below.

We note that reset pulses lead to partial amorphization near the BE of our SL-PCM devices [**Fig. 1(e)**]; however, the SL layers above and surrounding remain crystalline. These regions may act as a template to reconstruct the SL region (which went through melt-quench) near the BE [11], [16]. Thus, the heating efficiency in SL-PCM is maintained upon switching back and forth because the vdW interfaces can be maintained.

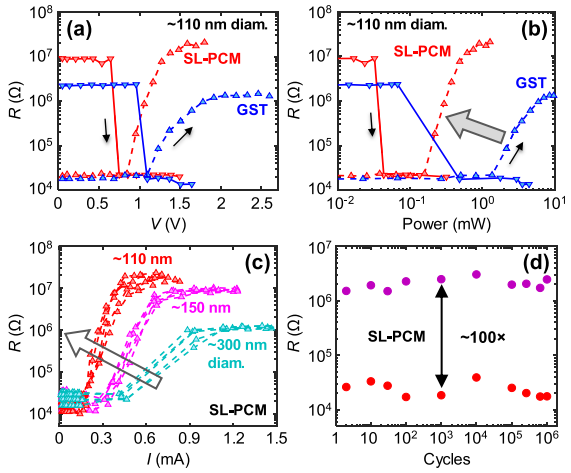

Fig. 2. **Electrical Analysis:** DC read resistance vs. **(a)** voltage and **(b)** power for SL-PCM and control GST devices with ~110 nm BE diameter. P_{reset} is reduced by >30× for SL-PCM. Small arrows show measurement direction, from HRS-LRS and from LRS-HRS. **(c)** I_{reset} reduction with BE diameter across multiple SL-PCM devices. **(d)** ~100× resistance ratio of SL-PCM maintained for >10^6 cycles, measured in a ~110 nm BE diameter device with 1.1 V, 1/20/1 ns (reset) and 0.7 V, 1/20/200 ns (set) pulses, using a write-verify scheme.

The vdW-like gaps in the SL also limit ionic migration [10], which helps maintain a higher on/off ratio in SL-PCM vs. control GST devices. We also note that strong electro-thermal confinement relies on the realization of SL layers with sharp vdW-like interfaces using an optimized set of process parameters [17]–[19]. Non-optimized SL deposition can lead to void formation [20] or Te segregation [21].

Fig. 1(h) shows ~10× lower resistance drift with coefficient $v \approx 0.01$ in our SL-PCM devices vs. control GST PCM ($v \approx 0.1$, typical for undoped GST [22]), both devices

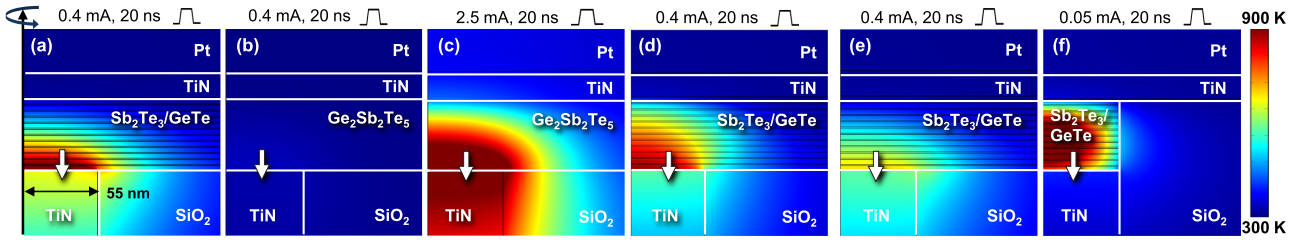

Fig. 3. **Electro-thermal simulations:** Temperature distribution in our **(a)** mushroom cell superlattice (SL) PCM, same as the fabricated structure in Fig. 1(a), and **(b)** control GST PCM mushroom cell, both at the end of 0.4 mA, 20 ns current pulses, and **(c)** control GST PCM mushroom cell at the end of a 2.5 mA, 20 ns current pulse, demonstrating the effect of thermal confinement from SL layers. Heat confinement for the mushroom cell SL-PCM structure at the end of 0.4 mA, 20 ns current pulse: **(d)** with thermal properties of SL-PCM and electrical properties the same as GST, and **(e)** with electrical properties of SL-PCM and thermal properties the same as GST. **(f)** A confined cell SL-PCM reaches similar temperature as the mushroom cell in (a) even at the end of a 50 μA, 20 ns current pulse. All simulations have BE (TiN) diameter of 110 nm. Note that the left edge is the axis of cylindrical symmetry and the vertical and horizontal scales are unequal. White block arrows show the direction of current flow.

well-cycled ($>10^4$ cycles). The lower drift in SL-PCM can be attributed to reduced atomic diffusion due to the vdW interfaces [5], [6], [23] and/or less structural relaxation in a smaller amorphous dome [**Fig. 1(e)**]. The low resistance drift also enables multi-level capability in SL-PCM. **Fig. 1(i)** shows four stable resistance states with low drift, achieved using several reset pulses of increasing amplitude (0.5 V to 1.3 V).

More electrical measurements reveal 25-30× lower P_{reset} [calculated from R vs. I in **Fig. 1(f)** and R vs. voltage (V) in **Fig. 2(a)**] in SL-PCM compared to control GST devices [**Fig. 2(b)**]. **Fig. 2(c)** shows I_{reset} scales with BE diameter of multiple well-cycled SL-PCM devices, with improved heating efficiency for the smaller diameters, as evident from the steeper slopes. We recall that the mushroom cell geometry has significantly anisotropic current flow, so the in-plane resistivity (which is up to 10× lower for SL-PCM than for GST [14]) makes a significant contribution. Thus, SL-PCM displays less scaling of LRS with different BE diameters [11], compared to GST PCM devices [15] where current flow is more uniform. In **Fig. 2(c)** the LRS is also influenced by cycle-to-cycle and device-to-device variation (e.g. of BE heater or SL resistivity) [11]. **Fig. 2(d)** shows that ~100× resistance on/off ratio is maintained for $>10^6$ cycles.

To gain insight into the role of thermal and spatial confinement in SL-PCM, we performed coupled electro-thermal simulations [24] (**Fig. 3**). These simulations include our measured cross-plane thermal conductivity of the SL ($k \approx 0.38$ W/m/K), thermal boundary resistance at TiN/SL interfaces (upper bound TBR ~ 52 m^{2}K/GW) as well as measured in-plane (5.8×10^{-4} Ω·cm) and cross-plane (1.1 Ω·cm) electrical resistivities of the SL [14]. To incorporate the thermoelectric effect, we use temperature-dependent Seebeck coefficients of Sb_2Te_3[25], GeTe [26] and TiN [27]. The simulation details for control GST PCM were described in Ref. [28].

Figures 3(a,b) show the temperature (T) profiles computed in the mushroom-cell SL-PCM and GST PCM at the end of a current pulse (0.4 mA, 20 ns), revealing significantly higher heat confinement and peak T ~ 900 K in the SL-PCM vs. the GST PCM (~322 K). Additionally, the control GST PCM would require much larger current (~2.5 mA) to reach the same peak temperature [**Fig. 3(c)**] as the SL-PCM, for the same BE diameter (here 110 nm). **Fig. 3(d)** and **Fig. 3(e)** show simulations of SL-PCM devices including thermal (electrical) properties of the SL while keeping the electrical (thermal) properties the same as GST. The peak temperatures reached are ~785 K and ~645 K, respectively, indicating that the SL thermal properties play a stronger role for heat confinement than the electrical properties, in mushroom cells. We also find that electro-thermal confinement in SL-PCM can be further enhanced using a confined cell structure [**Fig. 3(f)**], projecting $J_{reset} \sim 0.5$ MA/cm^2 in such a device.

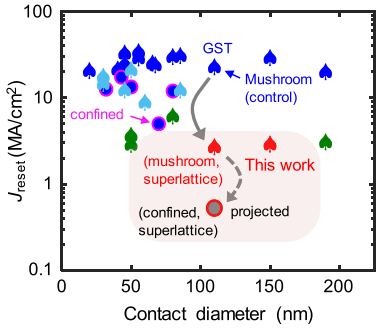

Fig. 4. **Benchmarking:** J_{reset} vs. BE diameter for various PCM technologies. SL-PCM results from this work are shown in red. J_{reset} for other PCM are from Refs. [3], [28], [29]. Mushroom cells are shown as spades, confined cells as circles, GST in dark blue, doped GST in light blue, and other SLs in green. GST is the $Ge_2Sb_2Te_5$ stoichiometry. Lower J_{reset} can also be obtained on flexible substrates [12].

We note the electro-thermal confinement is caused by the large anisotropy of the SL (nearly ~2000× between cross-plane and in-plane electrical resistivity), the lower cross-plane thermal conductivity (~3-4× lower than crystalline GST) and the ~1.8× higher TBR at TiN/SL vs. TiN/GST interfaces [14]. These unique features together with the small amorphous region observed at HRS in SL-PCM enable the large J_{reset} reduction compared to GST PCM.

Finally, **Fig. 4** summarizes the mushroom cell SL-PCM results in this work vs. conventional PCM [3], [28], [29]. Arrows in **Fig. 4** show the trends of J_{reset} reduction from GST to SL-PCM, and from mushroom to confined cell SL-PCM [projected from Fig. 3(f)], all enabled by the better electro-thermal and structural confinement.

IV. Conclusion

We demonstrated up to 10× lower reset current density (J_{reset}) in mushroom cell GeTe/Sb_2Te_3 superlattice PCM, compared to control GST devices. This was enabled by electro-thermal confinement of a thermally-driven phase change mechanism. The SL-PCM devices also show four stable resistance states with low resistance drift, while maintaining scalability with bottom electrode diameter. These results pave the route to low power, high-density memory and neuromorphic computing applications using PCM.

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