PHASE-CHANGE MEMORY

Ultralow–switching current density multilevel phase-change memory on a flexible substrate

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Phase-change memory (PCM) is a promising candidate for data storage in flexible electronics, but its high switching current and power are often drawbacks. In this study, we demonstrate a switching current density of ~0.1 mega-ampere per square centimeter in flexible superlattice PCM, a value that is one to two orders of magnitude lower than in conventional PCM on flexible or silicon substrates. This reduced switching current density is enabled by heat confinement in the superlattice material, assisted by current confinement in a pore-type device and the thermally insulating flexible substrate. Our devices also show multilevel operation with low resistance drift. The low switching current and good resistance on/off ratio are retained before, during, and after repeated bending and cycling. These results pave the way to low-power memory for flexible electronics and also provide key insights for PCM optimization on conventional silicon substrates.

Numerous emerging flexible electronics for the internet of things (IoT) (*1*, *2*) benefit from low-power embedded memory (*3*–*5*); examples include electronic skin (*6*), paper-like deformable displays (*7*), and smart IoT sensors for food and drug monitoring (*2*). Many of these applications could revolutionize personalized health care and global supply chains, particularly if they can rely on flexible substrates, which are easier to integrate with various form factors and surfaces. However, integrating conventional silicon-based memory into flexible electronics is difficult owing to the limited bendability of thinned silicon, complicated transfer processes, and potential thermal challenges on substrates with low thermal conductivity (*4*, *8*, *9*). As an alternative, memory devices could be fabricated directly on the flexible substrates, as long as this can be done at sufficiently low temperature (typically below 250°C). For example, flash and ferroelectric memory have been directly demonstrated on flexible substrates, but at the expense of higher operating voltage and power consumption than needed for their rigid counterparts (*4*, *10*).

Two other memory candidates that can be processed directly on flexible substrates are resistive random-access memory (RRAM) and phase-change memory (PCM) (*11*–*13*). Although many demonstrations exist with RRAM, its filamentary operation causes variability issues (*4*, *12*). By contrast, PCM offers lower variability than RRAM while providing faster speed, larger memory window, and longer write endurance than flash (*14*). These attributes and its potential for multilevel memory make PCM a candidate of interest for data storage in flexible electronics (*15*, *16*). The same properties are also important for IoT devices, which must often process data locally because of limited communication bandwidth with cloud servers (*17*).

However, a fundamental challenge of PCM has been its relatively high switching current and power, posing an obstacle for widespread adoption on both rigid (silicon) and flexible substrates (*12*, *13*, *18*). PCM on flexible substrates has been relatively unexplored, and previous studies (*13*, *18*) operated with high current owing to the use of conventional phase-change materials (e.g., $Ge_2Sb_2Te_5$) and lithography limitations (e.g., limited ability to focus) on uneven flexible substrates. Although the reset current of PCM is known to decrease with the cell size (*14*), such scaling is more difficult to achieve on flexible substrates; thus, reducing the reset current density becomes of greater importance. Reducing current density also benefits PCM on rigid substrates (*19*), where the area used by memory selector devices (which supply the current in high-density memory arrays) is valuable and must be minimized (*14*, *20*).

Here, we achieved ultralow reset current density and multilevel operation, which are difficult to realize for PCM on flexible substrates, with a combined approach that includes (i) use of a superlattice phase-change material, which limits heat loss into the metal electrodes; (ii) taking advantage of the very low thermal conductivity of the flexible substrate, which blocks heat loss from the bottom electrode (BE); and (iii) Joule heat confinement in a pore-like geometry. Our PCM devices were directly fabricated on a flexible polyimide (PI) substrate (Fig. 1A), without any layer transfers and a maximum process temperature of 200°C. The superlattice phase-change material (*21*) was deposited as 12 periods of alternating Sb_2Te_3 (4 nm) and GeTe (1 nm) layers. The ~600-nm-diameter pore-like device is surrounded by ~35-nm Al_2O_3 (Fig. 1B) on a TiN bottom contact [see (*22*) for fabrication details, fig. S1, and table S1].

We used high-resolution scanning transmission electron microscopy (STEM) to image the superlattice cross section on a silicon substrate, with the same deposition conditions as for the flexible PCM (Fig. 1C). [STEM sample preparation is difficult on the weak, electrically and thermally insulating polymer, which can warp during focused ion beam milling (*23*, *24*).] STEM imaging displays Sb_2Te_3 and $Ge_xSb_yTe_z$ layers, revealing some interfacial reconfiguration known to occur during deposition kinetics (*25*) but preserving clear and parallel van der Waals–like (vdW-like) gaps (*26*). X-ray diffraction (XRD) data in Fig. 1D show sharp polycrystalline peaks from the same superlattice film used for the STEM cross section. (Additional XRD data are shown in fig. S2 for a similar superlattice on TiN/PI/Si.) The pronounced (00*l*) out-of-plane XRD peaks correspond to highly oriented layers parallel to the substrate. A small broadening and shifting of some Sb_2Te_3 peaks and the presence of $Ge_xSb_yTe_z$ peaks (fig. S2) are consistent with partial diffusion of Ge atoms into Sb_2Te_3 (*27*, *28*).

The resulting PCM devices on the ~5-μm PI substrate are flexible (Fig. 1E), and we measured their resistance (*R*) versus current (*I*) before and during bending (Fig. 1F). For set and reset programming, respectively, we used 1-, 20-, and 500-ns and 1-, 60-, and 1-ns rise, width, and fall pulses (see fig. S3 for the setup and fig. S4 for an example output pulse). We read the resistance of all devices with a 50-mV direct current (dc) bias (*22*). Our ~600-nm diameter flexible PCM devices switch at ~0.2 to 0.25 mA of reset current (I_{reset}), with a resistance ratio up to ~100, maintaining the switching characteristics during both flat and bent substrate conditions. The estimated reset current density (J_{reset}) of ~0.1 MA/cm^2 is about two orders of magnitude lower than that of conventional PCM on rigid silicon substrates (*29*, *30*) and more than an order of magnitude lower than that of existing flexible PCM (*13*) (Fig. 1G).

We found that the reset current scales with the pore cell area (from ~600- to ~800-nm diameters; Fig. 2A), indicating the scalability of our technology, further supported by additional benchmarking (fig. S5). Our devices also demonstrate reasonably low cycle-to-cycle variation (Fig. 2B). We calculated resistance versus power (Fig. 2C), which we estimated from *R* versus *I* (Fig. 2B) and *R* versus voltage (*V*) (fig. S6A). We further noted low cycle-to-cycle variation for >450 cycles (fig. S6B). The peak reset power is ~0.8 mW; this could be further reduced with smaller cell diameters

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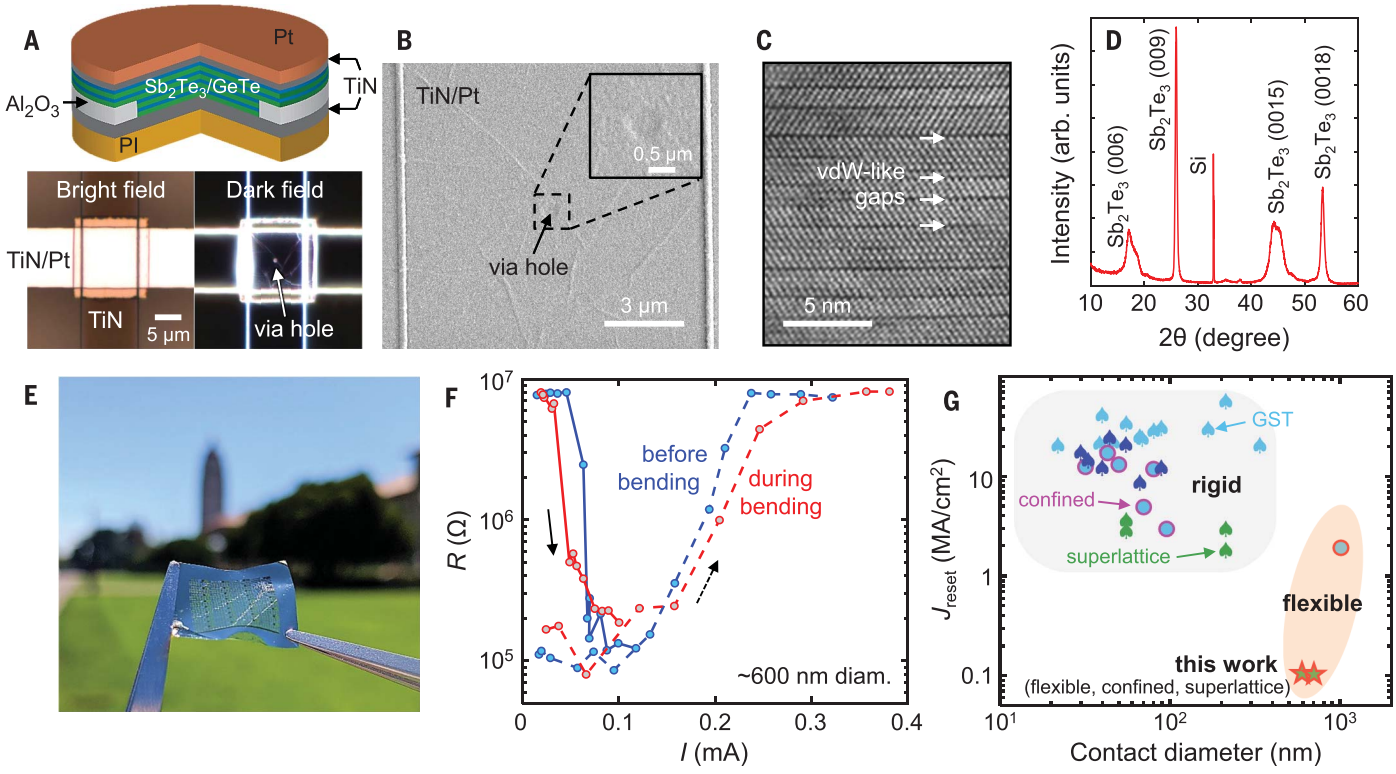

Fig. 1. Flexible superlattice PCM. (**A**) (Top) Schematic device cross section. (Bottom) Top-view optical images of fabricated devices. (**B**) Top-view scanning electron microscopy image of a device with a ~600-nm via hole (i.e., a hole in the Al_2O_3 insulating layer, defining the active device region). The inset shows a zoomed-in view. (**C**) High-resolution STEM cross section of the superlattice stack deposited on a Si substrate, using the same conditions as for the flexible PCM devices. STEM shows 5-atom Sb_2Te_3 layers, as well as 7- and 11-atom layers with Ge atoms diffused into $Ge_xSb_yTe_z$ (*25*), all separated by clear vdW-like gaps (see also fig. S7). (**D**) XRD of the same superlattice stack as in (C), demonstrating the polycrystallinity of the as-deposited films (see also fig. S2). (**E**) Photograph of one of our flexible substrates with memory devices. (**F**) Read resistance versus current for our flexible PCM (with a ~600-nm via hole) before and during bending to a radius of 4 mm, demonstrating low-current switching in both the flat and bent conditions. Solid arrow, from high-resistance state (HRS) to low-resistance state (LRS); dashed arrow, from LRS to HRS. Ω, ohms. (**G**) Benchmarking of reset current density (J_{reset}) reveals that J_{reset} is about two orders of magnitude lower than that of conventional PCM on rigid silicon substrates (*20*, *21*, *29*, *30*) and one order of magnitude lower than that of other flexible PCM (*13*). Some trends can be discerned—e.g., J_{reset} is reduced from mushroom-type cells (spades) to confined cells (circles) and is also reduced from conventional $Ge_2Sb_2Te_5$ (GST; light blue) or doped GST (dark blue) to superlattice PCM (green). Flexible PCM also has lower J_{reset} than its rigid counterparts, and our combination of flexible substrate with superlattice PCM in a confined cell yields the lowest $J_{reset} \approx 0.1$ MA/cm^2 (red stars).

but is limited here by the optical lithography. The reset energy of ~48 pJ (*22*) is nearly an order of magnitude lower than that of other devices, which used a filamentary bottom contact (*18*), owing to our shorter reset pulses of ~60 ns. Our reset power is two orders of magnitude lower than that of earlier nonfilamentary flexible PCM (*13*).

We also explored the multilevel capability and resistance drift of our flexible superlattice PCM, demonstrating four stable-resistance states (Fig. 2D). The same figure also reveals a low resistance drift coefficient ($\nu \sim 0.002$ to 0.008), which is more than an order of magnitude lower than that of conventional PCM (*31*) with clearly distinguishable resistance states [see supplementary text section I and table S2 (*22*)]. We applied several separate reset pulses of the same shape (1, 60, and 1 ns) and increasing amplitude (2.1, 2.6, 3.1, and 3.5 V) to achieve the intermediate-resistance states. Figure 2D also reflects retention of the low- and high-resistance states beyond 10^4 s. The low resistance drift is attributed to the presence of vdW-like gaps in the superlattice material even after electrical cycling (fig. S7), which can limit structural relaxation and long-range atomic diffusion. This behavior is a notable advantage of superlattice-type PCM, regardless of the substrate choice (*32*).

We measured our flexible PCM under a tensile bending radius of 4 mm (Fig. 3A). The devices maintained a resistance on/off ratio of >10 for 10^3 cycles while flat, then for 10^2 cycles while bent (Fig. 3B; fig. S8 shows additional endurance measurements taken over 10^4 cycles). *R*-versus-*I* measurements in flat and bent conditions (Fig. 1F) indicate that low I_{reset} is preserved upon bending, with a resistance on/off ratio of nearly 100. Further, we measured the bending cyclability of our PCM devices (Fig. 3C). We read their dc resistance after several bending cycles and measured the resistance states for a consecutive 300 s, with 30-s intervals between each resistance readout. These results show that both high- and low-resistance states are maintained with low drift before bending, as well as after 100 bending cycles. Notably, low switching current is preserved even after 200 bending cycles (Fig. 3D). The robustness of our devices during bending can be attributed to the PI thickness of 5 μm, which leads to a small strain of ~0.06% even at a 4-mm bending radius (*33*). Encapsulation with another few-micrometer-thick polymer layer would place our devices along the neutral mechanical plane, further reducing their strain (*34*). A comparison with other flexible memory technologies—in terms of retention, endurance, and choice of bending radius—is provided in table S3.

Finally, we sought to understand what leads to the ultralow current density in our flexible superlattice PCM devices. Earlier work had suggested that Ge atom movement may be responsible for switching in similar superlattice PCM on rigid substrates (*21*). However, we have recently found that the

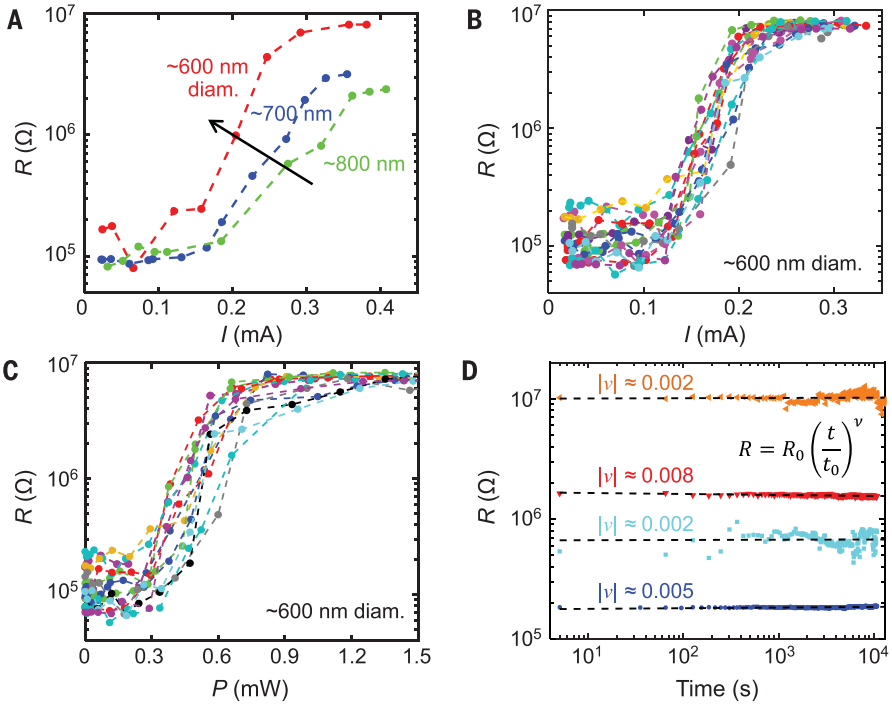

Fig. 2. Scaling, power, and multilevel measurements. (**A**) Read resistance versus current for our devices, showing the scaling of I_{reset} with cell area. (**B**) Resistance versus current for 15 cycles, showing low cycle-to-cycle variability of these devices (see also fig. S6B). (**C**) Resistance versus power (P) for 15 cycles, showing a switching power (P_{reset}) of ~0.8 mW. (**D**) Four stable-resistance states in the flexible PCM device with 600-nm diameter, showing multilevel capability with ultralow resistance drift over 10^4 seconds [see supplementary text section I (*22*)]. The resistance of the highest state (~10 megohms) is slightly higher than in the other panels because the multilevel states were reached with single-shot pulses from the lowest-resistance state, whereas the data in (A) to (C) were obtained with gradually increasing pulse magnitudes. R_0 is the resistance at an arbitrary time t_0, and t is the time after the last switching event.

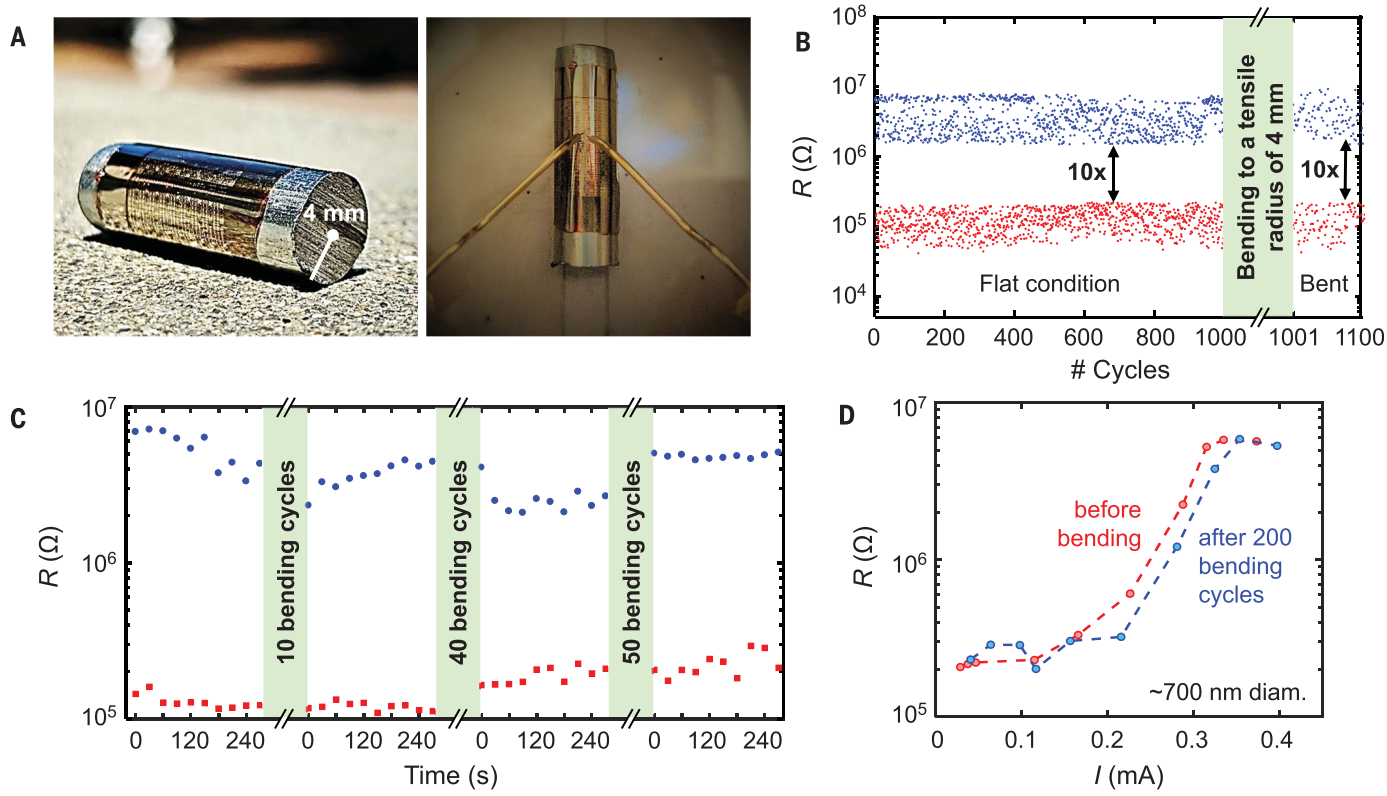

Fig. 3. Characterization before and after bending. (**A**) Measurement setup for our flexible PCM devices under a bending radius of 4 mm. (**B**) Resistance versus number of switching cycles before (i.e., flat condition) and during bending, showing that a 10-fold resistance window (10×) is maintained. (**C**) A resistance on/off ratio >10 is maintained over time upon cyclic bending. (**D**) Resistance versus current before bending and after 200 bending cycles, showing that low I_{reset} and the resistance on/off ratio are maintained after bending cycles.

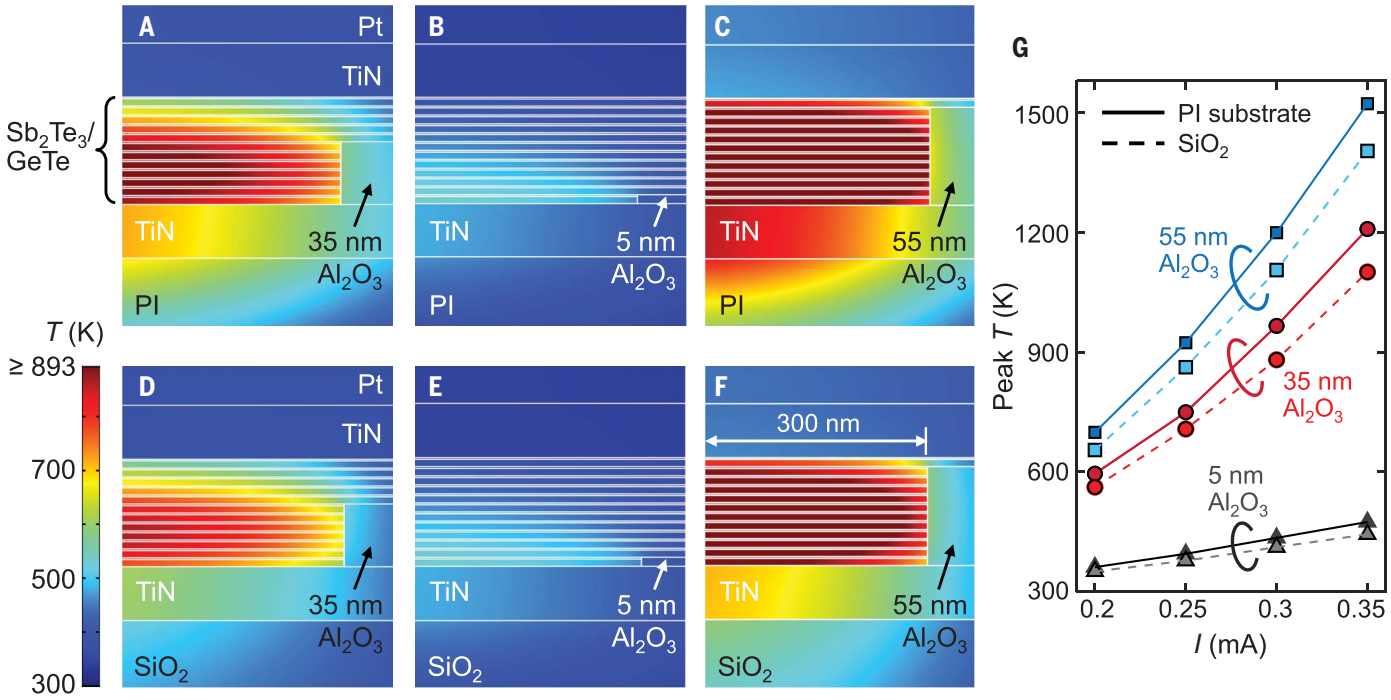

Fig. 4. Electrothermal simulations. Temperature distributions after a reset current pulse (0.3 mA, 60 ns) in superlattice PCM devices on flexible PI with (**A**) 35-nm Al_2O_3 insulation (see fig. S9 for an extended temperature profile into the PI substrate), (**B**) 5-nm Al_2O_3 insulation, and (**C**) 55-nm Al_2O_3 insulation, demonstrating the effect of thermal confinement from the superlattice layers and lateral Joule heat confinement from the Al_2O_3 insulation. Temperature distributions of similar devices on a rigid SiO_2 substrate with (**D**) 35-nm Al_2O_3 insulation, (**E**) 5-nm Al_2O_3 insulation, and (**F**) 55-nm Al_2O_3 insulation, showing less thermal confinement on a rigid substrate with higher thermal conductivity. The left edge is the axis of symmetry in (A) to (F), device diameters are 600 nm, and the vertical and horizontal scales are unequal. (**G**) Peak temperature versus current at the end of a 60-ns pulse for the devices whose temperature distributions are shown in (A) to (F).

superlattice has low cross-plane thermal conductivity and very high electrical anisotropy (*35*) owing to its numerous parallel vdW-like interfaces. Thus, we exploited these properties to conceive our design, which includes confinement of the superlattice PCM cell in a pore-like geometry on a substrate with ultralow thermal conductivity (the flexible PI). This leads to the pronounced reduction of switching current density, which points to a strong thermal component of the switching mechanism.

To gain deeper insight into the role of heat confinement in the pore device, we performed electrothermal simulations [Fig. 4 and supplementary text section II (*22*)]. These reveal simultaneous effects of thermal confinement due to the numerous interfaces, higher electrical resistivity across the superlattice, lateral Joule heat confinement in the pore geometry, and the thermally resistive PI substrate (Fig. 4 and fig. S9). By contrast, the temperature profile of a pore-type $Ge_2Sb_2Te_5$ device on PI (fig. S10) shows less thermal confinement and a much lower peak temperature (~368 K) than in the superlattice PCM device (~966 K). This simulation further confirms the efficacy of electrothermal confinement provided by the superlattice material with numerous vdW-like interfaces (*36*).

We also simulated devices with different Al_2O_3 side-wall thicknesses and found that heat is more concentrated in the active PCM cell region with increasing Al_2O_3 thickness. Thus, the peak temperature required for phase change can be achieved with a lower current pulse (Fig. 4, A to G). We attribute this behavior to improved electrical heating confinement (further visualized in fig. S11, where the peak vertical current density appears across a substantially larger portion of the PCM superlattice for 35-nm versus 5-nm Al_2O_3). For the same input current, 5 nm of Al_2O_3 thickness provides negligible confinement (Fig. 4B), resulting in a substantially lower (by a factor of ~2.2) peak temperature than in our nominal devices (Fig. 4A), whereas 55-nm Al_2O_3 provides better confinement (Fig. 4C).

The flexible PI substrate is very effective for achieving thermal isolation and lower reset current, in contrast to conventional rigid substrates that often include a combination of oxides (such as SiO_2) and silicon. The ultralow thermal conductivity of the flexible PI substrate ($k_{PI} \approx 0.12$ W m^{-1} K^{-1}) (*37*) is an order of magnitude lower than that of amorphous oxides or nitrides (*38*) and two orders of magnitude lower than that of silicon. As a result, it prevents heat loss from the TiN BE. For our nominal device structure with 35-nm Al_2O_3, the peak temperature in the BE is ~20% higher with the PI substrate than with a SiO_2 substrate (Fig. 4, A and D). This indicates that in our laterally confined pore-type PCM cell, the thermal conductivity of the substrate (e.g., PI versus SiO_2/Si) plays an important role, especially for heat loss from the BE, lowering the reset current density in flexible PCM compared with its rigid counterparts (Fig. 1G). Our conclusions are supported by the peak temperature–versus–current plot (Fig. 4G) that shows the importance of confinement in our devices for obtaining low reset current density. These findings should also enable future thermal engineering of PCM devices on silicon by introducing heat-blocking layers or even air gaps below the BE.

In summary, we developed a flexible, superlattice memory with much lower switching current density (~0.1 MA/cm^2) than in all other PCM types, as well as very low reset energy and power relative to other flexible PCMs. These characteristics were enabled by heat confinement in a superlattice material within a pore-type device on an ultralow–thermal conductivity substrate. The flexible PCM devices display multilevel capability with low resistance drift, indicating promise for emerging

in-memory computing applications. These results usher in data storage in flexible IoT electronics and also provide key insights for thermal engineering of conventional PCM on commercial, rigid silicon substrates.

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SUPPLEMENTARY MATERIALS

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Materials and Methods
Supplementary Text
Figs. S1 to S11
Tables S1 to S3
References (*39*–*67*)

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Supplementary Materials for

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Materials and Methods

Sample Fabrication. The devices were fabricated on a rigid silicon support for ease of handling during deposition and patterning steps (**fig. S1**). First, a ~5 μm thick polyimide layer (PI-2610, HD MicroSystems) was spin-coated (1500 rpm, 300 rpm/s, 40 s) on top of the silicon chip and baked on a hot plate at 90°C and 150°C for 90 s each. Then, the PI was cured in a nitrogen oven at 250°C for 30 min. All device patterning was done in direct-write lithography tools (Heidelberg MLA 150) with laser wavelengths of 375 nm and 405 nm. The ~30 nm thick TiN bottom electrodes were obtained by direct current (dc) magnetron sputtering (Ti reactive sputtering in N_2) on the PI and defined by lift-off. The sputtering parameters for all materials are listed in **table S1**. Afterwards, a 35 nm thick Al_2O_3 insulating layer was deposited by atomic-layer deposition (ALD) at 200°C using trimethylaluminum (TMA) and water as precursors. The via holes with diameters down to 600 nm were chemically wet-etched with commercial aluminum etchant (J.T. Baker, Aluminum etch 16-1-1-2) at 40°C.

The phase change superlattice was sputtered in the order indicated in **fig. S1B**. Prior to deposition, the bottom TiN surface was *in situ* cleaned by Ar ion etching [30 standard cubic centimeters per minute (sccm) Ar flow, 50 W radio-frequency (rf) bias for 10 minutes] to remove any native oxide. First, a ~3 nm thick Sb_2Te_3 seed layer was deposited at room temperature. Then, the temperature was raised to ~180°C at a rate of 10°C/min and then 12 periods of GeTe (~1 nm) and Sb_2Te_3 (~4 nm) alternating layers were deposited at ~180°C. The total thickness of the superlattice was ~60 nm. Finally, after letting the sputtering chamber cool down to room temperature, a 10 nm TiN capping layer (Ti reactive sputtering in N_2) was deposited *in situ* to protect the phase change layers from oxidation. The phase change stack was patterned by reactive ion etching (RIE) with 30 sccm Cl_2 / 5 sccm BCl_3, 10 sccm Ar, 60 W rf power at a pressure of 10 mTorr. Next, after doing an *in situ* Ar cleaning for 2 minutes, 20 nm TiN followed by 60 nm Pt was sputtered and defined by lift-off as the top electrode.

Finally, the PI substrate was released from the silicon carrier while immersed in deionized water to complete the fabrication process. A fabrication process flow diagram and additional details on deposition parameters are shown in **fig. S1**.

Electrical Measurement. The electrical measurement setup has two main functions, namely pulsed writing and direct current (dc) reading. We apply a small amplitude reset pulse to the device and then follow that with a dc read. We measure the resistance of all devices with a 50 mV dc bias. We repeat this process for increasing amplitude reset pulses to the device. While performing pulsed switching on devices, we calculate the peak transient current by measuring the peak voltage across the 50 Ω input on the oscilloscope. For peak power calculations, we assume nominal applied voltage and peak current. The energy is estimated by multiplying the peak power with the reset pulse width (~60 ns, see **fig. S4**), which is likely a conservative upper bound of the true energy consumed during a reset event. Once the Joule heating caused by the voltage pulse is greater than the melting temperature of the phase change layer and if the quench rate is fast enough, the phase is changed from crystalline to amorphous and hence the resistance changes from a low resistance state to a high resistance state.

Supplementary Text

Supplementary Section I: Resistance Drift Analysis

The resistance drift of the four different states shown in **Fig. 2D** from the main text was fitted with a power law commonly used in PCM devices (*39*, *40*):

$$R = R_0 \left(\frac{t}{t_0}\right)^{\upsilon},$$

where R is the resistance, R_0 is the resistance at an arbitrary time t_0, t is the time after the last switching event and v is the drift coefficient. Here, R_0, t_0 and v are used as fitting parameters. Plotted on a double-logarithmic scale the fit results in straight lines with the slope of v as indicated in **Fig. 2D**. The values of all fitting parameters for the four different resistance states are given in **table S2**.

Supplementary Section II: Electro-thermal Simulation

Electro-thermal simulations were performed using COMSOL™ Multiphysics. The coupled electro-thermal simulations solve the current continuity equations to calculate the potential and current density profiles, and the Fourier heat equation to calculate the temperature profile self-consistently.

The simulation domain takes all material electrical (resistivity, ρ) and thermal characteristics (thermal conductivity, k) as the main input parameters. Isothermal boundary condition is assumed at the bottom interface of the polyimide (PI) substrate at $T = 300$ K. On the outer circumference open boundary conditions are assumed, such that the heat can flow out of the domain (to the environment at $T = 300$ K) or into the domain. At the top boundary, a convective heat flux boundary condition is assumed, as these devices were measured in ambient air. Below the TiN bottom electrode (BE), either 1 μm thick PI or SiO_2 were used in the simulations because the temperature profile already reaches room temperature within a depth of a few hundred nanometers into these substrates (see **fig. S9**). The BE surface is taken as the ground potential $V = 0$. The left margin of the simulation domain is the central axis of symmetry of the device, thus only one-half of the PCM cell cross-section is shown in all simulation figures (**Fig. 4**, **figs. S9**, **S10**, **S11**).

For comparison, we simulated Sb_2Te_3/GeTe superlattices as well as conventional $Ge_2Sb_2Te_5$ (GST) devices. We include the known temperature-dependent thermal conductivity, electrical resistivity of GST (*41*, *42*) and bottom electrode (TiN) (*43*, *44*). We also incorporated the recently-measured thermal conductivity of the Sb_2Te_3/GeTe superlattice stack (~0.38 W/m/K), the in-plane and cross-plane electrical resistivity of the superlattice (5.8×10^{-4} Ω·cm and 1.1 Ω·cm, respectively), and thermal boundary resistance (TBR) at the interface with TiN (~52 m^2K/GW) (*35*). We also consider the temperature-dependent Seebeck coefficient of GST (*19*, *44*, *45*), Sb_2Te_3 (*46*, *47*), GeTe (*48*) and TiN (*44*). Reasonable estimates are assumed in the case of parameters not directly reported. We have not used any fitting parameter in the simulations.

Simulations include both Joule heating and thermoelectric phenomena (*19*) by solving the cylindrical heat conduction equation, $C(\partial T/\partial t) = \nabla(k(\nabla T)) + \rho J^2 - TJ\nabla S$, with the boundary condition for the Peltier heating as $TJ\Delta S$ at the junction of two materials with the Seebeck coefficient difference ΔS. Here, C is the volumetric specific heat, T is the absolute temperature, t is the time, k is the thermal conductivity, ρ is the electrical resistivity, J is the electrical current density and S is the Seebeck coefficient.

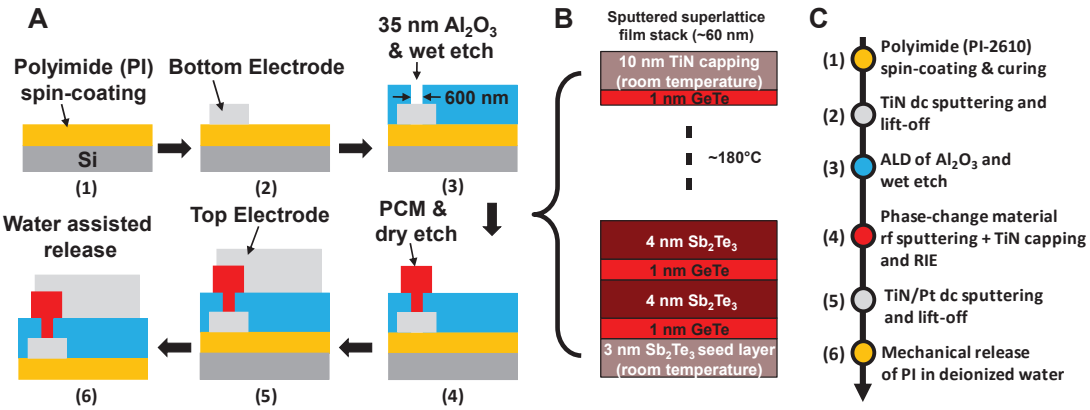

fig. S1. (**A**) Schematic process flow for flexible superlattice phase-change memory (PCM) devices. (**B**) Sputtering steps which form the superlattice PCM layer. The chamber base pressure was kept below 10^{-7} Torr. (**C**) Process sequence for the materials used in **A**. ALD: Atomic-layer deposition; RIE: Reactive ion etching; dc: direct current; rf: radio frequency. See Materials and Methods section for additional descriptions of various fabrication steps.

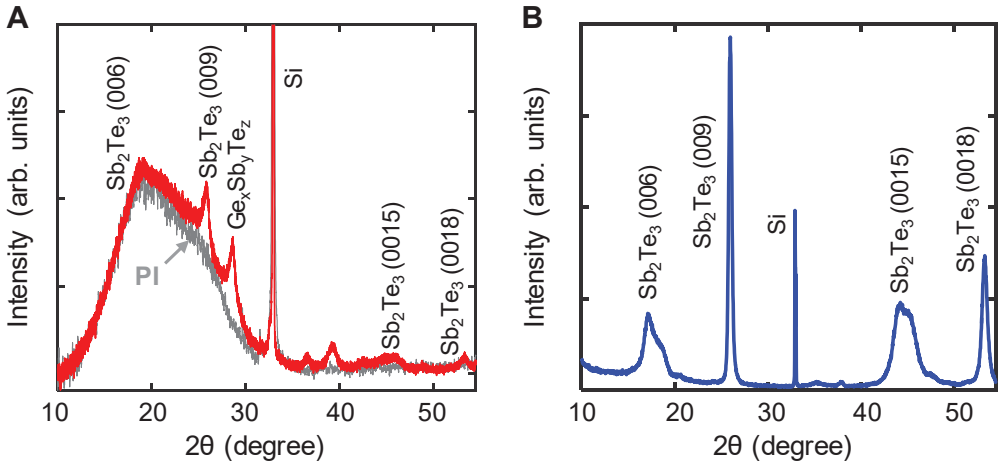

fig. S2. X-ray diffraction (XRD) of the superlattice stack (capped *in situ* with additional 10 nm TiN to prevent oxidation) deposited on (**A**) TiN (30 nm) / 5 μm polyimide (PI) / Si, and (**B**) on Si (same as Fig. 1D), using the same conditions as for the flexible PCM devices, confirming the polycrystallinity of the as-deposited films. The out-of-plane Sb_2Te_3 peaks in the XRD data reflect highly oriented films parallel to the substrate. The grey line in (A) represents the XRD spectrum of 5 μm thick bare PI on Si. Broadening and shifting of some of the Sb_2Te_3 peaks [(006) and (0015)] including additional $Ge_xSb_yTe_z$ peaks (*49–51*) indicate partial diffusion of Ge atom into Sb_2Te_3 (*27*, *28*, *52*) known to occur during deposition kinetics (*25*). Note, the spectra in (A) and (B) also show additional possible peaks from TiN and TiON (*53*, *54*).

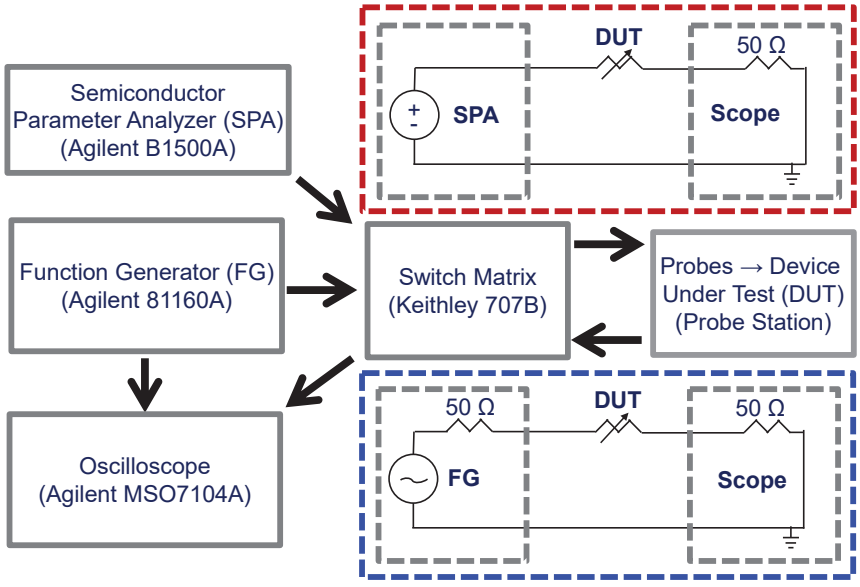

fig. S3. Electrical measurement setup: The measurement setup uses a semiconductor parameter analyzer (SPA), function generator (FG), and oscilloscope. The electrical measurement setup has two key functions, namely pulsed writing (performed in the block shown in dashed blue) and dc reading (performed in the block shown in dashed red). For pulsed switching and current measurements, we used an Agilent 81160A FG to produce the pulses and an Agilent MSO7104A mixed signal oscilloscope with 50 Ω of termination to measure transient current of the device under test (DUT). To measure the dc read resistance for all devices, we applied a 50 mV dc bias with an Agilent B1500A SPA. We used a Keithley 707B Switch Matrix to control the connection and alternate between pulsed and dc measurement.

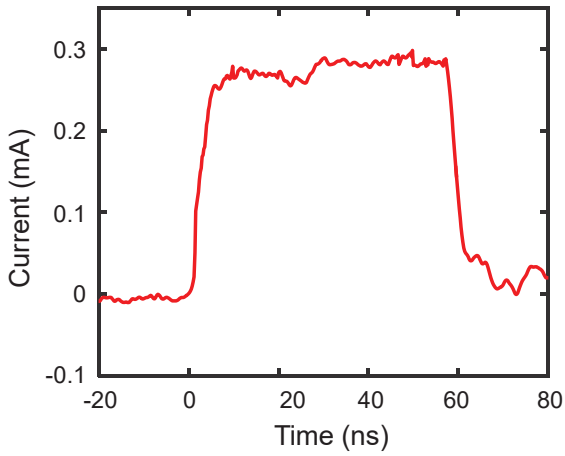

fig. S4. The transient output current pulse (obtained from the measured peak output voltage pulse across the 50 Ω termination of the oscilloscope) during a typical reset input pulse (3.5 V, 1/60/1 ns) of a flexible superlattice PCM device with diameter ~600 nm.

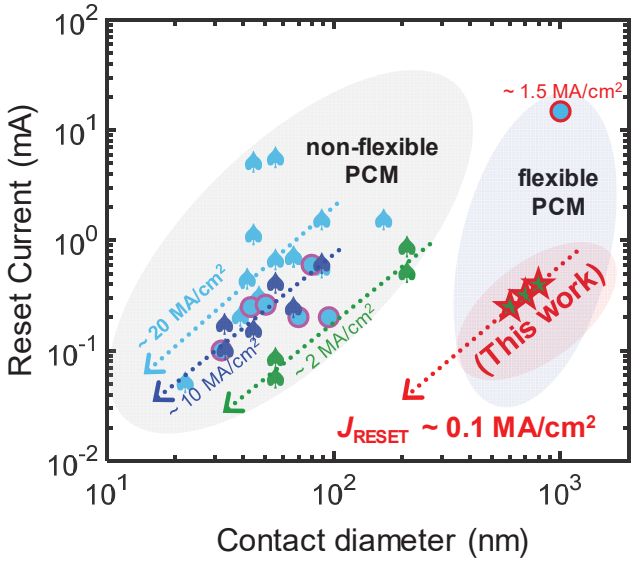

fig. S5. Benchmarking: Total reset current (in mA) *vs*. contact diameter showing the expected scaling. Green and blue arrows indicate well-known scaling for PCM on rigid (non-flexible) substrates in the literature (*20*, *21*, *29*, *30*). Red arrow illustrates expected scaling for flexible superlattice PCM devices in this work. Spade symbols indicate mushroom-type cells and circles are confined cells. (Stars used for this work.) Light-blue and dark blue colors represent conventional $Ge_2Sb_2Te_5$ (GST) and doped-GST, while green indicates superlattice material stacks.

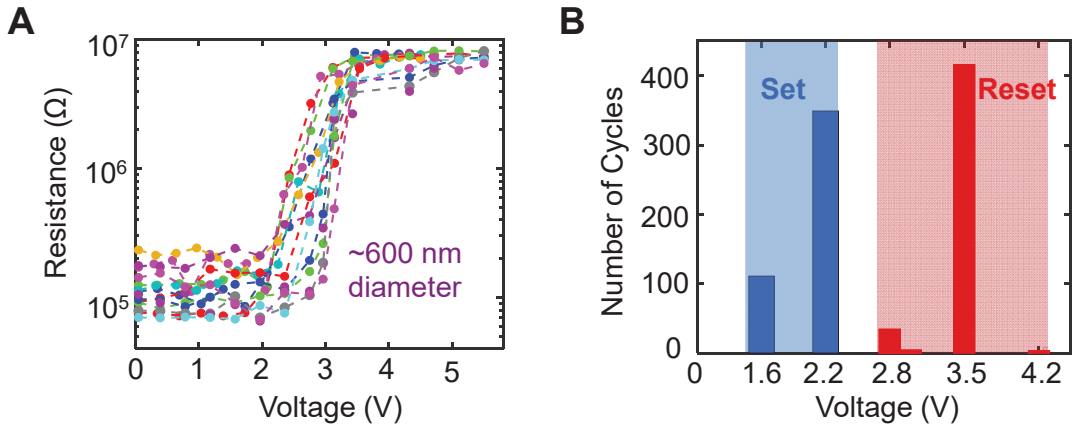

fig. S6. (**A**) Read resistance (*R*) vs. voltage (*V*) for multiple cycles (here 15 representative cycles shown for a device with ~600 nm diameter via hole). (**B**) Set and reset voltage distribution for >450 cycles demonstrating low cycle-to-cycle variability in our flexible superlattice PCM devices. The pulsing voltage magnitudes (1/20/500 ns pulse) required for transition from high to low resistance state (set) are shown in blue. Voltages (1/60/1 ns pulse) for transitions from low to high resistance state (reset) are shown in red.

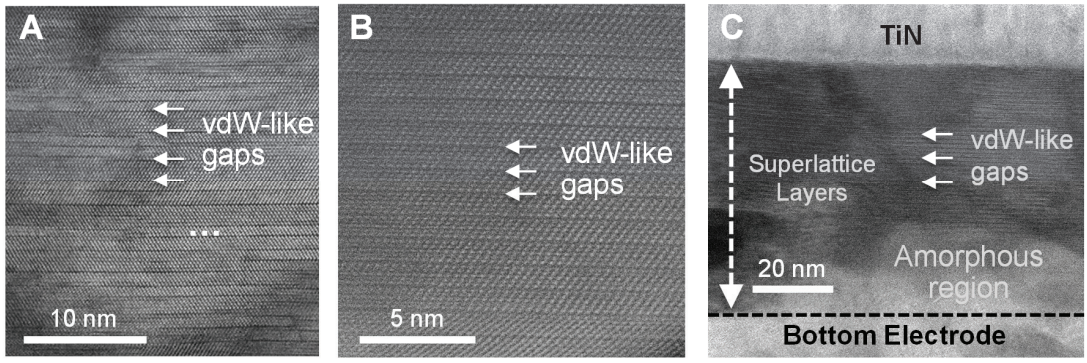

fig. S7. (**A**) Zoomed-out scanning transmission electron microscopy (STEM) of **Fig. 1C** from the main text. 5-atom Sb_2Te_3 layers are clearly visible, as are other odd-numbered atom layers formed by Ge intermixing into $Ge_xSb_yTe_z$ (*55*). All layers preserve sharp, parallel van der Waals-like (vdW-like) gaps [shorter interlayer distances compared to true vdW gaps in two-dimensional materials (*26*)] with few stacking faults visible. (**B**) High-resolution STEM of a superlattice PCM device near bottom electrode (on TiN bottom contact and with rigid SiO_2/Si substrate) in the low resistance state (LRS) after 8000 switching cycles. (**C**) High-resolution STEM for a well-cycled (10^6 cycles) superlattice PCM device (on TiN bottom contact and with rigid SiO_2/Si substrate) in the high resistance state (HRS). The alternating superlattices were deposited with the same process as those for the flexible PCM devices, and on the same bottom contact material (TiN). STEM reveals the presence of parallel interfaces and vdW-like gaps in the superlattice stack even for a well-cycled device in both LRS and HRS, while an amorphous region appears in HRS. We note that while obtaining such STEMs on a flexible substrate is highly challenging, the observations made here about the superlattice layers are applicable to flexible superlattice PCM devices regardless of the choice of substrate (flexible PI or non-flexible silicon) on the same bottom electrode material (TiN).

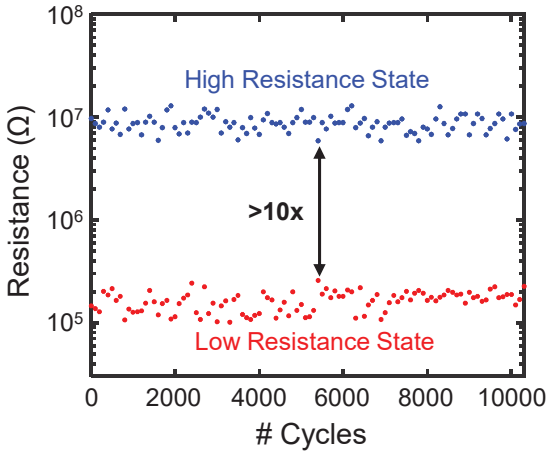

fig. S8. Additional endurance in flat condition after bending. >10 resistance on/off ratio maintained for $>10^4$ cycles, measured using 3.5 V; 1/60/1 ns and 2.2 V; 1/20/500 ns reset and set pulses, respectively. We read the dc resistance values at an interval of every 100 switching (set-reset) cycles.

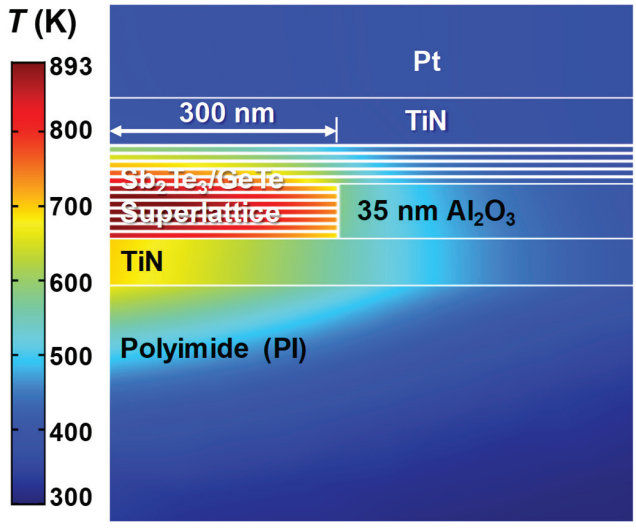

fig. S9. Computed temperature profile at the end of a reset pulse (0.3 mA, 60 ns) in flexible PCM with Sb_2Te_3/GeTe superlattice phase change layers, including the thick PI layer (1 μm PI simulated of which the top 150 nm are shown here). This is an extended version of main text **Fig. 4A**. The left margin is the central axis of symmetry of the device, thus only one-half of the PCM cell is shown. The vertical and horizontal scales are unequal. Similar simulations were carried out with 1 μm SiO_2 substrate instead of PI, in main text **Figs. 4D-F**. Note that realistic PCM devices on rigid SiO_2/Si substrates may have thinner SiO_2, or a more complex network of insulators, interconnects, and selector devices beneath them.

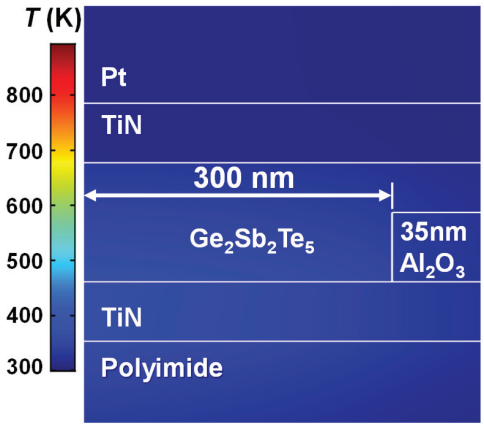

fig. S10. Temperature profile at the end of a reset current pulse (0.3 mA, 60 ns) in a flexible PCM device with conventional $Ge_2Sb_2Te_5$. The simulated peak temperature (~368 K) in flexible PCM device using $Ge_2Sb_2Te_5$ is significantly lower compared to the superlattice-like flexible PCM devices experimentally demonstrated in this work (**Fig. 4A**). The left margin is the central axis of symmetry of the device, thus only one-half of the PCM cell is shown. Note that the vertical and horizontal scales are unequal.

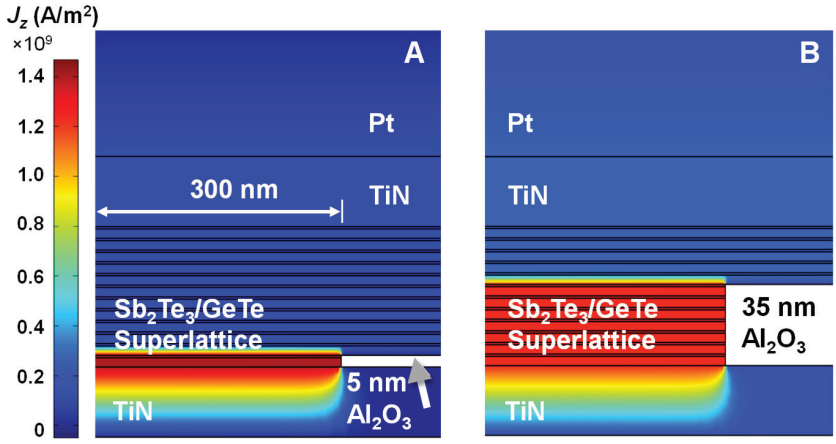

fig. S11. Distribution of the vertical (cross-plane) current density J_z for flexible superlattice PCM devices with (**A**) 5 nm thick Al_2O_3 insulation layer and (**B**) 35 nm thick Al_2O_3 insulation layer. The electrical interface resistance of the vdW-like gaps primarily impacts Joule heating in the vertical current flow direction. Thus, the electro-thermal properties of the superlattices are more effectively utilized in a pore-type structure. The left margin is the central axis of symmetry of the device, thus only one-half of the PCM cell is shown. Note that the vertical and horizontal scales are unequal.

Material	Power (W)	Pressure (mTorr)	Gas flow (sccm)	Temperature
Ti	100 (dc)	3	Ar: 30, N_2:15	Room temperature
Pt	100 (dc)	2	Ar: 25	Room temperature
Sb_2Te_3 (seed layer)	30 (rf)	4	Ar: 30	Room temperature; annealed in-situ to 180°C
Sb_2Te_3 (in superlattice)	30 (rf)	4	Ar: 30	180°C
GeTe (in superlattice)	30 (rf)	4	Ar: 30	180°C

table S1. Sputtering parameters for various materials used in the phase-change memory devices. dc: direct current, rf: radio frequency. The choice of the deposition parameters listed here were obtained by thorough optimization of the process parameters, including narrowing down the process window to achieve good quality superlattice films with van der Waals-like (vdW-like) interfaces and flexible superlattice PCM devices. Because the interfaces play an important role in these devices, it is desirable to have a layered structure with vdW-like gaps. While the exact choice of deposition temperature could be specific to the deposition tools and environment (e.g., AJA ATC-1800 magnetron sputtering system here), an optimum temperature is needed to maintain good polycrystallinity of the phase change layers (*56*) while too high of a temperature can result in global diffusion and voids within the superlattice film (*57*) and ultimately the loss of tellurium because of its high vapor pressure (*50*, *58*). The *in situ* cleaning of the bottom electrode surface with Ar etching is needed to remove any native oxide to ensure non-filamentary operation of PCM (*59*), and to obtain superlattice films with parallel orientation to the bottom electrode (*60*). In addition, room temperature deposition of an initial Sb_2Te_3 seed film as the first layer in the superlattice stack followed by annealing to higher temperature is beneficial to obtain subsequent good quality superlattice layers with better degree of orientation and possibly larger grain size (*61*).

Resistance state	R_0 (Ω)	t_0 (s)	ν
#1 (at ~2×10^5)	1.757×10^5	0.5368	0.005376
#2 (at ~7×10^5)	6.598×10^5	0.1847	0.001964
#3 (at ~2×10^6)	1.637×10^6	15.58	-0.008101
#4 (at ~1×10^7)	1.000×10^7	0.9619	0.002186

table S2. Fitting parameters of resistance drift of four different states shown in **Fig. 2D** from the main text.

Reference	**This Work**	Ref (*13*)	Ref (*18*)	Ref (*62*)	Ref (*63*)	Ref (*64*)	Ref (*65*)	Ref (*66*)	Ref (*67*)
Memory type	PCM	PCM	Filamentary PCM	RRAM	RRAM	Flash	MRAM	CBRAM	FeFET
Material	Sb_2Te_3/ GeTe	GST 225	GST225	Al_2O_3/ ZnO /Al_2O_3	GeO -HfON	CNT-graphene	CoFeB/ Mg/ CoFeB	Ga_2O_3	Organic material
Cell diameter (μm)	0.6	1	NA	100	NA	NA	80	100	1000
Switching Voltage (V)	3.5	8.5	4.2	1.2	3	10	NA	1.3	4
Switching Current (mA)	0.25	14.5	0.45	0.4	0.0016	NA	NA	4	NA
Switching Speed (ns)	60	140	200	40	50	100	NA	NA	NA
Switching Energy (pJ)	48	17255	378	19.2	0.24	NA	NA	NA	NA
On/Off Ratio	~100	40	40	>100	900	10	2	10^5	>100
Number of Resistance States (#)	4	2	2	2	2	2	2	2	2
Endurance (cycles)	$>10^4$	100	100	10^4	10^5	500	40	1400	2700
Retention	$>10^4$ s	10^4 s	10^4 s	$>10^4$ s	10^4 s	1000 s	2 weeks	10^4 s	$>8 \times 10^4$ s
Bending Radius (mm)	4	10	10	3	9	8	3	5	5.5
Bending Cycles (#)	200	1000	2000	$>10^4$	10^5	1000	40	10^4	7500

table S3. Comparison of our flexible PCM with other demonstrations of flexible non-volatile memories. The table shows that our memory devices are overall competitive (across various parameters) with the best demonstrations of flexible non-volatile memory to date. However, our flexible superlattice PCM stands out with two unique features: **i)** The switching *current* can be further reduced by shrinking the bottom electrode size, which is not possible in filamentary-type memories like RRAM or conductive-bridge (CBRAM). In other words, the record-low switching *current density* achieved here provides an excellent basis for reaching extremely low current and power in smaller devices. **ii)** Our devices have multiple resistance states (4 levels) and simultaneously excellent retention (low drift), making this type of memory particularly interesting for high-density storage and in-memory computing.

Abbreviations: PCM: Phase-change memory. RRAM: Resistive random access memory. Flash: Flash memory. MRAM: Magnetoresistive random access memory. CBRAM: Conductive bridge random access memory. FeFET: Ferroelectric field-effect transistor. NA: not available.

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22. Materials and methods are available as supplementary materials.

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