High Thermal Conductivity Insulators for Thermal Management in 3D Integrated Circuits

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***Abstract*— As physical transistor scaling nears its fundamental limits and many applications are increasingly bottlenecked by memory bandwidth, three-dimensional (3D) integration is a promising avenue for continuing Moore's law. Effective thermal management is crucial to unlocking the full performance benefits of 3D integrated circuits (ICs), due to the difficulty of removing heat from all layers in the 3D stack, and also due to thermal coupling between layers. Here, we explore the limits of passive thermal management in 3D ICs achievable using high thermal conductivity electrical insulators AlN and hexagonal BN (hBN). We show that replacing the thermally-resistive interlayer dielectrics of 3D ICs by high thermal conductivity insulators can greatly reduce the thermal resistance between layers and eliminate many of the thermal challenges of 3D ICs. Moreover, in a memory-on-logic architecture in which thermal insulation between memory and logic is desirable, highly anisotropic insulators such as hBN could be used as a heat spreader to keep both memory and logic dies relatively cool.**

***Index Terms*— Thermal management, nitrides, three-dimensional integrated circuits, heat spreader, thermal conductivity.**

I. Introduction

THE semiconductor industry has relied on increasingly creative ways to follow Moore's law, including new transistor designs, different dielectric and interconnect materials, as well as solving layout and reliability challenges. Three-dimensional (3D) integration [1], [2], [3] offers a way to further increase transistor density by stacking dies vertically to cram more components into an integrated circuit [4] package. Moreover, by boosting logic-memory connectivity [5] through dense vertical vias, 3D integration can greatly improve memory bandwidth [6], [7], [8], [9], which is in heavy demand in data science and machine learning workloads [10], [11].

However, 3D integration is not without challenges, one of which is thermal management. The dies in the 3D stack which are far from heat sinks could reach high temperature [12], leading to myriad performance and reliability challenges [13], [14], unless power density is reduced considerably compared to modern planar ICs. Furthermore, in a memory-on-logic architecture, it may be desirable to thermally isolate the logic and memory dies to improve efficiency and data retention by keeping the memory layer cool [15].

In this work, we compare three different materials as the interlayer dielectric (ILD) of 3D ICs: silicon dioxide (SiO_2) with thermal conductivity (k) = 1.4 $Wm^{-1}K^{-1}$ [16], aluminum nitride (AlN) with $k \approx 250$ $Wm^{-1}K^{-1}$ [17], [18] and hexagonal boron nitride (hBN) with $k \approx 400$ $Wm^{-1}K^{-1}$ in-plane and ≈ 5 $Wm^{-1}K^{-1}$ cross-plane due to its layered, highly anisotropic nature [19]. SiO_2 is taken as a standard reference material, even though the low-κ porous dielectrics commonly used in modern chips tend to have a lower thermal conductivity (TC) than SiO_2 [20].

II. Results

A. Geometry Simplifications

A quantitative thermal analysis is strongly dependent on the detailed layout, materials, and packaging of a 3D IC. In order to consider as broad and relevant a scenario as possible, here we analyze two main geometries: (1) a 3D IC with five stacked logic dies, all generating heat, and (2) a 3D IC with a memory die on a (heat-generating) logic die. The first case is a simple model for a 3D logic IC in which heat removal from the upper dies is the primary concern. The second case models a memory-on-logic architecture wherein the main concern is the peak temperature rise in the memory die.

As a simplifying assumption, each die is taken to be identical, with its detailed geometry taken from the execution unit of the OpenSPARC T2 processor core [21] designed in a 28 nm process design kit (PDK), with 9 layers of interconnects. The circuit geometry of a single die was obtained by extruding the layout of this circuit into 3D. This is illustrated in Fig. 1 for a small section of the interconnect network. The wide range of length scales in the interconnect network makes it difficult to mesh and simulate the complete geometry. We thus reduce each interconnect layer (for each ILD material considered) into a uniform, anisotropic medium that yields the same thermal resistance (TR) in each of the x, y and z directions [22], [23] via the procedure described in Fig. 1. In the z (vertical) direction, uniform temperature boundary conditions are applied to the top and bottom surfaces of each interconnect layer of thickness t (embedded in the appropriate ILD), with a temperature difference ΔT. The TC component k_{zz} of the effective medium is calculated as $\bar{q}t/\Delta T$, where $\bar{q}$ is the resulting average vertical heat flux, so that the effective medium has the correct vertical TR. This procedure is similarly repeated in the lateral directions, yielding k_{xx} and k_{yy}.

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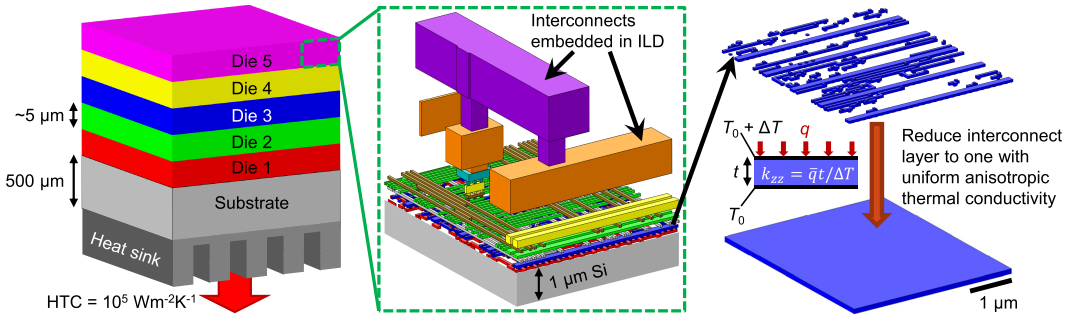

Fig. 1. Simplifying the stacked 5-die thermal simulation, with each (of 9) interconnect layer replaced by a uniform, anisotropic effective material. The interlayer dielectric is not shown, for clarity. The effective thermal conductivity of an interconnect layer in a certain direction is determined by applying constant-temperature boundary conditions on opposite sides, and computing the average normal heat flux $\bar{q}$ through the layer.

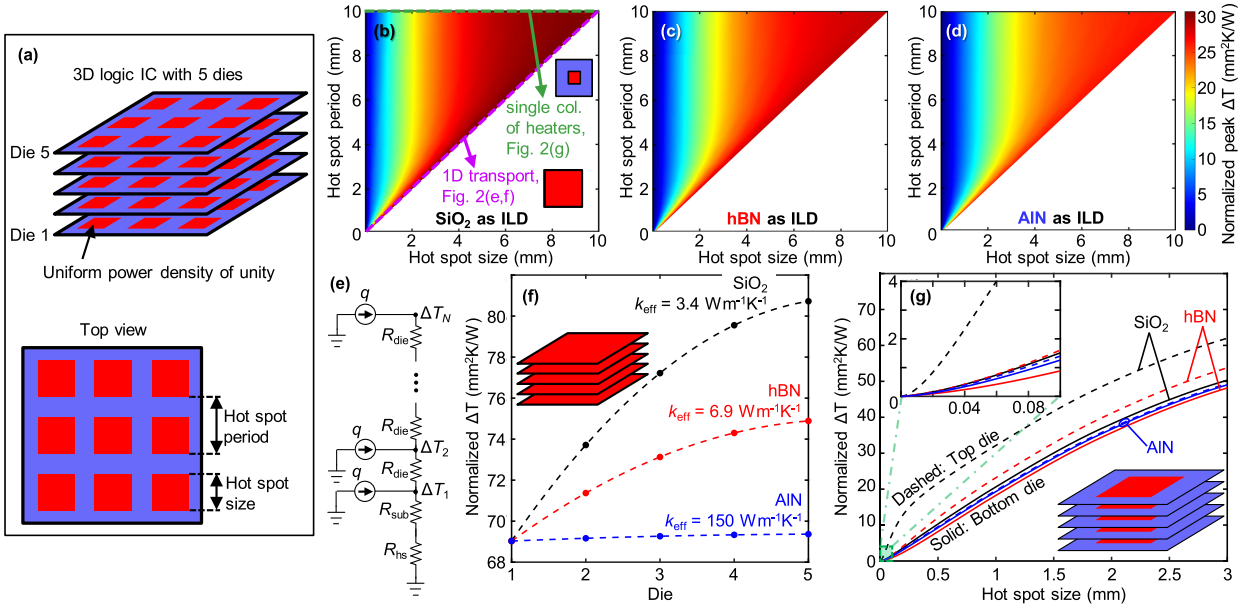

Fig. 2. (a) Simplified schematic of periodic array of heaters (with uniform power density) in a 5-die logic IC. (b-d) The peak temperature rise (ΔT) above ambient (normalized by heater power density) in the uppermost die as a function of hot spot size and period for SiO_2, hBN and AlN as ILD, respectively. (e) Thermal circuit for the 1D heat transport problem. (f) Normalized ΔT in each die, heated uniformly. Dashed lines are the best fits to the analytic solution of the 1D heat transfer equation. (g) Normalized peak ΔT in the top (dashed) and bottom dies (solid lines) as a function of hot spot size, for only a single column of hot spots. Inset: zoomed-in view of ΔT for hot spots smaller than 0.1 mm.

We note that the choice of ILD influences the system simulations through different effective TCs. In particular, due to its anisotropy, hBN yields a higher k_{xx} and k_{yy}, causing a reduction in the spreading TR of interconnect layers in the 3D IC.

B. Heat Removal

To simply model a 5-die 3D logic IC, we consider the periodic array of square heaters shown in Fig. 2(a). Each heater (hot spot) dissipates uniform power density of unity at the top of 1 μm thick Si, just below the 4 μm thick interconnects (see Fig. 1). The 1 μm Si thickness chosen here falls between Si thicknesses found in monolithic 3D ICs ($<$ 500 nm) and those using through-silicon vias (10s of μm) [24] and has little effect on our overall conclusions. The IC is assumed to be cooled primarily from the bottom, where the heat spreader, thermal interface material (TIM) and heat sink are lumped into an effective heat transfer coefficient (HTC) of 10^5 $\mathrm{Wm^{-2}K^{-1}}$. This HTC is typical of common TIMs used in device packaging [25], [26], and close to what is achieved with advanced cooling solutions [27], [28], [29]. We choose such an optimistic cooling solution to ensure the relevance of our results to future packaging technologies, and to focus on the impact of the ILD choice, because for more common cooling solutions and large hot spots, the package and heat sink TRs tend to dominate chip temperatures [30]. For simplicity, we assume an adiabatic boundary at the top surface.

We can gain insights into the differences between the ICs with different ILDs by simulating this configuration for various hot spot sizes and periods. Figure 2(b-d) show the peak temperature rises above ambient (normalized by the heater power density) in the uppermost die as a function of hot spot size and period for SiO_2, hBN and AlN as the ILD material, respectively. For large hot spots, hBN and AlN yield considerably lower temperatures than SiO_2. This can be understood by looking at the case of equal hot spot size and period, the dashed magenta line in Fig. 2(b). Here, the hot spots are all "just touching", such that each die is heated uniformly and heat flow is one-dimensional (1D). This 1D thermal circuit is shown in Fig. 2(e), where q is the heater power density, $N = 5$ is the number of dies, R_{die}, R_{sub} and R_{hs} are the die, substrate and lumped heat sink TRs per unit area, respectively. Fig. 2(f) shows the temperature in each die for this case.

This 1D vertical heat flow problem can be solved analytically, and noting that all heat generated in die m flows "down", the temperature rise in die n due to die m is $\Delta T_{n,m}/q = R_{\mathrm{hs}} + R_{\mathrm{sub}} + R_{\mathrm{die}}(\min\{n, m\} - 1)$. The temperature rise in die n

is found by adding the contributions from all N dies, yielding:

$$\Delta T_n/q = (R_{\text{hs}} + R_{\text{sub}})N + R_{\text{die}}(n-1)(N-n/2).$$

The simulated die temperatures are naturally well-described by this equation, and the best-fit curves are shown as dashed lines in Fig. 2(f). From the fit lines, we can determine R_{die}, and using $R_{\text{die}} = t_{\text{int}}/k_{\text{eff}} + t_{\text{Si}}/k_{\text{Si}}$ (total thickness of interconnect layers $t_{\text{int}} \cong 4$ μm, Si thickness $t_{\text{Si}} = 1$ μm, and Si TC $k_{\text{Si}} = 140$ $\text{Wm}^{-1}\text{K}^{-1}$) determine the effective TC k_{eff} of each die for different dielectrics. We find $k_{\text{eff,SiO2}} = 3.4$ $\text{Wm}^{-1}\text{K}^{-1}$, $k_{\text{eff,hBN}} = 6.9$ $\text{Wm}^{-1}\text{K}^{-1}$ and $k_{\text{eff,AlN}} = 150$ $\text{Wm}^{-1}\text{K}^{-1}$. We note these numbers are impacted by the Cu interconnects and the thermal boundary resistances between dissimilar materials, so k_{eff} differs from the ILD TC (i.e. it is higher for SiO_2 and higher than hBN cross-plane, but lower for AlN).

Owing to its high TC, AlN yields by far the highest k_{eff} and is thus most effective for extracting heat from dies that are far from heat sinks. Hence, for a logic-on-logic architecture where power distribution is uniform or hot spots are rather large, the cross-plane TC of the ILD is the most important parameter and should be maximized for low temperatures. Note also that $k_{\text{eff,hBN}}$ is only slightly higher than hBN's cross-plane TC, which shows that even though hBN's high in-plane TC does reduce the vertical TR of dies by facilitating heat transfer into interconnects (this is captured during interconnect geometry simplification, explained in Section II-A), its effect on the overall TR is very small.

At the other end of the spectrum, consider the case of a very large hot spot period, illustrated by the green dashed line in Fig. 2(b), so that the 3D IC is effectively heated by a single column of heaters. This represents a kind of worst-case scenario in which highly active circuit blocks dissipating large amounts of power happen to coincide vertically in each die. While we have also explored more thermally favorable arrangements of heaters with minimal vertical overlap [31], the thermal impacts of the ILD remain similar. Lowering temperatures in 3D ICs through thermally-aware floorplanning is discussed elsewhere [32], [33].

Fig. 2(g) takes a closer look at the worst-case scenario, plotting the peak temperature rises in the lowermost and uppermost dies. Once again hBN and AlN offer much lower temperatures than SiO_2, with the top and bottom die peak temperatures being very close for AlN. Looking at the smaller hot spots (< 300 μm), the high in-plane TC *and* low cross-plane TC of hBN jointly allow the heat generated in upper dies to spread over a larger area of the substrate, yielding the lowest temperatures in the *bottom* die, lower than AlN by over 20%. For small hot spots, hBN also yields much lower temperature rises in the uppermost layer than its low cross-plane TC might suggest, approaching the effectiveness of AlN at cooling the *upper* layers. This shows that lateral heat spreading provided by strongly anisotropic materials such as hBN is promising in logic-on-logic ICs if the power distribution is especially non-uniform.

C. Thermal Spreading and Decoupling

We finally consider a memory-on-logic scenario [Fig. 3(a)], with a top memory die heated by a hot spot in a bottom logic die [15]. Here, it may be desirable to thermally decouple the memory from the heat-generating logic [34], as high temperatures impact reliability [35] and retention [36], [37], [38] of memory technologies such as dynamic random-access memory. Moreover, it is important that hot spots in the logic layer do not result in large temperature non-uniformities in the memory die, to minimize spatial variability across memory devices. In our simulations, only the logic die generates heat, with the top and bottom surfaces of the IC modeled by a HTC of 10^5 $\text{Wm}^{-2}\text{K}^{-1}$. We note that the results for small ($\lesssim 500$ μm) hot spots and the overall trends remain largely the same for HTCs $< 10^5$ $\text{Wm}^{-2}\text{K}^{-1}$.

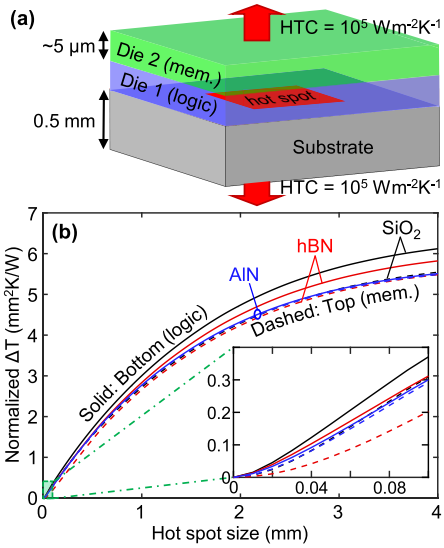

Fig. 3. (a) Simplified schematic of 2-die memory-on-logic IC, with hot spot in the logic die. (b) Normalized peak ΔT in the logic (solid lines) and memory dies (dashed lines) for different hot spot sizes and ILDs. Inset: zoomed-in view of ΔT for hot spots smaller than 0.1 mm.

The normalized peak ΔT in the active layers of the memory and logic dies are plotted in Fig. 3(b). For wide, chip-scale hot spots, the temperature rises are dictated mainly by the heat sink, so the ILD plays a minimal role. For smaller hot spots (see inset), there is still a relatively small difference between SiO_2 and AlN. However, hBN's anisotropic TC offers much lower temperatures in the memory die compared to other ILDs, reaching about half the logic die peak ΔT at a hot spot size of 60 μm. Consequently, with hBN, the effects of non-uniform heating in the logic die (characterized by the presence of localized hot spots) is greatly diminished in the memory die. These results indicate that hBN's relatively low *cross-plane* TC (despite being higher than that of SiO_2) serves to isolate the memory and logic dies somewhat, while its high *in-plane* TC helps it keep both dies relatively cool through lateral heat spreading.

III. Conclusion

We have described a simulation framework that, given the layout of a 3D IC, allows us to construct its simplified thermal circuit. We used this framework to analyze the implications of the ILD thermal conductivity on the temperatures of a 3D logic IC and a memory-on-logic IC, for various power distributions. Key insights are that (1) isotropic, high thermal conductivity insulators such as AlN are superior for heat removal for intermediate layers of the 3D stack, (2) strongly anisotropic materials such as hBN are effective at reducing peak temperatures due to localized hot spots, and (3) strongly anisotropic materials such as hBN can also be useful for reducing temperatures in applications that require thermal decoupling between dies.

REFERENCES

[1] P. Vivet, C. Bernard, F. Clermidy, D. Dutoit, E. Guthmuller, I.-M. Panadès, G. Pillonnet, Y. Thonnart, A. Garnier, D. Lattard, A. Jouve, F. Bana, T. Mourier, and S. Chéramy, "3D advanced integration technology for heterogeneous systems," in *Proc. Int. 3D Syst. Integr. Conf. (3DIC)*, Aug. 2015, pp. FS6.1–FS6.3, doi: 10.1109/3DIC.2015.7334468.

[2] M. M. S. Aly, M. Gao, G. Hills, C.-S. Lee, G. Pitner, M. M. Shulaker, T. F. Wu, M. Asheghi, J. Bokor, F. Franchetti, K. E. Goodson, C. Kozyrakis, I. Markov, K. Olukotun, L. Pileggi, E. Pop, J. Rabaey, C. Ré, H.-S. P. Wong, and S. Mitra, "Energy-efficient abundant-data computing: The N3XT 1,000x," *Computer*, vol. 48, no. 12, pp. 24–33, Dec. 2015, doi: 10.1109/MC.2015.376.

[3] M. S. Ebrahimi, G. Hills, M. M. Sabry, M. M. Shulaker, H. Wei, T. F. Wu, S. Mitra, and H.-S. P. Wong, "Monolithic 3D integration advances and challenges: From technology to system levels," in *Proc. SOI-3D-Subthreshold Microelectron. Technol. Unified Conf. (S3S)*, Oct. 2014, pp. 1–2, doi: 10.1109/S3S.2014.7028198.

[4] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics*, vol. 38, no. 8, pp. 114–117, 1965.

[5] H.-S. P. Wong, K. Akarvardar, D. Antoniadis, J. Bokor, C. Hu, T.-J. King-Liu, S. Mitra, J. D. Plummer, and S. Salahuddin, "A density metric for semiconductor technology," *Proc. IEEE*, vol. 108, no. 4, pp. 478–482, Apr. 2020, doi: 10.1109/Jproc.2020.2981715.

[6] Y. Xie, "Processor architecture design using 3D integration technology," in *Proc. 23rd Int. Conf. VLSI Design*, Jan. 2010, pp. 446–451, doi: 10.1109/VLSI.Design.2010.60.

[7] J. T. Pawlowski, "Hybrid memory cube (HMC)," in *Proc. IEEE Hot Chips Symp. (HCS)*, Aug. 2011, pp. 1–24, doi: 10.1109/HOTCHIPS.2011.7477494.

[8] D. U. Lee, K. W. Kim, K. W. Kim, H. Kim, J. Y. Kim, Y. J. Park, J. H. Kim, D. S. Kim, H. B. Park, J. W. Shin, J. H. Cho, K. H. Kwon, M. J. Kim, J. Lee, K. W. Park, B. Chung, and S. Hong, "A 1.2 V 8Gb 8-channel 128GB/s high-bandwidth memory (HBM) stacked DRAM with effective microbump I/O test methods using 29 nm process and TSV," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 432–433, doi: 10.1109/ISSCC.2014.6757501.

[9] M.-F. Chen, F.-C. Chen, W.-C. Chiou, and D. C. H. Yu, "System on integrated chips (SoIC^{TM}) for 3D heterogeneous integration," in *Proc. IEEE 69th Electron. Compon. Technol. Conf. (ECTC)*, May 2019, pp. 594–599, doi: 10.1109/ECTC.2019.00095.

[10] J. Y.-C. Sun, "System scaling for intelligent ubiquitous computing," in *IEDM Tech. Dig.*, Dec. 2017, pp. 1.3.1–1.3.7, doi: 10.1109/IEDM.2017.8268308.

[11] H. M. Makrani, H. Sayadi, S. M. P. Dinakarra, S. Rafatirad, and H. Homayoun, "A comprehensive memory analysis of data intensive workloads on server class architecture," in *Proc. Int. Symp. Memory Syst.*, Oct. 2018, pp. 19–30, doi: 10.1145/3240302.3240320.

[12] J. Jiang, K. Parto, W. Cao, and K. Banerjee, "Ultimate monolithic-3D integration with 2D materials: Rationale, prospects, and challenges," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 878–887, 2019, doi: 10.1109/Jeds.2019.2925150.

[13] M. G. Pecht, R. Radojcic, and G. Rao, *Gopal Rao, Guidebook for Managing Silicon Chip Reliability*. Boca Raton, FL, USA: CRC Press, 1999.

[14] A. Mogro-Campero, "Simple estimate of electromigration failure in metallic thin films," *J. Appl. Phys.*, vol. 53, no. 2, pp. 1224–1225, Feb. 1982, doi: 10.1063/1.330531.

[15] Y. Zhang, T. E. Sarvey, and M. S. Bakir, "Thermal challenges for heterogeneous 3D ICs and opportunities for air gap thermal isolation," in *Proc. Int. 3D Syst. Integr. Conf. (3DIC)*, Dec. 2014, pp. 1–5, doi: 10.1109/3DIC.2014.7152174.

[16] D. G. Cahill, "Thermal conductivity measurement from 30 to 750 K: The 3ω method," *Rev. Sci. Instrum.*, vol. 61, no. 2, pp. 802–808, Feb. 1990, doi: 10.1063/1.1141498.

[17] G. A. Slack, R. A. Tanzilli, R. O. Pohl, and J. W. Vandersande, "The intrinsic thermal conductivity of AlN," *J. Phys. Chem. Solids*, vol. 48, no. 7, pp. 641–647, 1987, doi: 10.1016/0022-3697(87)90153-3.

[18] R. L. Xu, M. Muñoz Rojo, S. M. Islam, A. Sood, B. Vareskic, A. Katre, N. Mingo, K. E. Goodson, H. G. Xing, D. Jena, and E. Pop, "Thermal conductivity of crystalline AlN and the influence of atomic-scale defects," *J. Appl. Phys.*, vol. 126, no. 18, Nov. 2019, Art. no. 185105, doi: 10.1063/1.5097172.

[19] E. K. Sichel, R. E. Miller, M. S. Abrahams, and C. J. Buiocchi, "Heat capacity and thermal conductivity of hexagonal pyrolytic boron nitride," *Phys. Rev. B, Condens. Matter*, vol. 13, no. 10, pp. 4607–4611, May 1976, doi: 10.1103/PhysRevB.13.4607.

[20] A. Delan, M. Rennau, S. E. Schulz, and T. Gessner, "Thermal conductivity of ultra low-*k* dielectrics," *Microelectron. Eng.*, vol. 70, nos. 2–4, pp. 280–284, Nov. 2003, doi: 10.1016/S0167-9317(03)00417-9.

[21] Oracle Hardware. *OpenSPARC T2*. Accessed: Aug. 1, 2022. [Online]. Available: https://www.oracle.com/servers/technologies/opensparc-t2-page.html

[22] H. Wei, T. F. Wu, D. Sekar, B. Cronquist, R. F. Pease, and S. Mitra, "Cooling three-dimensional integrated circuits using power delivery networks," in *IEDM Tech. Dig.*, Dec. 2012, pp. 14.2.1–14.2.4, doi: 10.1109/IEDM.2012.6479040.

[23] K. Etessam-Yazdani, H. F. Hamann, and M. Asheghi, "Impact of power granularity on chip thermal modeling," in *Proc. 10th Intersociety Conf. Phenomena Electron. Syst.*, 2006, pp. 666–670, doi: 10.1109/ITHERM.2006.1645409.

[24] P. Shukla, A. K. Coskun, V. F. Pavlidis, and E. Salman, "An overview of thermal challenges and opportunities for monolithic 3D ICs," in *Proc. Great Lakes Symp. VLSI*, May 2019, pp. 439–444, doi: 10.1145/3299874.3319485.

[25] R. Prasher, "Thermal interface materials: Historical perspective, status, and future directions," *Proc. IEEE*, vol. 94, no. 8, pp. 1571–1586, Aug. 2006, doi: 10.1109/Jproc.2006.879796.

[26] K. M. Razeeb, E. Dalton, G. L. W. Cross, and A. J. Robinson, "Present and future thermal interface materials for electronic devices," *Int. Mater. Rev.*, vol. 63, no. 1, pp. 1–21, Jan. 2018, doi: 10.1080/09506608.2017.1296605.

[27] A. Bar-Cohen, M. Asheghi, T. J. Chainer, S. V. Garimella, K. Goodson, C. Gorle, R. Mandel, J. J. Maurer, M. Ohadi, J. W. Palko, P. R. Parida, Y. Peles, J. L. Plawsky, M. D. Schultz, J. A. Weibel, and Y. Joshi, "The ICECool fundamentals effort on evaporative cooling of microelectronics," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 11, no. 10, pp. 1546–1564, Oct. 2021, doi: 10.1109/TCPMT.2021.3111114.

[28] K. Sefiane and A. Koşar, "Prospects of heat transfer approaches to dissipate high heat fluxes: Opportunities and challenges," *Appl. Thermal Eng.*, vol. 215, Oct. 2022, Art. no. 118990, doi: 10.1016/j.applthermaleng.2022.118990.

[29] R. Roy, S. Das, B. Labbe, R. Mathur, and S. Jeloka, "Co-design of thermal management with system architecture and power management for 3D ICs," in *Proc. IEEE 72nd Electron. Compon. Technol. Conf. (ECTC)*, May 2022, pp. 211–220, doi: 10.1109/Ectc51906.2022.00044.

[30] A. Jain, R. E. Jones, R. Chatterjee, S. Pozder, and Z. Huang, "Thermal modeling and design of 3D integrated circuits," in *Proc. 11th Intersociety Conf. Thermal Thermomechanical Phenomena Electron. Syst.*, May 2008, pp. 1139–1145, doi: 10.1109/Itherm.2008.4544389.

[31] J. H. Lau and T. G. Yue, "Effects of TSVs (through-silicon vias) on thermal performances of 3D IC integration system-in-package (SiP)," *Microelectron. Rel.*, vol. 52, no. 11, pp. 2660–2669, Nov. 2012, doi: 10.1016/j.microrel.2012.04.002.

[32] K. Cao, J. Zhou, T. Wei, M. Chen, S. Hu, and K. Li, "A survey of optimization techniques for thermal-aware 3D processors," *J. Syst. Archit.*, vol. 97, pp. 397–415, Aug. 2019, doi: 10.1016/j.sysarc.2019.01.003.

[33] K. W. Jung, E. Cho, S. Jo, S. Ryu, J. Kim, and D. K. S. Oh, "Assessment of thermal-aware floorplans in a 3D IC for server applications," in *Proc. IEEE 72nd Electron. Compon. Technol. Conf. (ECTC)*, May 2022, pp. 1036–1047, doi: 10.1109/Ectc51906.2022.00169.

[34] Y. Zhang, H. Oh, Y. Zhang, L. Zheng, G. S. May, and M. S. Bakir, "Thermal isolation and cooling technologies for heterogeneous 3D- and 2.5D-ICs," in *Handbook of 3D Integration: Design, Test, and Thermal Management*, vol. 4, P. D. Franzon, E. J. Marinissen, and M. S. Bakir, Eds. Weinheim, Germany: Wiley-VCH, 2019, pp. 347–373, doi: 10.1002/9783527697052.ch16.

[35] M. White, J. Qin, and J. B. Bernstein, "A study of scaling effects on DRAM reliability," in *Proc. Annu. Rel. Maintainability Symp.*, Jan. 2011, pp. 1–6, doi: 10.1109/RAMS.2011.5754522.

[36] M. Guan and L. Wang, "Temperature aware refresh for DRAM performance improvement in 3D ICs," in *Proc. 16th Int. Symp. Quality Electron. Design*, Mar. 2015, pp. 207–211, doi: 10.1109/ISQED.2015.7085426.

[37] J. Liu, B. Jaiyen, R. Veras, and O. Mutlu, "RAIDR: Retention-aware intelligent DRAM refresh," in *Proc. 39th Annu. Int. Symp. Comput. Archit. (ISCA)*, Jun. 2012, pp. 1–12, doi: 10.1109/ISCA.2012.6237001.

[38] K. Heyman. *DRAM Thermal Issues Reach Crisis Point*. Accessed: Aug. 1, 2022. [Online]. Available: https://semiengineering.com/dram-thermal-issues-reach-crisis-point/