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Recommended Methods to Study Resistive Switching Devices

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Resistive switching (RS) is an interesting property shown by some materials systems that, especially during the last decade, has gained a lot of interest for the fabrication of electronic devices, with electronic nonvolatile memories being those that have received the most attention. The presence and quality of the RS phenomenon in a materials system can be studied using different prototype cells, performing different experiments, displaying different figures of merit, and developing different computational analyses. Therefore, the real usefulness and impact of the findings presented in each study for the RS technology will be also different. This manuscript describes the most recommendable methodologies for the fabrication, characterization, and simulation of RS devices, as well as the proper methods to display the data obtained. The idea is to help the scientific community to evaluate the real usefulness and impact of an RS study for the development of RS technology.

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1. Introduction

Resistive switching (RS) is the property shown by some materials of cyclically changing their electrical resistivity between different stable levels when exposed to specific electrical stresses.[1] This property is interesting because these resistive states can be used to represent different logic states (e.g., the ones and zeros of the binary code), which may be useful for many digital applications (e.g., detectors,[2] information storage, and computation[3,4]). Most studies on RS materials and devices (≈95%[5]) reported stable RS between two resistive states, namely, high resistive state (HRS) and low resistive state (LRS). Some materials and devices show the ability of achieving more than two stable resistive states[6] (in this case the nomenclatures HRS and LRS are replaced by state 1, state 2, state 3, etc.), which may be used for multilevel information processing applications. However, reliably distinguishing each conductive state in multilevel devices is much more challenging due to the intrinsic variability of the device parameters (currents, switching voltages) in each state (see Section 3.4). This issue becomes extremely challenging when studying large group of samples statistically.

When fabricating a RS device, the material showing the RS capability (namely RS medium, which is typically an insulator) is sandwiched between two electrodes (in most of reports vertically[7]), leading to a microscale or nanoscale metal/insulator/metal (MIM) cell—the metallic electrodes are integral parts of the devices, i.e., the RS medium alone does not completely determine their characteristics. RS devices using semiconducting electrodes, i.e., forming metal/insulator/semiconductor (MIS) structures, have been also reported.[8,9] The first RS cells reported date from 1967,[10] and consisted on Au (30 nm), on SiO_2 (300 nm), and on

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Al junctions with a lateral device area of 9 mm^2. Over the time, new material combinations appeared, and currently RS can be readily achieved in various RS media, including transition metal oxides (TMOs),[11–14] chalcogenides,[15,16] polymers,[17,18] and 2D materials.[7] The most common metals used as electrodes are Pt, Au, Ag, Ti, Ni, and Cu,[1,19] although TaN and TiN are preferred in the industry.[20]

Different material combinations used in MIM cells require different types of electrical stresses in order to show RS, i.e., to induce HRS-to-LRS (set) and LRS-to-HRS (reset) transitions. Hence, the RS phenomenon can be classified into: i) unipolar and ii) bipolar RS, when the set and reset processes need to be triggered by applying stresses of the same or opposed polarity, respectively;[1] iii) nonpolar RS, when the set and reset transitions can be achieved by applying stress of any polarity;[21] and iv) threshold RS, when the LRS is volatile and the reset process takes place automatically when the stress is switched off.[22] By combining elements that show one of these pure RS mechanisms, additional RS behaviors have been observed, such as complementary RS, which can be achieved (for example) by connecting two bipolar RS devices in an antiserial manner[1] and/or using multistack insulators in the MIM cell.[23] Moreover, depending on the space occupied by the atomic rearrangements responsible for the state change, RS phenomenon may be also classified into: i) filamentary and ii) area-dependent.[1] RS is called filamentary if the atomic rearrangements inducing the switching take place in the form of small (<100 nm^2) spots within the RS medium. This mechanism is very similar to a reversible dielectric breakdown (BD) driven by the formation of one/few conductive filament/s (CF), and it is characterized by its fast switching speed (≈300 ps),[24] high LRS/HRS current ratios (namely I_{LRS}/I_{HRS}, up to 10^9[25]), and excellent integration capability (10^{11} bits cm^{-2}[3]). However, the high currents in LRS may increase the power consumption, plus the complexity of controlling the set/reset transition (due to their stochastic nature) results in a high cycle-to-cycle and cell-to-cell variability.[26] On the contrary, RS is called area-dependent if the RS is a homogeneous phenomenon that takes place at most of the locations laterally displaced (same depth) within the insulator. Area-dependent switching may happen at one or both metal/insulator interfaces, or even at the central depth of the insulator, and is related to diffusion effects and interface phenomena.[1,27,28] Distributed RS has the advantage of a lower power consumption (as no CF is completely formed/disrupted, in each state transition the currents in LRS cannot be so high), but the I_{LRS}/I_{HRS} ratios and switching speeds are not as competitive as in filamentary RS devices. Phase change materials may be considered area dependent, as the atomic rearrangements take place in the entire volume of the RS medium. However, their performance is closer to filamentary materials, as the atomic rearrangements effectively connect both metallic electrodes. Therefore, phase change materials and devices deserve special attention due to their high performance (i.e., switching speed, endurance) and impact in the RS device community,[29] and many of the fabrication and characterization methods discussed in this article are also applicable to them. The combination of layers with different properties is also a valid strategy to achieve specific performances. Recently RS cells using stacked bilayer RS media have shown both filamentary and distributed RS simultaneously,[9] which may be useful to build up RS devices with combined capabilities.

RS-based electronic products can include different amounts of RS cells depending on their applications, ranging from few (<10) in detectors[2] and logic gates,[30] to billions in nonvolatile memories (NVM)[31] and artificial neural networks.[32] The main challenges in the fabrication of RS-based NVMs are to ensure that all devices show good performance (see **Table 1**), and that all the RS cells within the RS device show nearly identical RS behaviors (i.e., low cell-to-cell variability). In fact, this second requirement is currently the greatest challenge (see Section 3.4),[3,26] and it is hindering the industrial mass production of RS-based NVMs. During the past decade the NVMs manufacturers have been the main players boosting RS technologies—this is a huge global market (47 billion United States Dollars in 2016[33]) that is expected to double by 2020.[34] Consequently, several NVM devices based on the RS phenomenon have been proposed during the past years, including the resistive random access memory (RRAM) and phase change memory,[26] and they have reached competitive performances compared to mainstream memories (i.e., static RAM, dynamic RAM, NOR and NAND flash) and other emerging memories (i.e., ferroelectric RAM, spin–transfer–torque magnetic RAM).[35,36]

RS-based NVMs started to be commercialized in 2015 by Panasonic,[37] and Adesto[38] also placed some RS based products in the market. However, despite the great progress achieved, RS-based NVMs are still not sufficiently robust for mass information storage,[26] and for this reason the devices commercially available are still restricted to very specific applications (e.g., controlling sensors[39]). Other RS applications, such as the use of RS cells as electronic synapses in artificial neural networks and neuromorphic computing[40] remain incipient, but their potential is greater, as they represent a completely new computing architecture with multiple applications (not only information storage). However, there is still no consensus on the performance metrics required of RS devices in order to be used as electronic synapses in artificial neural networks.

Research in RS devices is expected to be a very active field in the next decade, boosted by the Internet of Things,[41] and strong efforts need to be put into developing reliable RS technologies. Unfortunately, in recent years different methodologies have been used to fabricate, characterize, and simulate RS devices, being their real impact in RS technology and RS knowledge completely different. In this paper, we aim to clarify which are the correct methods for the study of RS devices, and how to provide useful knowledge for industrial RS technologies. This paper is focused on the fabrication and characterization of RS-based NVMs, as their performance and reliability criteria are the highest among all RS applications, but the methods presented here may be also applied for any type of RS device. This paper contains three technical sections, device fabrication (Section 2), device characterization (Section 3), and device simulation (Section 4), in which several technical recommendations are discussed, and a final section discussing the perspectives and challenges for the next years in RS science and technology (Section 5).

Table 1. Technology requirements for RS based NVMs versus best performances reported for RS based NVMs. The I_{ON}/I_{OFF} ratio is not strictly a technology requirement, but it is a reference parameter usually compared in RRAMs. Reproduced with permission.[7] Copyright 2017, Wiley-VCH.

Parameter	Technology requirements	TMOs based RRAMs		
		Best performances	Device structure	Ref.
Operating voltages	<1 V	0.7 V	$TiN/TiO_x/HfO_x/TiN$	[241]
		0.8 V	$Ti/ZrO_2/Pt$	[242]
		0.5 V	$TiN/Hf/HfO_x/TiN$	[52]
Power consumption	≈10 pJ per transition	0.1 pJ per transition	$TiN/Hf/HfO_x/TiN$	[52]
		0.1–7 pJ per transition	$Al/Ti/Al_2O_3$/s-CNT	[243]
Switching time	<10 ns per transition	300 ps	$TiN/TiO_x/HfO_x/TiN$	[24]
		<10 ns	$TiN/TiO_x/HfO_x/TiN$	[241]
		approximately ns level	$TiN/Hf/HfO_x/TiN$	[52]
Endurance	$>10^9$ cycles	10^{12} cycles	$Pt/Ta_2O_{5-x}/TaO_{2-x}/Pt$	[120]
		5×10^9 cycles	$Pt/TaO_x/Pt$	[129]
		$>10^{12}$ cycles	$Ta/TaO_x/TiO_2/Ti$	[121]
		10^{10} cycles	$Pt/TaO_x/Ta$	[116]
		10^{11} cycles	$W/AlO/TaO_x/ZrO_x/Ru$	[244]
Data retention	>10 years	>10 years@85 °C	$Pt/Al_2O_3/HfO_2/Al_2O_3/TiN/Si$	[133]
		>10 years@85 °C	$Pt/TaO_x/Pt$	[129]
MIM cell size	576 nm^2	5 nm^2	$TaN/TiN/Zr/HfO_2$/CAFM tip	[245]
		10 nm × 10 nm	$TiN/Hf/HfO_x/TiN$	[52]
I_{ON}/I_{OFF} ratio	10^6	3×10^6	Ni/GeO/STO/TaN	[127]
		2×10^6	$Pt/Gd_2O_3/Pt$	[246]

2. Device Fabrication

The study of RS in different materials is normally conducted in one or few MIM cells (test structures), as most laboratories in universities and research institutes do not have the capability to fabricate an entire RS product. Three kinds of MIM test structures are the most common when studying RS: i) common bottom electrode (BE, **Figure 1**a), ii) cross-point (Figure 1b), and iii) cross-bar (Figure 1c). The first one uses a conductive substrate that serves as common BE for all the MIM cells.[42] Then, an insulating film is deposited on its entire surface and finally several top electrodes (TE) with a specific area can be patterned along the surface of the insulator.[43] A top-view scanning electron microscopy (SEM) image of matrices of RS cells (with different sizes) fabricated using this method is displayed in Figure 1a. Instead of a conductive substrate, an insulating substrate covered with a metallic film can be also used, but in that case the insulator should not cover the entire surface of the underlying metal film, which needs to be contacted for electrical characterization.

After fabrication, the devices can be characterized in a probe station connected to a semiconductor parameter analyzer (SPA) by contacting to the TE and BE. If very small TEs are fabricated, they might also be contacted using the probe tip of a conducive atomic force microscope (CAFM),[44] although one needs to have in mind that: i) the tip/electrode contact may not be as good as in the probe station (e.g., molecules of water from the relative humidity of the environment may be present between the tip and the electrode), reducing the overall detected current,[45] ii) the tip conductivity may degrade fast,[46] iii) the electronics of standard CAFMs present important limitations for the measurement of RS[47] (see Section 3.5), and iv) the measurement process is more complex, i.e., a topographic map is required to find the electrode on which the tip will be placed, and therefore the characterization time will be much longer. For these reasons, the use of CAFM to test MIM cells (placing the CAFM tip on the top electrode) has not widespread, and in RS research CAFM is mostly used for studying scalability,[9] as well as to distinguish which locations of an insulator drive RS and which do not[48,49] (in both cases the CAFM tip serves as top electrode). Therefore, the main problem of the device structure in Figure 1a is that the minimum size of the devices that can be characterized with the tip of the probe station is always >100 μm^2.

To solve this problem, cross-point RS cells can be fabricated (see Figure 1b),[50] although their fabrication process is slightly more complex because it involves two lithography steps: deposition of the BE and TE, and ideally a third photolithography step to etch the RS medium deposited on the BE may be also necessary. In this case the metallic pads for probe station contact are still large (typically 10^4 μm^2), but the sandwiched MIM area can be much smaller. Using photolithography and electron beam lithography (EBL), cross-point MIM cells as small as 1 μm × 1 μm[51] and 10 nm × 10 nm[52] can be fabricated, respectively. While cross-point structures can be very competitive for RS studies in terms of scalability, some genuine circuit level factors (such as sneak path leakage currents[53]) cannot be analyzed

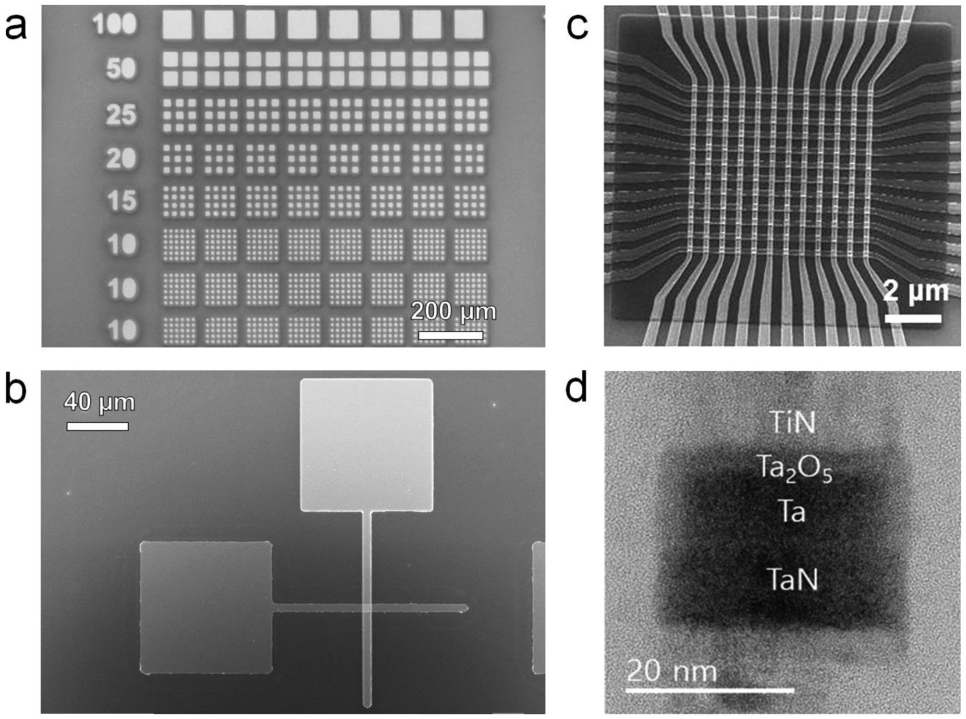

Figure 1. Common structures for the study of RS devices. SEM images of the three main types of structures commonly used to study resistive switching. a) TE deposited on blanket samples with a common BE. b) Isolated cross-point RS devices. c) Cross-bar structure formed by multiple cross-point structures interconnected. d) Cross-sectional TEM image of a 28 nm wide MIM structure. a,b) Reproduced with permission.[42] Copyright 2018, Wiley-VCH. c) Reproduced with permission.[55] Copyright 2016, Springer Nature. d) Reproduced with permission.[60] Copyright 2017, Royal Society of Chemistry.

using this kind of structure. For such purpose, some reports built planar[54,55] and 3D[56] cross-bar arrays (see Figure 1c). In this case, the MIM cells are interconnected with thin wires that end up in large pads,[54] so they can be characterized using the probe station. The test setup for advanced cross-bar circuit structures typically requires die packaging and dedicated printed circuit board or custom probe card in combination with switch matrix tool.[57] Note that the term cross-bar refers to a collection of interconnected cross-point devices; therefore, using the term cross-bar to refer to a single and isolated cross-point structure is misleading.

Thus, the types of structures used to characterize RS may vary a lot, and therefore the impact of the knowledge extracted from each of them will be also very different. The preferred configuration is the cross-bar because it is the most demanded for realistic RS products, although cross-point can also provide very accurate information about the functioning of one single RS cell. However, if the RS cells embedded in the cross-bar array do not have enough nonlinearity, the signals collected when studying a specific cell may contain contributions from the adjacent ones. For this reason, it is recommendable that studies on cross-bar RS structures also include data about isolated cross-point devices.

The most important parameter when studying RS devices is the area of the MIM cell—that affects the currents in HRS (I_{HRS}), and sometimes also in LRS (I_{LRS}, e.g., in devices with distributed RS mechanism). In CF-based devices, the RS is a stochastic process that always takes place at the weakest locations of the sample;[58] if the device size is larger the probability of finding weaker points is larger, which modifies the set and reset voltages (V_{SET} and V_{RESET}, respectively). This produces different BD energies that create CFs with different sizes, and subsequently the characteristics of the devices are also different. In general, smaller CF-based RS devices show lower I_{HRS} and larger V_{SET}/V_{RESET}.[22] For this reason, vertical MIM structures with a common BE and large (>100 μm^2) TEs should be avoided; when the fabrication of cross-bar and cross-point structures is impossible, vertical MIM structures with large electrodes should be combined with nanoscale electrical characterization experiments (e.g., CAFM, see Section 3.5) in order to confirm good RS scalability,[9] which is essential to demonstrate that the findings are applicable to ultrascaled devices. Another disadvantage of devices made of a common BE with large TEs (as in Figure 1a) is that the tip of the probe station exerts a non-negligible pressure in the active area of the RS device, which may change the characteristics measured due to mechanical stress. Ideally, the area of the MIM device should be as small as possible. References [59] and [60] reported MIM-like RS devices with diameters of 10 and 28 nm, respectively (see Figure 1d).

Furthermore, the methods involved in the fabrication of the RS cells and devices (e.g., metal and RS medium deposition and lithography) are critical for ensuring the good quality of the results. In particular, minimizing thickness fluctuations and maintaining clean interfaces (between the metallic contacts and the RS medium) are mandatory. Keeping the vacuum between each step is also beneficial for the RS devices, although in many cases that may not be possible because the electrodes and RS medium might be fabricated using different equipment. In the

following sub-sections some specific technical advice for each process step is given.

2.1. Selecting the Bottom Electrode

The surface of the substrate used needs to be as flat as possible, as that would reduce the number of bonding defects and avoid thickness fluctuations of the layers deposited on top; this is critical to reduce cell-to-cell variability. The best way is using a Si wafer covered by a few-hundred nanometer SiO_2 film as substrate; the reason is that such substrate has a root mean square (RMS) surface roughness <0.2 nm,[61] which is similar to the roughness of industrial wafers on which real RS devices should be integrated. The SiO_2/Si wafer should be covered with a metallic film as BE (the recommended thickness is >50 nm to withstand the high current densities in LRS). This metallic film may cover the entire surface of the SiO_2/Si wafer if working with RS cells that share a common BE (see Figure 1a), or just cover some specific areas to delimitate cross-point or cross-bar BEs (see Figure 1b,c). The use of noble metals (Au, Pt) as BE is more common than metals that can easily oxidize (Ti, Cu)—and recommendable when working in university labs without exhaustive air and humidity control—because they collect less oxygen from the atmosphere during the time between BE and RS medium deposition (although in the industry noble metals may not be used due to their high cost and etching issue). It should be noted that introducing oxygen intentionally in the RS devices is fine but in a controllable way, e.g., using thermal treatments or doping techniques; the adsorption of oxygen from the atmosphere to form RS media[62] is always undesired. However, the adhesion of Au or Pt to the surface of the substrate (SiO_2/Si wafer) may be not ideal, and sometimes an interfacial film of few-nanometers Ti may be used to facilitate its adhesion.[63] It should be noted that (ultimately) the use of industry-compatible conductive alloys (TaN, TiN) is desired, although controlling the amount of oxygen may be challenging in laboratories of several universities and research institutes (in such case, using noble metals may lead to better quality interfaces). For metal deposition, the use of electron beam evaporation (EBE) is the most recommended tool because it leads to a very smooth surface, although sputtering also leads to an acceptable surface roughness. The worst option for metallic substrate serving as BE is the use of metallic foils,[64] as their surface can be very rough (RMS > 100 nm).[65]

2.2. Deposition of the RS Medium

The deposition of the insulating film is the most critical step, and its surface needs to be as smooth as possible to avoid cell-to-cell variability. The most common techniques used for TMO deposition are atomic layer deposition (ALD)[66] and sputtering.[67] While the use of ALD can lead to surfaces as smooth as RMS < 0.2 nm,[68] the surface roughness of sputtered films (RMS < 1 nm[69]) is still acceptable for RS applications. In fact, in some cases sputtered RS media have shown better RS performance than ALD ones due to their larger initial density of defects, which can trigger the initial BD at lower voltages, producing less damage in the insulator and preventing irreversible BD.[48] As an example, in many works as-grown ALD HfO_2 does not show RS;[48] only after an annealing at moderate (≈500 °C) temperatures the HfO_2 generates defects (mainly at the grain boundaries) and shows RS. On the contrary, sputtered HfO_2 shows stable RS without the need of such annealing.[70] Moreover, stoichiometry control is more straightforward in sputtering than ALD. However, it should be noted that in 3D cross-bar devices the RS medium must be deposited in the vertical sidewalls of high-aspect-ratio holes, and the only technique able to do this is ALD.[71–75] Many recent reports showed several-layer 3D vertical RS devices where the RS films were prepared by physical vapor deposition; this may be good as a proof-of-concept, but these devices are not expected to show high performances in terms of cell-to-cell variability unless they are fabricated using ALD.

Several studies of polymers[17,18] and 2D materials[7,75] as RS medium used the spin coating technique: a drop of liquid-phase material is deposited on the substrate (common BE) and spun (at 1000–3000 rpm for 1–3 min, depending on the viscosity of the material used); afterward the sample is normally heated at moderate temperatures (below 100 °C) for a few (<5) minutes. This process leads to the formation of a film with thicknesses always >100 nm,[75] and a surface roughness much larger than that of TMO-based RS cells, i.e., RMS > 10 nm.[75] When using the spin coating methodology, the risk of prohibitive cell-to-cell variability is very high due to the large surface roughness (if the surface of the BE is very flat and the RS medium surface is very rough, that would produce thickness fluctuations from one device to another). In recent years, several publications fabricating RS cells via spin coating of novel 2D materials,[7,75] polymers,[17,18] and chalcogenides[15,16] appeared, and they demonstrated a proof-of-concept observation of RS through one/few cycles. Unfortunately, none of them included cell-to-cell variability information, and in most cases even the total number of devices characterized was not indicated. In fact, we are not aware of any work using spin coating technique combined with cross-point structures, meaning that all known studies apply to large device sizes >100 μm^2; therefore, additional corroborations of those findings in smaller RS cells are necessary.

It should be highlighted that, independently of the deposition method, when depositing the RS medium on metal-coated SiO_2/Si wafers it is recommendable to keep a part of the BE exposed, so that it can be later contacted with the tip of the probe station. Several groups do not follow this step and later scratch the surface of the insulator with the tip of the probe station (applying a vertical/lateral mechanical stress using the screws of the tip manipulator). Although this method works, it should be avoided when possible because it may damage the probe station tips and reduce the lifetime of the devices (e.g., if the thickness of the bottom metal is reduced due to scratching, it may be more susceptible to melting due to high currents during LRS, which may reduce the endurance of the RS cells).

2.3. Patterning the Top Electrodes

When working with cross-point and cross-bar structures, the electrodes (both BE and TE) are deposited via photolithography or EBL combined with metal deposition (e.g., EBE or

sputtering). The use of lithographic techniques ensures that all test structures will have the same shape, and avoids the deposition of metal outside the selected areas (i.e., no metal can penetrate below the photoresist). The only drawback is that the surface of the RS medium needs to be initially covered with a film of photoresist that is later removed, and that may lead to polymer residue contamination[76] (see **Figure 2**a,b). Although the developing process of the photoresist could be improved and the samples might be intensively cleaned, one should note that the surface of a material as-deposited will be always cleaner than after exposure to photoresist and developing, especially if this process is not done in the industry.

When working with devices that use a common BE (see Figure 1a), this problem can be mitigated by using a shadow mask, which also eases the entire process. A shadow mask is simply a piece of metal with holes patterned exactly with the shape of the electrodes to be deposited, and it is placed directly on the sample during metal deposition. However, the use of shadow masks may bring other undesired problems, such as deviation on the shape and size of the holes (Figure 2c), and penetration of metal below the mask (i.e., out of the areas reserved for the electrodes, see Figure 2e–h). Nevertheless, if a laser-patterned shadow mask is used (see Figure 2d), these problems can be minimized.[63] Some studies used the metallic

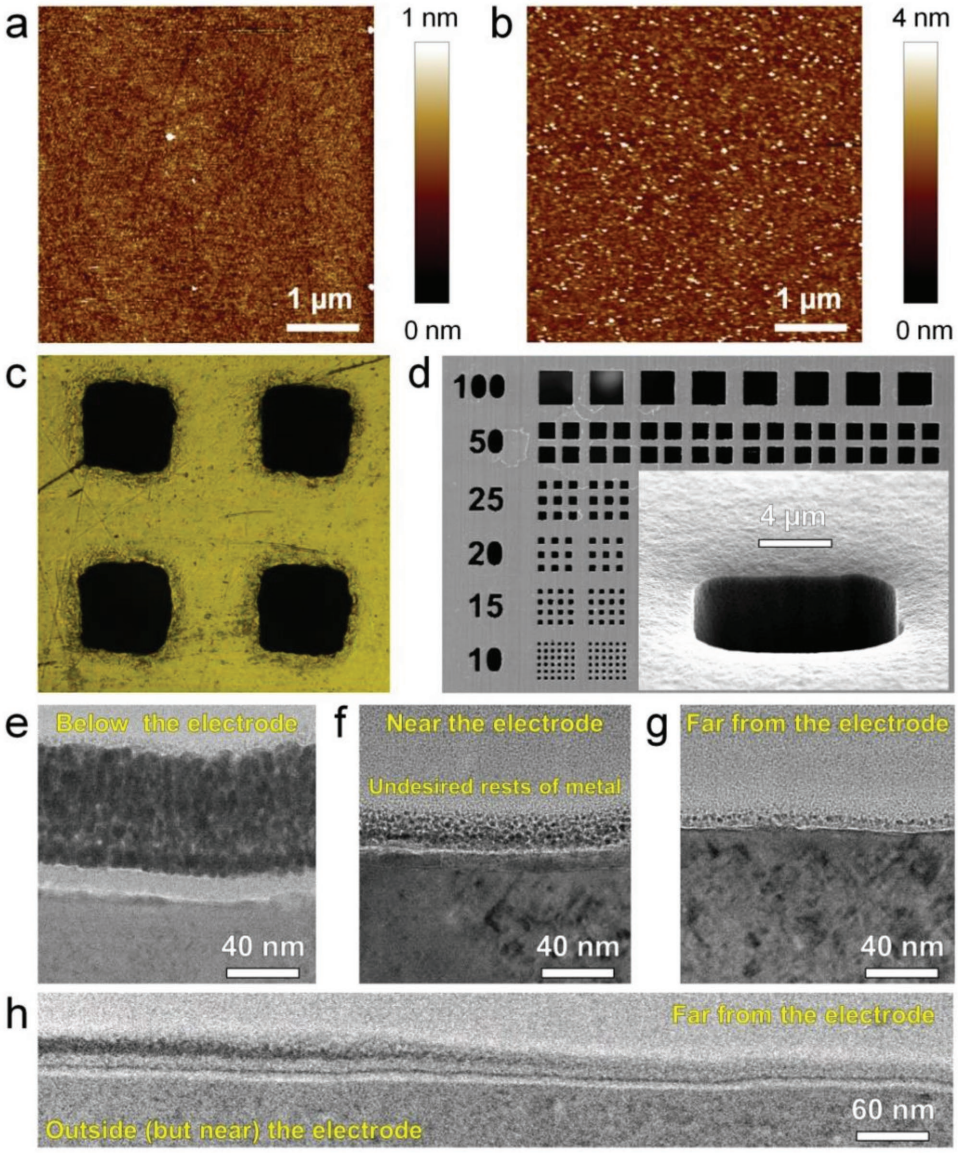

Figure 2. Using photolithography versus shadow mask. Topographic AFM maps of the surface of a Si wafer a) as-purchased and b) after deposition and removal of a photoresist (before metal deposition). Despite intense cleaning, the surface always includes some rests of photoresist residues that are impossible to avoid. c) Optical microscope photograph of a standard shadow mask patterned mechanically. The size of the holes is 50 µm × 50 µm. d) SEM image of a laser patterned shadow mask. The inset shows a zoomed image of the hole. The cross-sectional TEM images collected in a MIM sample like that of Figure 1a, e) below, f) near and g) far from the electrode. h) Large-area SEM image of an area outside (but near) the electrode. Panels (e)–(h) demonstrate that using a shadow mask rests of metal can penetrate below it, propagating below the shadow mask (<1 µm), expanding the area of the electrode laterally in an uncontrolled way.

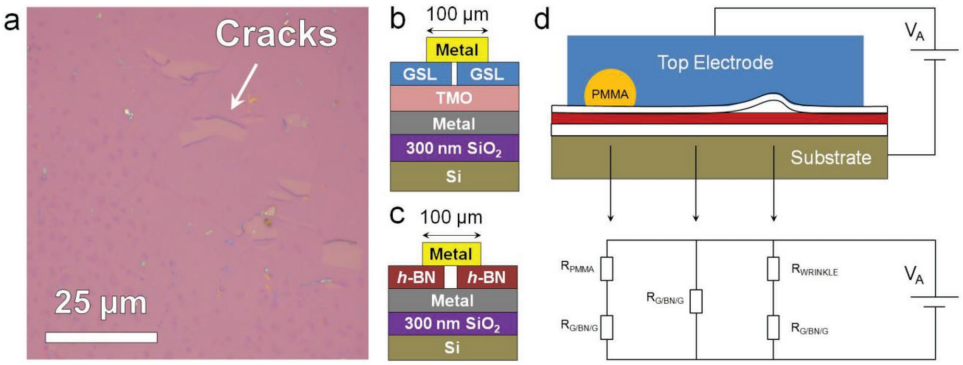

Figure 3. Fabrication issues of RS cells made of 2D materials. a) Optical microscope image of a single layer graphene sheet with several cracks, wrinkles, and multilayer islands. When transferring ≈6 layers thick graphene using exactly the same method a much lower amount of cracks (in some cases even negligible) has been observed. Schematic of b) a metal/*h*-BN/metal and c) a metal/graphene/TMO/metal RS device. If the 2D material is monolayer the formation of cracks is much easier, and this would produce shorted devices in the metal/*h*-BN/metal ones, and accumulation of CFs at the cracks in the metal/graphene/TMO/metal ones. d) Schematic (top) and equivalent electrical circuit (down) of a metal/graphene/insulator/graphene/metal RS cell under bias (V_A). The cell includes one polymer (PMMA) residue and one wrinkle. The schematic indicates that the RS event will never take place at those locations, as the BD (CF formation) takes place at the weakest location of the sample, and these are more resistive.

grids for specimen holder in transmission electron microscopy (TEM) as shadow mask;[77] while this is a clever and cheap way to pattern electrodes with well-defined shapes, it needs to be said that the typical size of the holes in a TEM grid is too large (≈300 μm in diameter), and only one size per sample is available. We note that (for the same lateral size) electrodes patterned on flat surfaces using a shadow mask can be more easily distinguished and contacted in the probe station than those patterned on rough surfaces. We are aware of some studies patterning top electrodes using a shadow mask and silver paint (spread using a brush).[64] It should be emphasized that this process leads to a bad interface and should be avoided by all means.

2.4. Fabrication RS Cells Based on 2D Materials

When fabricating RS devices using 2D materials, additional challenges exist, depending on the process used to synthesize the 2D material. The best quality material is normally achieved by mechanical exfoliation, but this leads to small material flakes (typically <10 μm) with uncontrollable thicknesses,[78] and it requires EBL to pattern the electrodes.[79] This makes it very difficult (if not impossible) to collect statistical information. The two most widespread methods to synthesize 2D materials applied to RS devices are chemical vapor deposition (CVD) and liquid-phase exfoliation.[7]

CVD can be used to grow high quality graphene,[80] molybdenum disulfide (MoS_2),[81] molybdenum diselenide ($MoSe_2$),[82] tungsten disulfide (WS_2),[83] tungsten selenide (WSe_2),[84] and hexagonal boron nitride (*h*-BN),[85–87] among many others. The problem is that the temperature used for the growth is typically >700 °C, which prevents growing the 2D material on wafers with existing integrated circuits due to diffusion problems; the maximum temperature allowed for complementary metal-oxide-semiconductor (CMOS) back-end of line integration is typically 450 °C.[88] Recently, thermally assisted conversion of metallic films at CMOS back-end compatible temperatures has been demonstrated to yield promising layered films, such as platinum diselenide ($PtSe_2$).[89–91] A solution commonly employed is to synthesize the 2D material on the most suitable substrates (metallic foils for graphene[80] and *h*-BN[85–87] and SiO_2 or sapphire for 2D transition metal dichalcogenides (TMDs)[81–83]) and transfer it on the desired sample using different methods,[92–94] being the wet transfer with the assistance of a polymer scaffold the most used by the RS community.[94] However, three main issues need to be taken into account: i) if the 2D layered material is too thin (e.g., monolayer) and the top electrodes are very large (>10^4 μm^2),[95] the 2D material below the TE is likely to contain cracks (see **Figure 3**a). This is not a problem of a researcher doing a wrong transfer, as transferring monolayer 2D materials at wafer scale without producing cracks is (unfortunately) not possible using the current transferring technologies. This is a problem because at those locations with cracks the vertical structure will be less resistive, and CFs will always form there. In fact, the presence of holes and pores in 2D materials has been used to control the location of CFs.[96–98] Therefore, the currents may be flowing across a region without 2D material, and the knowledge extracted may not be applicable to the desired material structure. Nevertheless, if the device size is reduced to <25 μm^2, this problem could be avoided (the density of cracks is not that high). In fact atomically thin RS devices with high I_{LRS}/I_{HRS} ratios >10^4 could be fabricated using several different types of monolayer materials, including *h*-BN and 2D TMDs (of the form MX_2, where M = Mo or W, and X = S or Se).[99] As far as the switching mechanism is concerned, on one hand a filamentary model was proposed based on area-dependent studies,[99] and on the other hand local laser annealing showed that the work function of MoS_2/Ti contacts can be intentionally tuned, leading to a distributed change on the resistivity.[100] Despite these two works are not in conflict, more studies analyzing single layer RS media are necessary. Another way of avoiding the generation of cracks in the 2D material during its manipulation is to use thicker 2D layered stacks, which may be also useful to increase the current I_{LRS}/I_{HRS} in the RS device.[63,101] ii) The transferred 2D material may contain some wrinkles and polymer residue. While wrinkle-free and polymer-free 2D materials are preferred, it should be noted that such locations are more resistive, meaning

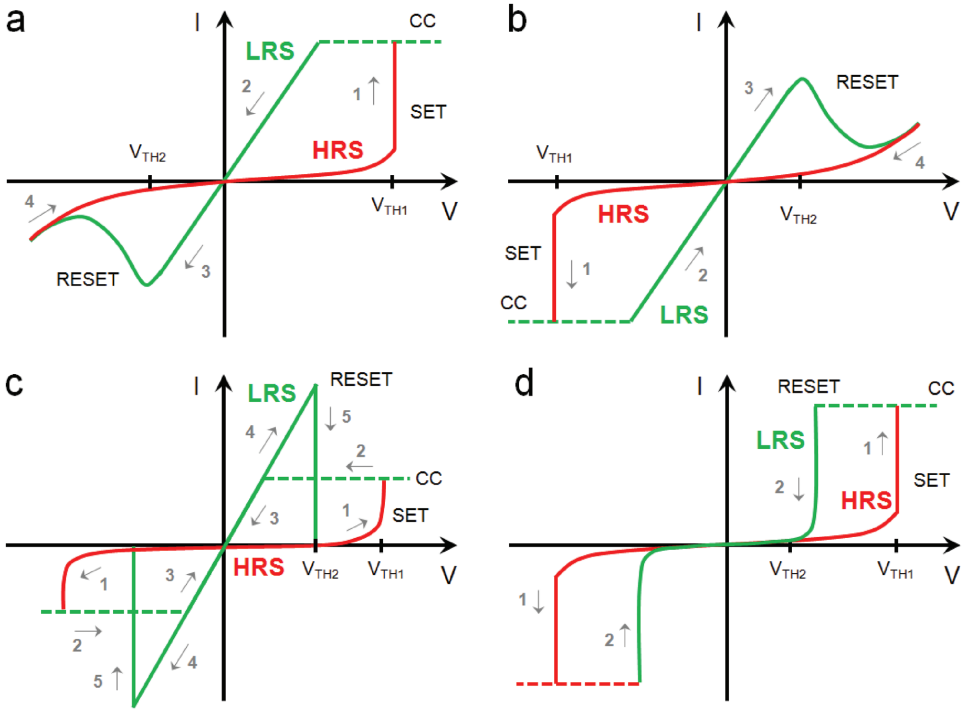

Figure 4. Types of RS characteristics. a,b) Typical *I–V* sweeps showing one cycle of and bipolar RS, inducing the set with positive and negative polarities (respectively). c,d) Typical *I–V* sweeps showing the presence of and unipolar and threshold RS (respectively). For bipolar RS one entire cycle expands to two quadrants of the Cartesian axis (1st and 3rd), while unipolar and threshold are confined to only one, which can be either the 1st (positive set) or the 3rd (negative set). a,c) Adapted with permission.[1] Copyright 2016, Wiley-VCH.

that the CFs will not form there when the electrical field is applied (see Figure 3d). Therefore, the presence of wrinkles and polymer residue in RS devices based on 2D materials can be understood as a reduction of the effective area of the device.[102] It should be also noted that one method to avoid the formation of wrinkles in 2D materials is to enhance the roughness of the substrate where it is transferred.[103] And the third issue is iii) the transferred 2D material may contain several metallic impurities, e.g., from the metallic substrate where it was grown[104] or mobile ions originating from the environment.[105] In ref. [104], it was demonstrated that present transfer techniques could lead to metallic residue concentrations exceeding 10^{13} atoms cm^{-2}, when the maximums allowed by the CMOS industry are below 10^{10} atoms cm^{-2}.[106]

Unfortunately, the CVD growth of graphene and *h*-BN on metal-coated wafers is still very challenging due to metal dewetting at high (>800 °C) temperatures. Reference [107] achieved the growth of *h*-BN via CVD on metal-coated wafers, but only *h*-BN stacks were characterized and no device was fabricated. Some studies tried to reduce the growth temperature of 2D materials, but that leads to much lower quality (which may not be necessarily bad for the fabrication of RS media). More studies in this direction are necessary.

Two additional remarks when working with CVD-grown 2D materials are: first, it is important that the layered structure is confirmed,[7] otherwise the devices may not show the genuine behaviors of these materials—especially important for RS devices is the high thermal conductivity of 2D layered materials. In fact, we are aware of some studies claiming the use of layered graphene and *h*-BN when the cross-sectional TEM images reveal clear amorphous structure.[108,109] And second, RS devices using planar (lateral) graphene[110,111] and MoS_2[112,113] structures have been reported; however, these structures are not sufficiently compact for realistic applications, and the mechanisms (electromigration, grain boundaries modification) cannot be controlled accurately. For these reasons, planar resistive switching configurations have not raised the interest of the industry.

When the 2D materials are assembled by liquid-phase exfoliation, the main concern is the same as when using other spin-coated materials: process and roughness induced variability (see Section 2.3). For this reason, in RS studies using spin-coated 2D materials, it is extremely important to include variability information.

3. Device Characterization

When studying the RS performance of MIM cells, the way in which the electrical characteristics are collected is critical for making a correct interpretation. Normally the electrical tests are carried out in a probe station, and the most common figure of merit is the collection of two current versus voltage (*I–V*) sweeps: one showing the set and another showing the reset process (see **Figure 4**). To do so, one of the electrodes in the MIM cell is grounded, and a ramped voltage stress is applied to the other one.[1] In most cases, the use of a current limitation (CL) is necessary in order to limit the energy delivered (and damage

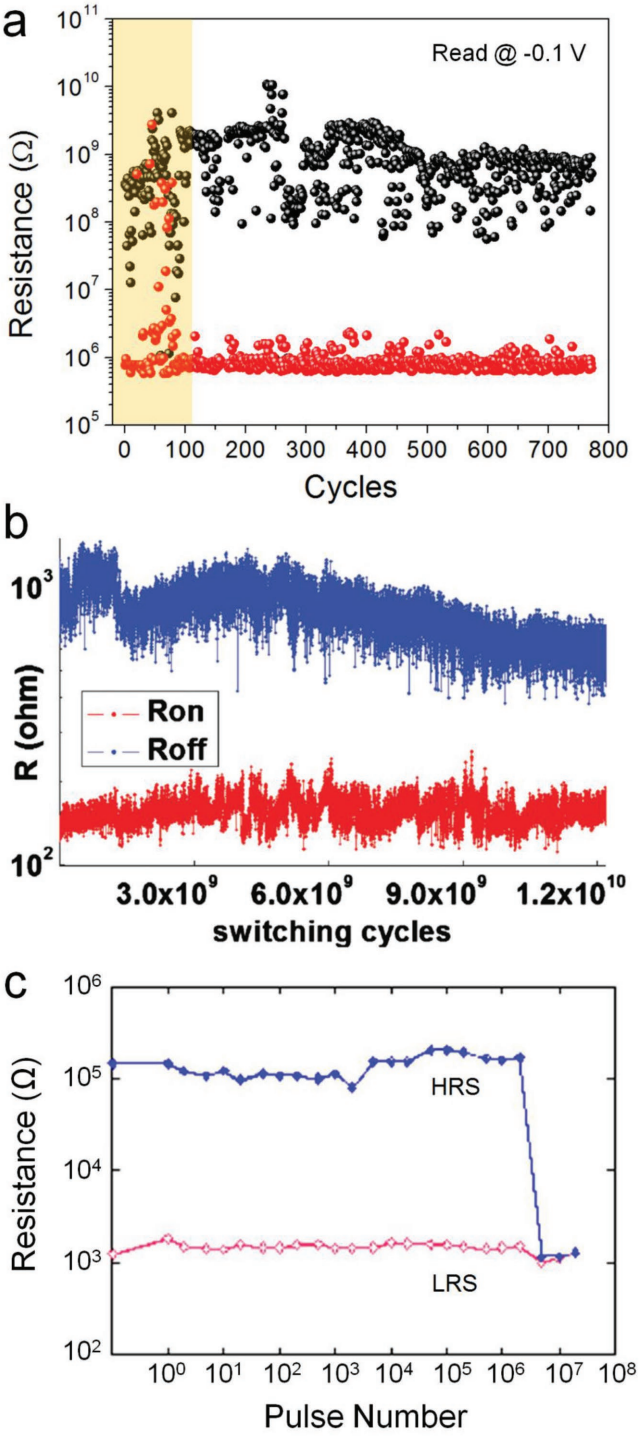

Figure 5. Endurance plots collected by three different methods. a) By measuring several *I–V* curves and extracting the resistance at −0.1 V. b) By using pulse stresses recording the current simultaneously and calculating the resistance for each cycle (namely current-visible PVS). c) By using pulsed stresses without measuring the current simultaneously (namely current-blind PVS). The resistance is extracted by stopping the tests and collecting one *I–V* curve, and extracting the value of the resistance in that specific cycle. Method (a) is too slow and the stresses applied do not correspond to the real functioning of the devices, although it can prove switching in each single cycle. Method (c) is faster and uses realistic stresses, but it cannot properly prove the switching in all the cycles. Method (b), which is the recommended one, is faster than (a) and proves the switching in each single cycle. a) Reproduced with permission.[9] Copyright 2017, Wiley-VCH. b) Reproduced with permission.[116] Copyright 2010, American Institute of Physics. c) Reproduced with permission.[13] Copyright 2007, American Institute of Physics.

introduced) during the BD, otherwise the stress may lead to an irreversible BD and no reset would be detected in subsequent *I–V* sweeps.[1] However, this observation (proof-of-concept) is not sufficient for understanding the nature and quality of the RS phenomenon in a MIM cell, and several other figures of merit including endurance, data retention, switching time, power consumption, variability, scalability, and charge transport mechanism must be studied as well. In addition, it is important to note that *I–V* sweeps do not match the operating conditions of realistic devices, which work under short (<100 ns) pulsed voltage stresses (PVS).[1] In the following sub-sections, all these figures of merit and the most suitable methods to acquire them are discussed in detail.

3.1. Endurance

In a RS, device endurance is defined as the number of times it can be switched between two (or more) resistive states keeping enough resistance ratio between them.[3,7] Therefore, an endurance test consists of finding out what is the maximum number of set/reset transitions (cycles) for which RS phenomenon with enough current on/off ratio can be measured, and its common figure of merit is the R_{HRS} and R_{LRS} versus cycle (see **Figure 5**). The failure of the device may not happen in one specific cycle, but it may be progressive.[114] Therefore, one needs to set up a threshold current on/off ratio below which the device is considered to have failed. However, the criterion to define RS device failure may be different depending on the application. In ref. [115], the authors defined an I_{ON}/I_{OFF} ratio of 5 for considering device failure. While this may be perfectly fine for their application, other authors may consider it inadequate for other cases.

The endurance characteristics of RS cells can be obtained by performing different experiments, three of them being the most common: i) *I–V* sweeps, ii) current-visible PVS, and iii) current-blind PVS. The first experiment consists of the collection of sequences of *I–V* sweeps in a single RS cell (like those in Figure 4), and the subsequent extraction of R_{HRS} and R_{LRS} dividing a selected read voltage (typically ±0.1 V[9]) by the corresponding currents observed in the *I–V* sweeps at that voltage (see Figure 5a). This method is reliable because one can ensure the correct switching of the device in each cycle. A challenge is that this method is very slow, because the time required for collecting an *I–V* sweep can be very long (≈30–60 s), especially if low currents (<1nA) are measured. Moreover, the *I–V* sweep method does not match the stresses applied to realistic devices (they operate via PVS), and therefore the data presented using this method may not be strictly representative of the endurance of the same RS cell under real operation conditions.

The second experiment consists of the application of a train of PVS, in which the user can modify the voltages (V_{UP} and V_{DOWN}) and times (t_{UP} and t_{DOWN}), and simultaneously measure the currents driven[116] (namely, current-visible PVS

method). Normally one pulse with large V_{UP} ($|V| > 1$ V) is used to set/reset the devices, and read pulses are intercalated to read the conductance of the RS cell after each stress ($V_{READ} = 0.1$ V). Then, the values of R_{HRS} and R_{LRS} can be calculated for all test cycles (as in the *I–V* sweeps method, see Figure 5b). The current-visible PVS method is much faster than the *I–V* sweeps because the pulse widths can be of the order of microseconds, which allows collecting millions of cycles in few minutes; moreover, this method matches well the functioning of realistic devices. A challenge is that the PVS method often requires advanced hardware; for example, the Keithley 4200 SPA (equipment commonly used by many groups for these tests) requires an additional module to do this experiment, which involves additional cost. Moreover, several SPA cannot measure low currents <10 μA during pulse mode operation (i.e., that is the noise level during pulse mode operation), which could be a limitation when characterizing devices with high R_{HRS} (>10 kΩ).

The third experiment consists of the application of PVS but without measuring the current simultaneously (namely, current-blind PVS). After a specific number of PVS cycles without measuring the current, the stress is stopped and the resistivity of the RS cell is measured in DC mode or collecting an *I–V* sweep. This method does not require advanced hardware, all commercial SPA (and even pulse generators) can do this experiment, and it is as fast as the normal PVS that measures the current in each cycle. The endurance characteristics collected using this method can be clearly distinguished because the data points are very spaced[13] (see Figure 5c). However, unlike the *I–V* sweep and PVS methods, the current-blind PVS method cannot ensure that 100% of the pulses applied actually induced state transitions in each cycle. For example, ref. [13] claims RS during more than 10^6 cycles, but only 24 data points for each resistive state are displayed; the same happens for ref. [117], in which an endurance of 10^7 cycles is claimed, but only 70 data points are displayed. Actually, refs. [13] and [117] did not explain if they measured the current during each cycle, but we assume that they used current-blind PVS due to the low amount of data points displayed—if one measures the current in each cycle and has the data, surely he/she will display them, as the authors in ref. [116] did (see Figure 5b). For this reason, the current-blind PVS method should only be used in very well optimized technologies at the industrial stage, and scientists based in universities and research institutes should avoid the use of this method to characterize the endurance of their prototypes. It is important to understand that using current-blind PVS to evaluate the endurance of incipient RS cells (such as RS cells based on 2D materials[117]) is not a reliable choice, as that can easily produce endurance overestimation; therefore, the endurance values reported in such kind of studies (e.g., refs. [13] and [117] although there are many others) should be further corroborated using the current-visible PVS method (i.e., measuring the current in each cycle).

Another issue that may affect the endurance of the cells is the relaxation time during the *I–V* curves or pulses. Normally the larger the relaxation time, the higher the endurance measured. Therefore, it might be possible that endurance tests using *I–V* curves and current-blind PVS may result on higher endurances than the normal PSV method. Some works have applied triangular or sinusoidal signals (no relaxation time) to switch RS devices,[118,119] but to the best of our knowledge this method has been only used for proof of concept switching, not for endurance tests. It should be highlighted that when measuring extreme endurances up to 10^{12} cycles even current-visible PVS method could still be too slow. For example, considering that monitoring one entire RS cycle via current-visible PVS method takes ≈1 ms (including the duration of the first read pulse, set pulse, second read pulse, and reset pulse, plus the time distance between them), the time required to measure endurances of 10^9, 10^{10}, and 10^{11} cycles would be 11.5, 115, and 1157 days (respectively). An acceptable method to characterize extreme endurances is to monitor the switching of each cycle during the first 10^6–10^7 cycles using current-visible PVS method, and then shift to PVS-blind method (collecting a decent amount of ≈50 points per decade). Reducing a bit the time of the read, set and reset pulses are recommendable when measuring extreme endurances.

Currently, RS devices with endurances up to 10^{12} cycles have been reported in different types of MIM cells, including Pt/Ta_2O_{5-x}/TaO_{2-x}/Pt[120] and Ta/TaO_x/TiO_2/Ti.[121] In this sense, there is consensus that tantalum oxides seem to be the RS medium providing the best endurances.

3.2. State Retention

Studying data retention of a nonvolatile RS device consists of checking if the LRS and HRS are stable over time after the set and reset transitions (respectively).[3,7] To do so, after inducing the set/reset transition (either by an *I–V* sweep or a PVS) the state retention can be studied by applying a constant voltage stress (CVS) over time using a low (≈0.1 V) read voltage, and subsequently measuring a current versus time (*I–t*) curve for each resistive state.[22] Therefore, the figure of merit for state retention analysis is the *I–t* curve, which is normally accompanied by the voltage used during the read *I–t* curve (often indicated either inside the plot or in the figure caption, see **Figure 6**a). Normally the challenging point is to keep a long retention time in LRS, as the atomic rearrangements introduced during the set stress may vanish over the time. On the contrary, in HRS normally the retention is not a concern because that is normally the natural state of the device, and if no or low bias is applied the device should remain in it. It should be noted that in most RS devices the retention in LRS strongly depends on the CL used during the set transition.[22] For example, in CF based RS devices, a larger CL during the set *I–V* sweep produces a larger CF that is more stable over the time,[122,123] which will enlarge the state retention time detected in the subsequent *I–t* curve.[22] Therefore, in order to correctly evaluate the retention time detected in LRS (and compare among different works), the CL used during the set process (*I–V* sweep or PVS) should be indicated next to the *I–t* plot.

The desired data retention for RS-based NVM technologies is 10 years at 85 °C.[3,7] Obviously, state retention tests of 10 years are not doable, and for this reason normally much shorter times of few hours or days are reported.[124,125] We are aware of some reports that measured retention of few hours or days, and projected trends up to 10 years.[126,127] Doing consistent reliability projections of specific parameters of electronic devices is acceptable; for example, the time-dependent dielectric breakdown of gate insulators is normally projected over years, and this assumption is based on data obtained from stresses at voltages much larger than in real operation conditions.[128] However,

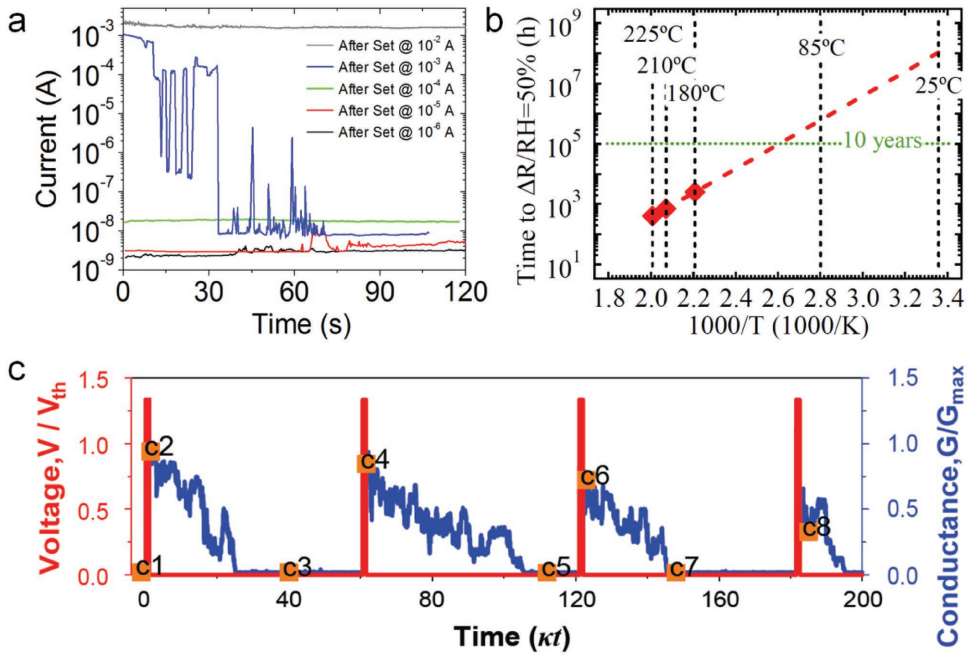

Figure 6. Measuring the retention and relaxation times of RS devices. a) *I–t* curves, collected using V_{READ} = 0.1 V, showing the retention of the LRS; as it can be observed, it strongly depends on the current limitation used. b) Arrhenius plot of data retention properties of TaO_x memory cells. c) Use of pulsed tests to monitor the relaxation of RS devices showing threshold type RS. This test is especially useful to study RS devices for neuromorphic applications and short term plasticity. a) Reproduced with permission.[22] Copyright 2018, IEEE. b) Reproduced with permission.[129] Copyright 2008, IEEE. c) Reproduced with permission.[134] Copyright 2017, Springer Nature.

several reports in the field of RS do not conduct any aggressive stress that allows doing such extrapolation. Therefore, such extrapolation is not accurate and should be avoided. One correct methodology to evaluate the retention of RS devices in aggressive conditions is to increase the temperature during the CVS applied to obtain the *I–t* curve.[129] At high temperatures, the atoms in the MIM cell acquire energy, which facilitates atomic rearrangements;[130] therefore, the retention measured in LRS at room temperatures will always be larger than that measured at higher temperatures. If this method is used, the temperature applied during the *I–t* curve measured to characterize the endurance should be indicated (as well as the read voltage). Actually, the best would be to measure the retention at several (preferably elevated, >80 °C) temperatures and extrapolating such data points, given any failures were observed[131] (see Figure 6b). Moreover, in several MIM cells the retention failure (i.e., the unwanted transition from LRS to HRS) occurs suddenly,[132] meaning that elaborating predictions based on short-times *I–t* curves may be a bit risky. A projected endurance of 10 years has been reported based on *I–t* curves collected at 85 °C in Pt/TaO_x/Pt[129] and Pt/Al_2O_3/HfO_2/Al_2O_3/TiN/Si.[133]

It should be noted that threshold-type RS devices are those in which the RS is volatile, i.e., the retention time ranges from some microseconds to few seconds. Studying the retention time of threshold-type RS devices is interesting in the field of neuromorphic computing, as they are suitable to emulate short-term plasticity learning rules because the retention time of the RS cell can be also interpreted as the relaxation time of an electronic synapse.[22] If the relaxation of the BD takes place in seconds or faster (down to microseconds), measuring an *I–t* curve after the set stress (*I–V* sweep or PVS) may produce important information loss, as some non-negligible time passes between the end of the set stress and the read *I–t* curve. In this case, the recommended methodology to detect the relaxation of the BD event is to apply one or few PVS (to set the device) and keep measuring the current (at 0[134] or 0.1 V[22]) after it. As the current measurement is not interrupted after the stress, the real relaxation process of the threshold device can be accurately studied (see Figure 6c). Unfortunately, most reports studying relaxation time of electronic synapses did not include information about the variability of the relaxation time. In ref. [135], the authors measured the relaxation time of Ti/*h*-BN/Au threshold-type RS devices during more than 500 cycles, and the variability of the relaxation time observed was strikingly low (<10%, see Figure 6d).

3.3. Switching Time and Energy Consumption

Studying the switching time and energy consumption (per state transition) in RS devices requires the application of PVS to the RS devices. Due to the positive feedback of the filament formation on the current, the forming and set transitions of RS devices are not self-limited. Therefore, careful electrical switching characterization requires a current limiting element in the circuit.[136] To limit parasitic capacitance effects during transient, it is required that this element is integrated in situ close to the RS device.[52,137,138] A transistor is commonly used for this in the well-known 1-Transistor/1-Resistor (1T1R) structure.[52,138] However, due to the strong nonlinearity of the

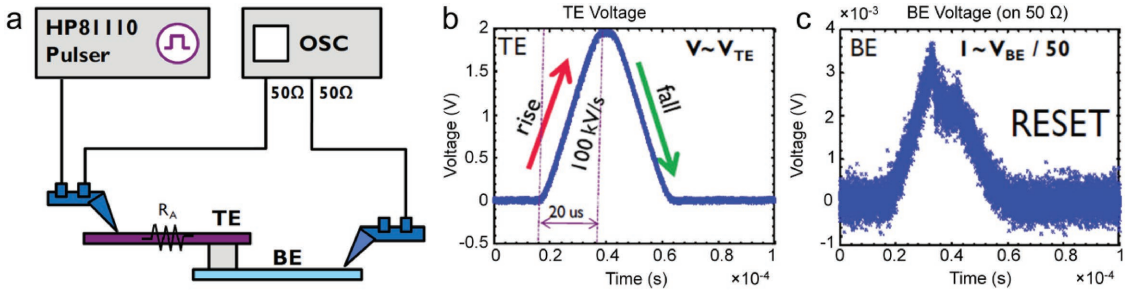

Figure 7. Switching time and energy consumption. a) Schematic of the setup recommended for the characterization of the switching time and energy in RS devices. The bias is applied using a pulse generator, and a series resistor is used to limit the current across the device in LRS. b) Voltage and c) current signals can be measured with the oscilloscope. Reproduced with permission.[139] Copyright 2012, IEEE.

current versus source–drain voltage, it is far more convenient to use an integrated load resistor as current limiter (in a so-called 2R structure) if we aim at extracting the actual voltage dropped on the resistive element ($V_{RS.DEV}$) during switching.[139] This applies particularly to the characterization of the power consumption of a resistive device.

In this respect, an appropriate setup would include a fast pulse generator, allowing to apply square or triangular pulses to one electrode of the 2R device structure, and a high-bandwidth oscilloscope, allowing to simultaneously acquire both the applied voltage and the transient current (see **Figure 7**).[139] The applied voltage is acquired on one channel of the oscilloscope connected to the TE, while the current is read-out by connecting the BE in series to the 50 ohm impedance-matched input resistance of the oscilloscope and converting into current the voltage generated on this shunt resistor—it is important to consider the shunt resistance and parasitic capacitance of the instruments used for electrical characterization, especially when using additional elements (e.g., transistor, resistor). Waveforms of both channels are then numerically processed to remove residual offset and noise. In this setup, the use of the 2R structure allows to calculate at any time the actual voltage $V_{RS.DEV}$ dropping on the resistive device.[139] In order to also extract the V_{SET} and V_{RESET}, it is convenient to apply triangular voltage ramps (see inset in Figure 7). The switching energy may then be calculated by integrating the current and voltage traces over time on the oscilloscope.

Using this methodology, the switching energy may be characterized for different operating currents by means of load resistors with various resistance magnitudes. On the other hand, minimum switching energies may be characterized by applying short pulses with high ramp rates.[3–7] Typically, the switching transient is of the order of a nanosecond, and the required switching time for stable filament set and reset lies in the range of a few nanoseconds.[52,138] For a set experiment, we observe that after the set transition voltage snapback, $V_{RS.DEV}$ stabilizes at a constant voltage during the transient (V_{TRANS}). V_{TRANS} is an intrinsic parameter for a given resistor; it was observed to depend neither on the operating current nor on geometrical factors.[139] Moreover, V_{TRANS} varies only slightly in the range 0.4–0.7 V for a wide range of oxide-based resistive devices.[138–140] This means that the transient energy may be fairly approximated by multiplying the transient current by ≈0.5 V. Hence, for an operating current of 100 µA, typical set energy and power lie in the range of ≈1 pJ and 50 µW, respectively. For the reset transition, it was observed that the maximum reset current is similar to the maximum set current, while the reset voltage equals V_{TRANS}, meaning that the reset energy is similar to the set energy.[139] Note that this is a general but not systematic observation. For example, conductive bridge devices typically deviate from this behavior and exhibit different set and reset energies.[141]

3.4. Variability

The spatial (cell-to-cell) and temporal (cycle-to-cycle) variation of the electrical characteristics (i.e., V_{SET}, V_{RESET}, I_{HRS}, I_{LRS}) of RS devices is still by far the most challenging obstacle toward widespread deployment of such devices in memory and computing applications. However, it is true that variability may be exploited for the development of useful systems, such as true random number generators and physical unclonable function devices for security applications. In the field of neuromorphic, computing the effect of variability is still under debate. Reference[142] suggested that variability may be useful for stochastic computing, although this work used a threshold device. More works in this direction are necessary. Nevertheless, cell-to-cell and cycle-to-cycle variability is a major problem to be avoided in RS devices for information storage.

The main problem of the literature available in the field of RS is that the lack of statistics often generates misleading information about the quality and stability of the memory window, leading to an excessively optimistic estimation of device performance. While cell-to-cell variability is something that could be solved by improving the fabrication process (i.e., providing homogeneous interfaces, identical sizes), the observation of large cycle-to-cycle variability is intrinsic in the physics of the device, and therefore influenced by the electrical stresses applied. The formation and rupture of a CF is a stochastic process, and for that reason predicting and controlling the shape of the CFs (which is the key factor defining the electrical properties of the RS devices) is extremely challenging. For this reason, all RS studies should include information about variability and yield. Even when the authors show such information, comparisons are difficult because variability studies in RS devices may

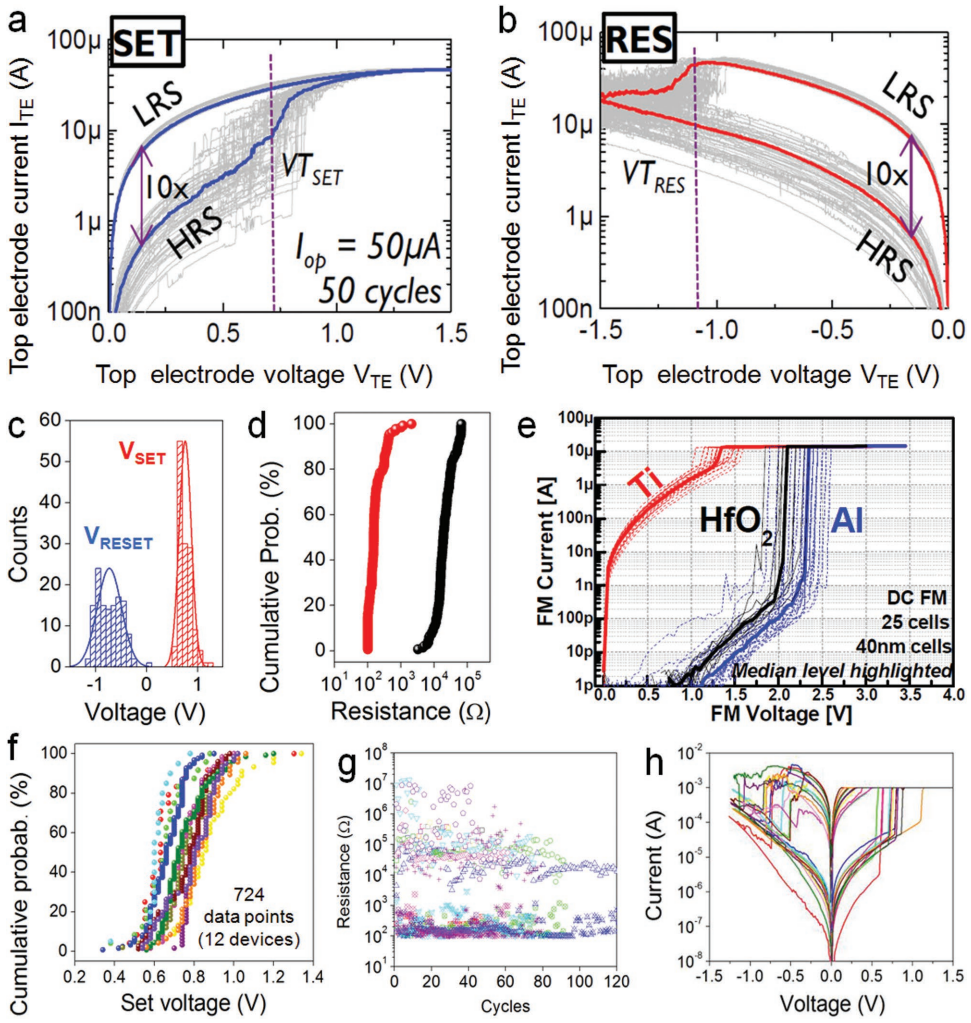

Figure 8. Statistical analyses to evaluate the variability of RS devices. a,b) *I–V* sweeps showing the typical bipolar RS behavior during 100 cycles. c) The histogram of V_{SET} and V_{RESET} for 100 *I–V* sweeps measured in a RS device. d) The histogram of R_{HRS} and R_{LRS} for 100 *I–V* sweeps measured in a RS device. e) *I–V* sweeps collected in different groups of devices; the median of each group (Ti, HfO_2, Al) is highlighted in bold. f) Superimposed cumulative probability plot of V_{SET} for 12 different RS devices. g) Endurance plot of 7 RS devices superimposed (empty symbols correspond to R_{HRS} and crossed symbols to R_{LRS}). In this plot only 100 cycles have been plot for clarity, as the goal is to analyze the variability. In all the panels of this figure the composition of the MIM-like RS device are irrelevant, the important is how the information (e.g., V_{SET}, V_{RESET}, R_{HRS}, R_{LRS}) is displayed. h) Median *I–V* sweep of 15 devices; for each device at least 100 cycles were measured. a,b) Reproduced with permission.[143] Copyright 2014, IEEE. e) Reproduced with permission.[144] Copyright 2014, IEEE.

differ a lot from one group to another, as there is no consensus on a typical figure of merit, nor standard variability limits established by the industry.[3,7] Here, we propose the figures of merit indicated in **Figure 8** as a method to evaluate variability in RS devices.

In the case of cycle-to-cycle variability, the endurance plot may be useful to understand how I_{HRS} and I_{LRS} change from one cycle to another (see Figure 5), but that gives no information on V_{SET} and V_{RESET}. A good example of cycle-to-cycle variability characterization is reported in ref. [143], where several cycles were visualized (see Figure 8a,b). Recommended methods for studying the variability of the switching voltages and resistances are to plot the histogram (Figure 8c) or cumulative probability plot (Figure 8d) of each parameter. This allows to easily evaluate their value and deviation, which is very valuable information when designing the threshold level to distinguish both HRS and LRS. Figure 8d offers a clear example of the reduction of the memory window when large statistics are considered. The graph clearly shows that, while the median window is ≈100×, no window is present between the tails of the two distributions. When analyzing cell-to-cell variability, one good method is to measure several cells and highlight the median characteristic (see Figure 8e).[144] However, in Figure 8e the information about the cycle-to-cycle variability is masked. In order to solve this problem, here we suggest some additional characteristics. One is to analyze V_{SET} and V_{RESET} variability by showing the cumulative probability plot of these parameters for each device superimposed (see Figure 8f). This plot is interesting because it allows fast visualization of the variability within one single device and from one device to another. When analyzing the cell-to-cell variability of R_{HRS} and R_{LRS}, one option may be showing an endurance plot with the data corresponding to several devices superimposed (as in Figure 8g), or

showing the median characteristics together with an error bar for each data point, where the bar size represents the interval (as done in ref. [145]). The latter enables to have a visual estimation of the cell-to-cell variability without crowding the plot with an excessive number of traces. Another possibility is to measure several (>100) *I*–*V* sweeps for different devices and plot together their median *I*–*V* sweep (see Figure 8h).

Switching variability has a strongly detrimental effect on the multilevel operation, which was initially considered one of the main advantages of RS technologies. The multilevel capability has been reported for a large plethora of RS devices, mainly thanks to the analog dependence of R_{LRS} (R_{HRS}) on the I_{SET} (I_{RESET}). Programming algorithms like incremental step pulse programming[146–148] and closed-loop pulse switching[60,149] have allowed a better control of the multilevel operation in RS devices. However, in the vast majority of cases, the multilevel operation is reported either on single devices or for median resistance levels. When large cycle-to-cycle and cell-to-cell statistics are considered, the distinction between the distribution tails of adjacent levels (bits) fades, strongly frustrating the multilevel operation. The deleterious effect of variability on the multilevel operation can be tackled from different perspectives. For the cycle-to-cycle (intrinsic) variability, which is related to the stochastic nature of the resistive switching mechanisms, program or verify algorithms can be implemented in the external circuitry to set two resistance boundaries for each level of operation. This increases the design complexity and the total write time. On the other hand, cell-to-cell variability, which is process-related, can be improved by aiming at a better uniformity across the wafer for the different integration steps. However, even when the programming variability can be strongly limited with the abovementioned solutions, the temporal variability hinders the multilevel operation. As reported in ref. [150], even when program or verify algorithms are used to force the resistance below or above certain levels, the spontaneous rearrangement of the defects leads to an unpredictable drift of the resistive state. Considering all the effects reported in this paragraph, the multilevel operation is nowadays considered extremely challenging to implement in RS devices.

3.5. Scalability

This is probably one of the most critical points in RS technologies and research. Researchers frequently report the RS behavior measured (via probe station) in devices with very large areas, of the order of 100 μm × 100 μm,[64,75] with a characteristic structure like that shown in Figure 1a (common BE). However, observations made in these devices may not be applicable to nanoscale devices, because the BD and RS are stochastic processes that take place at the weakest location in the total volume covered by the RS medium; statistically, larger devices (areas >25 μm^2) will show characteristics closer to those of dielectrically weaker locations, while real nanoscale devices (areas <100 nm^2) will show characteristics closer to dielectrically stronger locations. As an example, it has been demonstrated that smaller device areas lead to higher forming voltages.[22,59] Different forming voltages generate CFs with different sizes across the RS device, which strongly affects its characteristics and lifetime.

For these reasons, it is always highly recommended to report the characteristics of RS devices for different device areas. The most recommendable is to go down to the nanoscale range, although that may be complex because the standard photolithography tools used in most universities and research institutes can only pattern devices with minimum lateral sizes of few micrometers (≈3 μm). One option to pattern smaller devices is the use of EBL,[52] but that may be more time consuming. In addition, the percentage of devices successfully fabricated (yield) via EBL is normally lower, as the removal of the polymer mask after metal deposition (lift-off process) may damage or detach the patterned metallic electrodes. Nanometer-scale RS devices have also been obtained using carbon nanotubes as the bottom electrode,[151] or at the cross-point of two single-wall carbon nanotubes.[152] The latter cell areas are of the order of 1 nm^2 (limited only by the small nanotube diameter) and they represent the ultimate lower limit of RS cell dimensions. Their drawback is the difficulty in fabrication, and to date only individual devices[151,152] but no device arrays could be fabricated with this approach.

Another option is the use of local characterization tools, such as scanning tunneling microscopy (STM)[28,153] or CAFM.[154] In this case, the electrical stress can be applied to the STM/CAFM tip, which is placed directly on the RS medium (no TE deposition is necessary) to play the role of nanoscale TE (see **Figure 9**a). Using STM, lateral atomic resolution has been achieved when measuring ultrathin materials, like graphene[155] (a conductor) and *h*-BN[156] (an insulator). However, such extraordinary ability has never been proven when studying an RS medium. STM has been used to detect enhanced conductivity at the edges of columnar structures in pristine, sputter-deposited silicon-rich SiO_2 (SiO_x where $x \approx 1.3$).[157] Reference [157] demonstrated the possibility of switching in a wide spectrum of transition metal oxides using STM. Other studies include investigations of more advanced material systems.[28,158–165] Although STM may provide better lateral resolution than CAFM due to the smaller tip radius and its operation in ultrahigh vacuum, STM presents three important problems limiting its use in RS studies: i) the samples need to show some intrinsic conductivity prior to switching, otherwise it is impossible to measure tunneling current. This dramatically limits STM studies of resistance switching to conductive, leaky, or very thin materials; ii) the tip–sample distance is measured by evaluating tunneling current across the sample. This is a problem when measuring lateral scans, as one cannot know if a current increase or decrease is related to a change in the conductivity of the material (presence or absence of defects) or to a local topographic fluctuation of the RS medium; and iii) it is widely accepted that trustable STM measurements need to be done in ultrahigh vacuum, which enormously increases the complexity and slows down the overall experiments.

CAFM is a more practical tool that can easily distinguish between topography and conductivity changes, as they are measured independently (the first one using an optical or piezoresistive system to detect the deflection of the cantilever containing the probe tip, and the second one using a current-to-voltage preamplifier[154]). In CAFM experiments, the effective area at the tip/sample junction (A_{eff})—this is not the contact area, but the area across which the electrons can flow, which

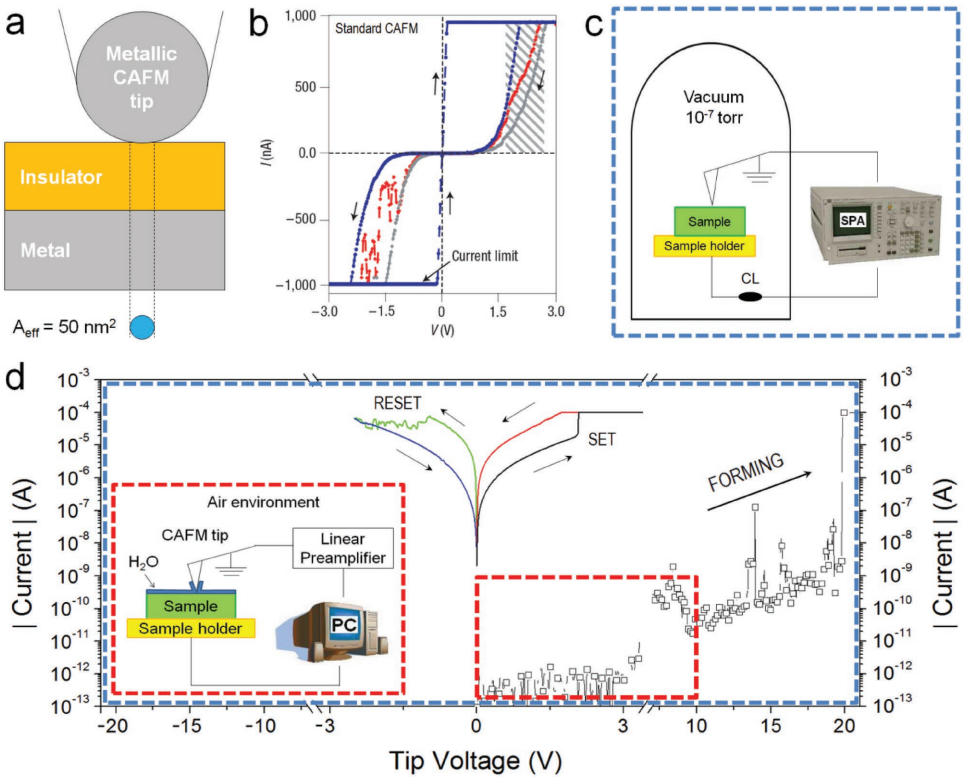

Figure 9. Nanoscale study of RS using CAFM. a) Schematic of a nanosized MIM structure using the tip of the CAFM as top electrode. b) Typical IV curves collected with standard CAFMs showing RS. The set and reset processes cannot be observed, just shifts in the *I–V* curves. c) Block diagram of an SPA connected to a CAFM tip working in vacuum for nanoscale bipolar RS characterization. This is the recommended setup for nanoscale RS characterization. d) *I–V* curves showing bipolar RS behavior, which have been collected with the setup shown in panel (c). The blue dashed line is the voltage and current range covered by the setup shown in panel (c). The inset shows the block diagram of a standard CAFM, which can only measure the current range highlighted with red dashed lines. b) Reproduced with permission.[233] Copyright 2006, Springer Nature. c,d) Adapted with permission.[47] Copyright 2014, The Electrochemical Society.

can be different[154]—may range between 1 and 700 nm^2, depending on the radius of the tip, stiffness of tip and sample materials, tip/sample contact force, and relative humidity of the environment,[45] being ≈50 nm^2[166] the most common/accepted value. Therefore, the CAFM can be used to prove the presence of RS in ultrascaled MIM cells. When performing sequences of *I–V* sweeps to explore RS with a standard CAFM, some essential factors need to be considered: i) most commercial AFMs do not allow applying voltages above ±10 V, which hinders the observation of the forming process in several samples; ii) most standard CAFMs just measure currents within 2–4 orders of magnitude. This makes visualizing the set and reset processes impossible, and only the shifts of the *I–V* sweeps (and their curvature change) can be detected (see Figure 9b). To solve these problems some manufacturers offer the possibility of using a logarithmic preamplifier[167–170] for current evaluation, but that module is expensive and not compatible with all CAFMs; iii) no CAFM can apply variable current limitation, which may produce undesired damage during the set process. It should be noted that most CAFMs show current saturation (see horizontal line in Figure 9b), but that not necessarily limits the current flowing across the tip/sample junction;[171] iv) measuring bipolar RS in metal oxides using a standard CAFM working in air conditions is very challenging because the relative humidity of the environment produces a water meniscus at the tip/sample junction, which leads to local anodic oxidation of the metal oxide.[172,173] Problems i), ii), and iii) can be solved by connecting an SPA directly to the CAFM tip and sample holder, while problem iv) can be solved by measuring in dry N_2 or vacuum atmospheres, which minimize the formation of a water meniscus at the tip/sample junction. The suggested CAFM setup for studying RS via sequences of *I–V* sweeps is displayed in Figure 9c.[47] Using this setup, both forming and cycling can be in situ monitored (see Figure 9d).

It is important to highlight that the CAFM cannot perform reliable endurance tests locally. The reason is that the tip of the CAFM experiences lateral thermal drift,[174] which slowly moves it to a different location; we characterized the thermal drift to be ≈10 nm h^{-1}, although it may differ a lot from one CAFM to another. Moreover, in many cases RS involves large currents up to ≈1 mA, which implies a current density at the tip/sample junction of ≈10^9 A cm^{-2}, as A_{eff} is ≈100 nm^2.[175] These ultrahigh current densities are very harmful for all CAFM tips, and there is no tip capable of resisting such aggressive stress, even when using solid conductive tips[46] (which may lose their sharp shape due to material melting, and even adhesion of particles at the apex due to thermochemical reactions, which kills their conductivity). For these reasons, the maximum number of RS cycles collected at a single location with a CAFM reported is 100;[176,177] therefore, the CAFM is an excellent

tool for elucidating which locations of the sample show RS, but not enough reliable for conducting endurance tests. In refs. [48,49], a CAFM working in dry N_2 and connected to an SPA was used to demonstrate that the RS in polycrystalline HfO_2 stacks only takes place at the grain boundaries, which are rich in defects.[178] Another important consideration is that the RS parameters measured with the CAFM tip (i.e., V_{SET}, V_{RESET}, I_{HRS}) may vary a lot depending on the measurement conditions (i.e., environment,[45,179,180] tip diameter,[166] contact force[181]). Therefore, fitting one single *I–V* sweep collected with a CAFM to any tunneling equation is meaningless; such fittings should always be performed statistically.[43,182]

Similar to the sequences of *I–V* sweeps, the RS can also be studied from sequences of current maps.[183–185] The advantage compared to sequences of *I–V* sweeps is that the current maps can test much larger areas (typically 1 μm × 1 μm to 10 μm × 10 μm), which allows performing statistical analyses of the size and currents driven by the CFs.[184] Moreover, as the area in which the RS takes place is larger, this can be combined with chemical tools, such as energy dispersive X-ray spectroscopy or X-ray photoelectron spectroscopy, to study the chemical changes involved in the switching.[183]

Another interesting possibility is the application of set/reset stresses at the device level and later analyze the local conductivity changes via CAFM maps. Measuring current maps by placing CAFM tip on the metallic electrode is not a good choice because that may blur the shape and currents driven by the CFs due to the large lateral conductivity of the metal; in other words, the currents driven by one spot can be detected even when the tip is placed on the metal far from it,[186] leading to a false CF size. Therefore, the top electrode needs to be removed before the CAFM scan. The main two options reported are: i) removing the top electrode via standard dry[187] or wet[185,188] etching. In fact, this was the first type of RS experiment conducted using CAFM,[188] and allowed for the first time detecting the changes on the size and resistivity of single CFs. This is the most common method, and it has been also used to remove the gate electrode in field effect transistors to analyze the reliability of the gate oxide after electrical stresses.[189] When using this method, it is very important to have a very large etching selectivity between the metallic electrode and the RS medium, otherwise the second one might be damaged, and the subsequent information collected via CAFM may not be accurate; and ii) the tip of the CAFM has been used to etch (scratch) the entire top metallic electrode,[190] and even the RS medium. While there is no question regarding the etching ability of the CAFM tip,[191] the reliability of the associated current measurement is questionable due to fast tip degradation,[46,192] generation of local heats during the physical etching that may change the properties (e.g., phase) of the underlying RS medium, and difficulty of keeping a constant electrical field during the etching (that would require accurately changing the voltage after each scan). More works discussing the effect of these concerns and the overall validity of this technique are required. An interesting novel method is the use of an ionic liquid electrolyte for the device level experiment,[193] as it allows being easily rinsed and the surface of the RS medium becomes exposed, perfect for carrying out CAFM experiments. More detailed explanations about the use of CAFM for the study of RS can be found in refs. [194,195].

3.6. Switching Mechanism

When attempting to discover the physics underlying RS mechanisms through imaging, the overarching principle guiding experimental design must be realism. Real, deployable RS devices are made with certain materials, assembled into a certain geometry with a particular fabrication process, and are switched using some particular electrical stimulus provided by a background support architecture. At present, no imaging technology exists that is capable of peering into a real, unmodified RS device with sufficient spatial resolution to resolve the physical processes of interest. To explore these physical processes, one must arrange improved imaging access, either by modifying a real device, or by building a custom analog. Inevitably the device that can be studied using the preferred imaging technique differs from a real device, if not at the beginning of the experiment, then by its conclusion. These differences can play an important role in dictating the imaged device's function, and in extreme cases can obscure the physics that is the stated target of the entire investigation.

So, the subject of an imaging experiment is necessarily a compromise between the ideal case of a real device, and the feasible case, which employs a device adapted for imaging. Given the necessity of this compromise, one must consider its consequences most carefully during two separate phases of the experimental investigation. First, during the experimental design phase, effort must be made to, within the experimental constraints, make choices that will minimize the potential of these compromises to create differences between the physics that will be observed in the imaged system, and the physics which occurs in the real, unimaged system. This step involves both guesswork as to what variables are most critical for maintaining a faithful representation, and also a cost-to-benefit analysis as to how much time, effort, and expense can be dedicated to controlling a given variable. A partial list of issues to consider, sorted into broad categories that necessarily have substantial overlap, is given below.

Materials: Materials foreign to a real RS device can be introduced by focused ion beam, electron beam, and ion mill sample preparation, which can deposit or implant such substances as gallium, platinum, electrons, hydrocarbons, or noble gases. Additionally, active interfaces exposed to air can absorb any number of contaminants. Gallium in particular is likely to be a bad actor in a RS study, as it is both conductive and mobile at room temperature and above.

Geometry: Geometric discrepancies from a real RS device can be topological or quantitative. In the former category, a topological difference is generated by introducing a new interface or surface that connects the two electrodes. Such an interface allows for surface migration, a transport mechanism that is physically distinct from, and generally faster than, the bulk migration that must occur in many categories of real RS devices. Worse, these interfaces are often both variable and not well characterized: they might represent a layer damaged relative to the bulk during the sample preparation process, or they have been exposed to ambient atmosphere with varying levels of humidity and other contaminants. In the quantitative category, some experiments will scale a critical dimension such as the electrode area or separation for convenience of fabrication

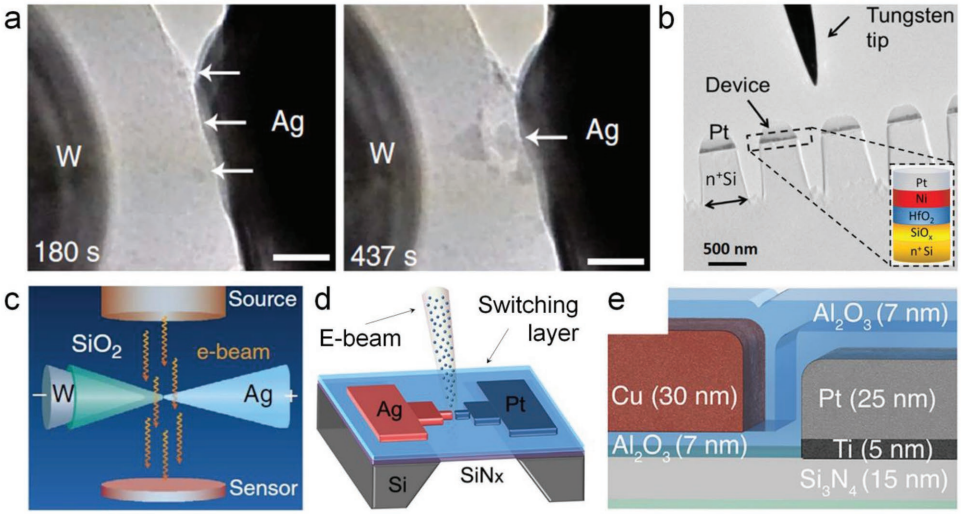

Figure 10. In situ TEM characterization of RS. a) TEM image of a W/SiO_2/Ag structure after being polarized for 180 and 437 s at 8 V, showing the formation of a CF across the dielectric. The scale bars in (a) are 20 nm. b) TEM image showing a tungsten tip approaching to a MIS sample with patterned nanopillars for in situ RS characterization. Schematic of MIM cells made using c) two metallic probes (one of them coated with the RS medium), and ultrathin insulating membranes where the electrodes and dielectrics are d) arranged planar or e) slanted. (a) Reproduced with permission.[19] Copyright 2014, Springer Nature. (b) Reproduced with permission.[11] Copyright 2015, Wiley-VCH. (c) Reproduced with permission.[19] Copyright 2014, Springer Nature. (d) Reproduced with permission.[234] Copyright 2016, IEEE. (e) Reproduced with permission.[235] Copyright 2015, the American Chemical Society.

or imaging. Often the RS device is scaled toward larger sizes, sometimes by orders of magnitude. In the case of an electron-transparent sample for in situ TEM studies, however, the device's thinness can produce an unrealistically small thermal conductance to ambient temperature. Naturally dimensional changes of any sort can drastically alter, for instance, the statistics of device switching, the switching times, and the switching voltages required.

Fabrication: As mentioned above, taking a real RS device and adding additional fabrication steps to prepare it for imaging can compromise the device function. However, while fabricating a custom device purely for the purpose of imaging an RS process (see **Figure 10**) can avoid the need for extra sample preparation steps, this approach can, depending on the fabrication process, still introduce possibly problematic discrepancies from real device function. For instance, by physically moving a mechanical probe, which serves as one electrode and might be coated with the barrier oxide, into contact with a counter electrode, one can form a device that shows RS characteristics and is amenable to imaging (Figure 10c). Another possibility is to fabricate an ultrathin electron-transparent MIM structure and place a mechanical probe on the top electrode (Figure 10b). However, when doing these experiments two important considerations need to be taken into account: i) in the first case (Figure 10c), the contact area, which defines the device size, shows a non-negligible degree of uncertainty; and ii) in both cases (Figure 10b,c) the tip/sample pressure is difficult to control. For this reason, when doing this experiment, it is recommendable first to characterize such parameters doing additional experiments using reference samples.[11,19] Computational studies may also help to shed light into this issue. Another possibility is to fabricate a horizontal geometry, where both electrodes are deposited in a single step, either underneath or on top of the electrolyte (Figure 10d). As discussed above, this shortcut relative to the real, vertically stacked RS device fabrication process (where the BE, electrolyte, and TE are put down sequentially) introduces a connecting interface. Of course, custom devices can also be fabricated in such a way that the materials are nominally identical with those found in a real device, but in practice behave much differently. For instance, a thermally grown oxide electrolyte might or might not perform like one put down with atomic layer deposition.

Electrical: In a deployed device, RS is affected by nanosecond-scale pulses with volt magnitudes, and the devices can switch millions of times without failure. Typical in situ imaging experiments operate in a quasi-DC regime with larger voltages, and manage anywhere from (most commonly) half of one switching cycle to a bare handful of full cycles. Even ex situ imaging experiments, which generally have much more realistic architectures, sometimes deliberately apply destructively large switching voltages to create conducting pathways that can be easily located for imaging. Stray capacitance quickly becomes problematic in systems where the switching voltages are generated remotely from the RS device. Minimizing cable lengths can help prevent device destruction. To date the characterization community has failed to image any RS device operating at a realistic speed for a large number of cycles. Clearly there is room for much improved realism in this area.

Supporting Architecture: Real RS devices are found in arrays, with bit and word lines, and have transistors or some other selector device to mitigate the sneak path problem. Generally, in situ imaging experiments have made no attempt to incorporate this background architecture. Destructive ex situ imaging experiments, on the other hand, have extracted data from entirely realistic cross-point arrays.

Imaging Technique: In the case of an imaging technique such as scalpel AFM, the act of imaging has a profound and obvious effect—total destruction—on the RS device. The information

that can be extracted from such a single snapshot is necessarily limited, a disadvantage counterbalanced by the advantage of the ability to probe an entirely realistic device architecture. However, a recent study reported serious concerns about the reliability of this technique when studying thin dielectrics (which is the case of RS devices).[192] With electron microscopy-based imaging, the effects of imaging can be more subtle. Here the importance of cycling devices under both beam-on and beam-off conditions cannot be overstated. The sensitivity of an RS device to the electron beam may depend strongly on the device chemistry, e.g., conductive bridge RAM or valence change memories. Cycling also allows one to distinguish between ageing or beam-induced imaging artifacts (e.g., beam-deposited contamination), and the bias-induced effects of interest.

Thermal Considerations: The operation of RS devices is often controlled by localized self-heating effects, especially in filamentary devices. Understanding heat and energy dissipation is crucial for the evaluation and design of devices (see also Section 4: simulation of RS), since most proposed switching mechanisms rely on thermally activated processes such as defect generation, ionic transport, etc.[1] Several unique structures have been used to evaluate the local temperature in resistive memory devices,[196–198] and ultrafast transient electrical measurements were proposed to study an effective device temperature.[199] Yet, detailed understanding of the switching and retention mechanisms in RS devices requires more thermal measurements, particularly spatially resolved temperature measurements in realistic device structures should be pursued. Experimental measurement of the local temperature in nanoscale devices is extremely challenging. The ultrafast transient technique[199] allows measuring realistic device structures but requires sub-nanosecond electrical measurement (or shorter than the thermal transient) and only an effective device temperature is obtained, which may be significantly different from the peak temperature.[198] Scanning thermal microscopy (SThM)[200,201] is a good candidate for measuring spatially resolved temperature with nanoscale resolution in future work. The main challenges for SThM measurements are the calibration of its signal to device temperature, and the heat spreading across the top electrode which could limit its spatial resolution. It should be noted that any thermal measurement must also be accompanied by a good electrothermal model.

Remarks on Experimental Descriptions: The second time to carefully consider the compromises made in an experimental investigation is during the presentation of the results. The authors of an experimental study know well and have thought deeply about the limitations of their methods. It is incumbent upon them, as the experts, to explain in plain terms both their efforts to mitigate the confounding compromises inherent to their experimental design, and where these efforts may have fallen short.

4. Simulation of RS: From Material to Devices and Systems

In the field of RS, simulations can be used to interpret experimental data, optimize processes and devices, project accelerated test results under specific operation conditions, predict performances, and screen new materials and device architectures. These computations require the use of models linking material properties to devices and circuits performances. Thus, a hierarchical multiscale modeling structure is needed, which is comprised of three main levels that have to be tightly connected; i) material properties calculation: atomistic approaches including ab initio methods are used to calculate fundamental material properties and defect characteristics; ii) device models: kinetic Monte Carlo (kMC) and finite elements methods (FEM) models are used to project the material properties into the electrical performances of devices, including variability and reliability; iii) semi-empirical/compact models: they are used in circuit simulations to assess the circuit/system performances starting from individual device characteristics. The proposed configuration of a desired multiscale simulation platform for RS devices is displayed in **Figure 11**. In this section, the main advantages and limitations of the different simulation approaches are discussed, including the experimental input needed for their calibration and verification.

4.1. Microscopic Models

Atomistic models are paramount for better understanding of the physical processes in RS devices, such as creation, recombination, and diffusion of defect species, and their role in the switching and charge transport mechanisms (e.g., CF formation and dissolution, evolution of material's structure, heat dissipation, and electrical conduction through these structures).[202,203] Such models should account for the charge transport and the phenomena leading to RS. To properly catch the physics of RS devices regardless of their composition and resistive state, microscopic models should include three main components: i) the relevant defects-related, atoms-related, and materials-related phenomena (generation, recombination, drift, and diffusion of defects/atoms, clustering effects, structural and phase changes in the materials, and related electrical/thermal/optical properties, reactions at interfaces) as well as their interplay.[204] ii) Electron and ion transport models, including carrier tunneling mechanisms, defects sub-band creation, and generalized Landauer approach/ballistic transport. iii) Finally, a (kinetic) Monte Carlo engine should be included to account for the inherent stochasticity of defects-related phenomena and simulate their evolution.

Available experimental information on the physical and chemical properties of materials (e.g., crystallographic and band structure, thermal conductivity, bandgap, work function) can be used for calibration of these models. The properties of the most relevant defects in each material (e.g., activation energies for the creation and recombination of defect species, their mobility within the insulator, defects thermal ionization, and relaxation energies) are typically calculated using ab initio models (such as density functional theory), and/or molecular dynamics models, and can be compared to the results of electrical characterization experiments (e.g., time-dependent dielectric breakdown, variable ramp-rate and temperature switching, random telegraph noise characterization).

This approach can provide a more detailed understanding of the complex physics underlying formation of CFs in

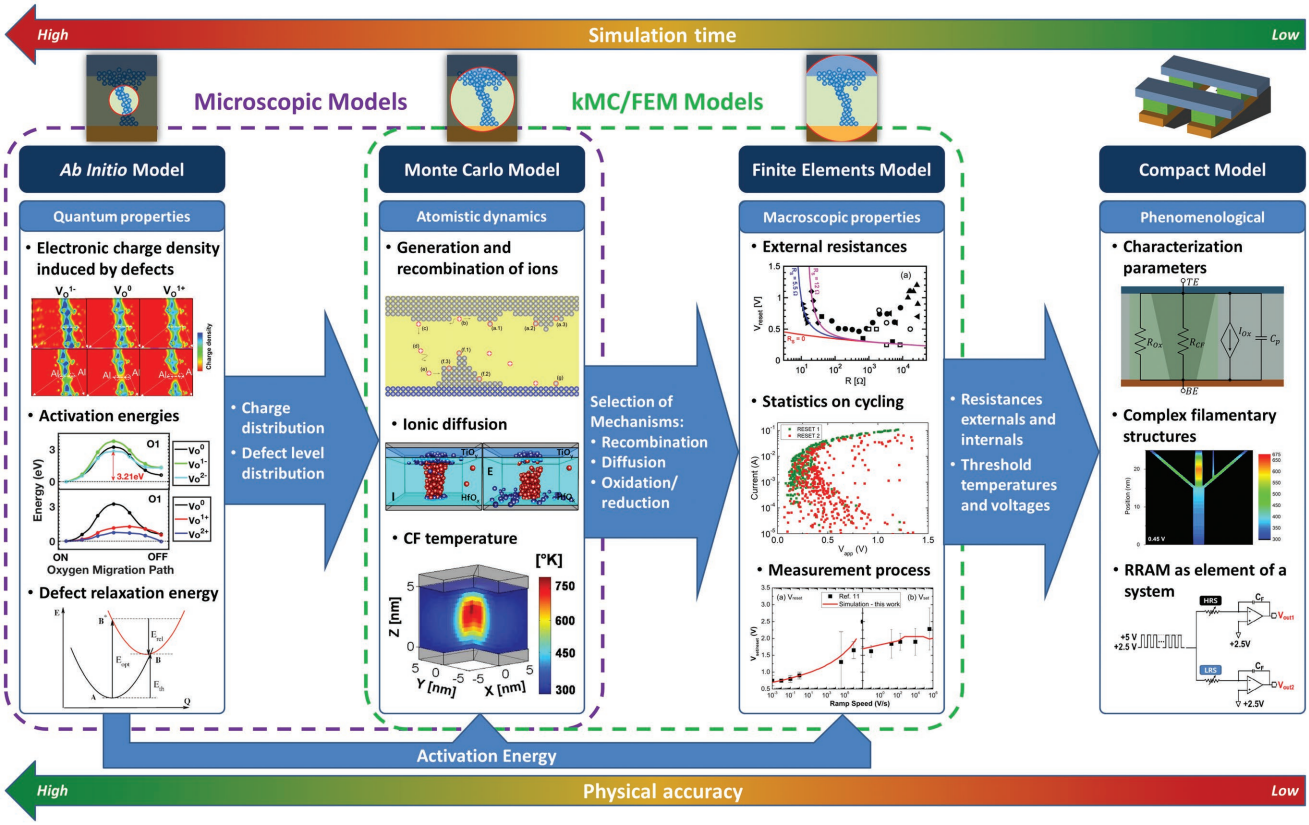

Figure 11. Schematics on the simulation models used for RRAM device characterization, describing the provided information level and detail. In multiscale approaches the information provided by a higher level model is transferred and embedded in the approximations used by the other models. The choice of a model is routinely determined by the agreement between the physical accuracy needed and the available simulation time. The figures shown in the ab initio model section are for Al:HfO_2. Reproduced with permission.[236] Copyright 2017, IEEE. Reproduced with permission.[237] Copyright 2006, AIP Publishing LLC. Figures for Monte Carlo model have been (from top to bottom): Reproduced with permission.[215] Copyright 2015, Royal Society of Chemistry. Reproduced with permission.[238] Copyright 2011, IEEE Electron Devices Society. In the same way, the figures of finite elements section: Reproduced with permission.[239] Copyright 2011, IEEE Electron Devices Society. Reproduced with permission.[211] Copyright 2013, AIP Publishing LLC. Reproduced with permission.[240] Copyright 2011, AIP Publishing LLC. Finally, the figures for Compact Model: Reproduced with permission.[222] Copyright 2016, IOP Publishing. Reproduced with permission.[230] Copyright 2015, IEEE Electron Devices Society. Reproduced with permission. 2015.[51] Copyright 2012, IEEE.

different materials[204–207] and thus help to design devices for specific applications.[208] It can help to identify which material is best-suited for a given target application and provide a useful reference to calibrate appropriate semi-empirical and compact models. To use this approach, one does not require preliminary knowledge of the structure of CF, and it can handle complex material structures exhibiting multilayers (which are extensively investigated and proposed in the literature). On the other hand, creating these comprehensive and complex models requires significant simulation time (several days to several months) and the use of large sets of possible combinations of configurations and structural effects (in some cases not so well defined). Due to these limitations, it is critical to understand which particular processes to include into the model and which could be safely excluded in order to obtain meaningful results while minimizing the simulation time. In many cases, such simulations are impossible without using high-capacity computational systems, which makes these models difficult to employ for simulations of circuits and systems.

4.2. kMC/FEM Models

The simulation of the electrical characteristics of RS devices requires numerical models based on the 3D FEM and kMC approaches. Besides simulating the electrical device behavior, both models allow reproducing the physical phenomena occurring in RS devices during operation and reliability tests.

FEM models simulate electron, ion, and heat transport by differential equations based on quasi-classical models, Poisson's equation for the electric field distribution and current continuity, Fourier's law for heat generation/diffusion, and a drift–diffusion model to describe ionic motion.[209] Density gradient induced diffusions and electric field driven drifts control the ionic migrations occurring by hopping across energy barriers determined by ab initio methods. This thermally activated ion-migration process emphasizes the key role played by the temperature, which accelerates the ionic migration, thus requiring a careful simulation of Joule heating effects.[210–213] This is particularly relevant for filamentary switching, where electrical conduction is strongly confined at a CF. Defects such as oxygen

vacancies and metallic impurities act as dopants for the oxide film, hence their migration can result in a change of CF shape, which in turn affects the device conductivity.[214–216]

kMC models represent another approach to simulate the electrical characteristics and physical processes happening in RS devices. The main difference compared to FEM models is that kMC models account for the individual contributions of defects/ions/vacancies, which allows simulating variability and reliability including statistics. Among the physical processes considered beyond those already accounted for by FEM models, it is worth mentioning the generation and recombination of oxygen vacancies, which play a crucial role in both forming and switching, and trap assisted tunneling, which is the main charge transport mechanism before forming and in reset conditions.[217,218]

Both FEM and kMC models have been shown to accurately agree with a broad range of experimental characteristics, including set and reset transitions under DC and pulsed conditions.[219,220] Typically, FEM allows describing the average device behavior, whereas kMC methods can capture current fluctuations and RS variability. In addition, kMC models can also describe the forming operation, allowing avoiding any assumption on the CF shape/composition considered in switching simulations.[221] Both FEM and kMC models require input material parameters calculated using ab initio calculations, and need to be calibrated on electrical device characteristics.

4.3. Semi-Empirical/Compact Models

The development of circuits and systems based on RS devices requires compact RS device model running in SPICE-like simulation environment.[222–227] These compact models rely on conceptual simplifications (e.g., the idea of a conductive filament with a given shape, e.g., cylindrical or conical) and physical assumptions inferred from empirical measurements.[102,228,229] A variety of semi-empirical models have been proposed, which assume that the CF/s in RS devices behaves as: i) an ohmic conductor, ii) an hourglass-shaped quantum-point contact, iii) a space-charge region, iv) a semi-conductive region that may create a Schottky junction with the electrodes, v) a highly defective region in the dielectric in which either hopping conduction or delocalized transport may occur. The charge transport mechanism can be estimated by fitting the shape and magnitude of the *I*–*V* sweeps obtained in the experiments (in both LRS and HRS) using models formulated using compact expressions, such as Schottky or Poole–Frenkel emission, variable-range or fixed-range hopping, Landauer formula (ballistic transport), Ohm's law, and tunneling (direct, Fowler–Nordheim or trap-assisted). The switching mechanisms, properly modeled using FEM and/or kMC approaches, can be included by simplifying the differential equation modeling ion/vacancy motion, generation, and recombination using empirical expression accounting also for the voltage and temperature dependence of the physical processes.[226,227,231,232]

Compact models are calibrated on FEM/kMC simulations and *I*–*V* sweeps measured under different conditions, which depends also on model parameters (e.g., Schottky barrier height, Poole–Frenkel barrier, hopping range, number of open Landauer channels, CF resistivity thermal resistance and capacitance, among others).

5. Discussion, Perspectives, and Challenges

Although RS is a phenomenon known for over half a century,[10] research in RS devices did not become exhaustive and widespread until 2008. During the last decade RS devices have been improved in terms of size, switching speed, power and energy consumption, endurance, and data retention. Some RS based devices have been commercialized (but still limited to small-capacity embedded memory of microcontrollers). While developing RS based NVMs for massive information storage still remains a challenge, mainly due to spatial and temporal variability problems; solving those challenges will bring enormous benefits to computing systems (e.g., reduce fabrication costs and enhance information storage performance). Furthermore, RS devices are expected to revolutionize the field of neuromorphic computing, as they can be used as electronic synapses in artificial neural networks. For these reasons, it is expected that RS devices will be a topic of intense research during the next decade.

During the past ten years a large number of RS studies have been reported. Unfortunately, we observed that many of them: i) do not provide enough information to reproduce the experiments, ii) use device structures that are not relevant/realistic from a technological point of view, iii) omit essential figures of merit, or iv) make claims that are not well supported by rigorous experimental or computational data. As a guide for RS scientists, **Table 2** summarizes the essential information that an ideal RS study should include.

When fabricating a RS test structure, small device areas are preferred. Using a substrate that serves as common electrode and large (>25 μm^2) top electrodes is not a good practice because the information obtained on a very large device may not be applicable to smaller devices of sizes relevant to real applications, especially in HRS (I_{HRS} and V_{SET}). If that cannot be avoided one needs to prove the presence of RS at the nanoscale using experimental techniques (CAFM or in situ TEM). The use of planar devices (which work under electromigration or grain boundaries modification phenomena)[110–113] is not realistic for technological applications due to their large size, high cell-to-cell variability, and difficulty to control the switching. We note that in several RS papers (unfortunately too many) essential information about the fabrication of the devices is missing, for example: i) the lateral size of the vertical MIM cells, and ii) the composition of the electrodes/dielectric. The first case is typical of some authors based at universities, who use large MIM sizes (due to the lack of photolithography or EBL in their labs) and neglect to discuss the device size as an important weakness. Some works vaguely mention the MIM cell size in the supporting material, while it should be clearly stated in the main text. Actually, the MIM cell size is so important that some authors even indicate it in the title,[52] which is appreciated. And the second is more typical in reports coming from some companies, which intend to advertise their work without disclosing proprietary information. More open disclosure of key process information will only help to advance this field.

Table 2. Checklist including the ideal list of parameters to be provided in a RS study.

Parameter	Recommendation
Device structure	• Cross-bar recommended (Figure 1c), cross-point is also OK (Figure 1b) • Common BE structure only if unavoidable • Planar structures are not competitive, should be used only for in situ TEM characterization
Thin films deposition	• Do not pattern electrodes using silver paint • Do not form oxides by exposure to natural air • Indicate the thickness of both electrodes and RS medium • Clarify if the devices were purchased or self-made
Device area and scalability	• Clearly state the lateral size of the MIM cells in the main text • Area $<10^4$ nm^2 is recommended (see Figure 1d) • Area <25 μm^2 is strongly recommended (see Figure 1b) • If device size >25 μm^2, CAFM (Figure 9a,d) or in situ TEM (Figure 10) are needed to demonstrate scalability of the RS
Electrical characterization setups	• Use integrated resistors or transistors to limit the current (Figure 7a) is better than the current limitation of the SPA (due to overshoot problem) • When using CAFM, logarithmic preamplifier or external SPA connection is recommended to apply/measure high voltages/currents (Figure 9c). For bipolar RS on oxides, the use of N_2 or vacuum chambers is necessary (Figure 9c) • If CAFM is used, indicate the properties of the tip (material, tip radius, spring constant) and atmosphere. Solid metallic probes are recommended if high currents (>10 μA) need to be collected
Endurance	• Indicate if R_{HRS}/R_{LRS} was studied via *I–V* sweeps, current-visible PVS or current-blind PVS. Always indicate the pulse sequence used • Current-visible PVS (Figure 5b) is highly recommended for the first 10^6–10^7 cycles. When measuring endurances $>10^7$ cycles, current-blind PVS may be used to keep a low testing time. • When using current-blind PVS to study extreme endurances, acquiring >50 R_{HRS}/R_{LRS} data points per decade is necessary • Claiming endurances of millions of cycles showing endurance plots with few (<100) very spaced data points (Figure 5c) is NOT OK, especially when working with prototype devices using novel materials. In such devices R_{HRS} and R_{LRS} should be measured in each cycle (Figure 5b)
State retention	• Indicate the current limitation used for the set (Figure 6a) • Indicate if high temperatures were used or not (Figure 6b) • Indicate the read voltage • In electronic synapses, statistical study of the relaxation is necessary (Figure 6c)
Switching time and energy consumption	• Carefully describe the setup used for this measurement (Figure 7a) • Indicate the minimum time detectable with your setup (resolution) • Monitor several cycles of set/reset current (Figure 7b,c)
Variability	• Indicate how many devices were measured • Indicate how many cycles per device were measured (Figure 8a,b) • Indicate what is the dispersion of V_{SET}, V_{RESET}, I_{HRS}, I_{LRS} from cycle-to-cycle and from cell-to-cell (Figure 8) • In multilevel devices cell-to-cell variability information is mandatory
Switching mechanism	• In situ atomic scale chemical studies are recommended (Figure 10) • Indicate the thickness of the lamella used in the TEM • Schematics describing RS without atomic scale chemical measurements is just an speculation, not a demonstration • Indicate the lateral resolution of the technique used
Simulation	• Indicate the models and numerical methods used (Figure 11) • Indicate the assumptions made • Indicate the simulation time

When characterizing a device, it is important to provide enough data supporting the usefulness of the RS mechanism, and these data need to be collected in a rigorous manner. The main problem that we observed in this direction is the lack of figures of merit in several papers. We would like to emphasize again that displaying one/few *I–V* sweeps showing set and reset transitions does not demonstrate the presence of RS in a MIM cell, even if the authors use a new material and aim at showing a proof-of-concept. RS devices are much more sophisticated than that, and competent RS studies must include endurance, retention, speed, power, energy, scalability, and variability information. Moreover, the switching mechanism must be discussed using experimental and/or computational evidences, instead of speculative schematics without any scientific data that support them. Schematics and drawings claiming the movement of atoms inside the MIM cell must be supported by atomic scale chemical analyses or computational studies, otherwise they are simple speculations and should be understood as such. The most important figure of merit missing in most RS papers is the variability, which is especially important in works claiming multilevel RS observations. Finally, in some cases, we observed that the characterization methods used to assess the figures of merit are not the most appropriate. In this direction, the use of current-blind PVS in incipient MIM structures is one of the most remarkable problems. While this method is valid for

well-established devices, in prototype devices made of novel materials it should be avoided; in these cases current-visible PVS are highly recommended.

6. Conclusions

The study of RS phenomena and RS devices can be accomplished in several different ways, and therefore the usefulness and impact of the findings reported will be different. Impactful RS studies should be performed in small (<25 μm^2) cells, preferably with cross-bar structure but also including information about isolated cross-point devices. It is strongly recommended to study the RS locally using CAFM and TEM, and such analyses become mandatory when the area of the devices analyzed is >25 μm^2. The material interfaces need to be flat (RMS < 400 pm), clean, and, to the extent possible, free of oxygen and moisture from the environment.

The main figures of merit to present in a RS study are: i) endurance plot, typically R_{HRS}/R_{LRS} versus cycle. It is important to conduct experiments that measure the R_{HRS}/R_{LRS} in each cycle, and claiming endurances of millions of cycles but showing endurance plots with few and very spaced data points should be avoided when working with prototypes (current-blind PVS combined with DC measurement of the state resistance should be used only in optimized devices at the industrial stage). Current-visible PVS is highly recommended. ii) State retention plot, typically an *I*–*t* curve. It is important to indicate the read voltage and the temperature used during the CVS applied for collecting the *I*–*t* curve, as well as current limitation used during the state transition (*I*–*V* sweep or PVS experiment applied right before to the *I*–*t* curve). iii) Switching time and energy consumption can be calculated in the same experiment. This experiment requires the use of PVS, and if any series device (resistor, transistor) is connected, its location (internal/external) should be described. iv) Variability. Information about how many devices were measured, number of cycles per device, and dispersion of the main RS parameters (V_{SET}, V_{RESET}, I_{HRS}, I_{LRS}) is necessary, and mandatory in multilevel devices. This is of utmost importance, as variability is the main problem of RS technologies. v) Switching mechanism. Although it is very complex, the atomic rearrangements producing the transition between HRS and LRS and vice versa should be analyzed. In situ TEM combined with chemical analyses is recommendable. Drawing schematics without any nanoscale experimental evidence is just a mere speculation, and should be interpreted as such. Furthermore, the use of multilevel computational methods is strongly recommended to complement the experiments and gain additional knowledge about the switching mechanism.

Except in the case of variability information (which should always be provided), failing to provide one of these figures of merit in a RS study might be acceptable, as collecting such large amount of data sets may not be possible for all researchers. What should be avoided by all means is to make exaggerated claims based on insufficient experiments, as that produces false knowledge (e.g., overestimation of endurance and state retention time). But the starting point is always a correct device fabrication, otherwise all the experiments coming later might be irrelevant. Adopting these recommendations in future RS reports would help the scientific community evaluate their real usefulness and impact, serving the overall development of reliable RS technology.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

electrical characterization, electronic synapses, nanofabrication, resistive random-access memories, resistive switching

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[1] D. Ielmini, R. Waser, *Wiley-VCH Book*, ISBN: 978-3-527-33417-9, Wiley-VCH, Weinheim, Germany **2016**.
[2] T. B. Pittman, B. C. Jacobs, J. D. Franson, *Phys. Rev. A* **2001**, *64*, 062311.
[3] International Technology Roadmap for Semiconductors, 2013 Edition, Process Integration, Devices, and Structures section, http://www.itrs.net (accessed: February 2015).
[4] M. F. Chang, P. F. Chiu, W.-C. Wu, C.-H. Chuang, S. S. Sheu, *Proc. IEEE 9th Int. Conf. on ASIC*, Xiamen, China **2011**, pp. 299–302.
[5] Note: We have performed a search in Web of Science using the keywords "resistive switching" or "memristor" or "RRAM" or "ReRAM" or "CBRAM" (all of them as topic), and we found 10498 papers. After that we refined the search using the keyword "multilevel" (as topic) and the number of results was reduced to 408 results (i.e. 3.88%).
[6] K. D. M. Rao, A. A. Sagade, R. John, T. Pradeep, G. U. Kulkarni, *Adv. Electron. Mater.* **2016**, *2*, 1500286.
[7] F. Hui, E. Grustan-Gutierrez, S. Long, Q. Liu, A. K. Ott, A. C. Ferrari, M. Lanza, *Adv. Electron. Mater.* **2017**, *3*, 1600195.
[8] E. Yalon, A. Gavrilov, S. Cohen, D. Mistele, B. Meyler, J. Salzman, D. Ritter, *IEEE Electron Device Lett.* **2012**, *22*, 1, 11.

[9] N. Xiao, M. A. Villena, B. Yuan, S. C. Chen, B. R. Wang, M. Eliáš, Y. Y. Shi, F. Hui, X. Jing, A. Scheuerman, K. C. Tang, P. C. McIntyre, M. Lanza, *Adv. Funct. Mater.* **2017**, *27*, 1700384.
[10] J. G. Simmons, R. R. Verderber, *Proc. R. Soc. London, Ser. A* **1967**, *301*, 77.
[11] X. Wu, S. Mei, M. Bosman, N. Raghavan, X. Zhang, D. Cha, K. Li, K. L. Pey, *Adv. Electron. Mater.* **2015**, *1*, 1500130
[12] C. Y. Lin, C. Y. Wu, C. Y. Wu, C. Hu, T. Y. Tseng, *J. Electrochem Soc.* **2007**, *154*, G189.
[13] C. Yoshida, K. Tsunoda, H. Noshiro, Y. Sugiyama, *Appl. Phys. Lett.* **2007**, *91*, 223510.
[14] A. Chen, S. Haddad, Y. C. Wu, T. N. Fang, S. Kaza, Z. Lan, *Appl. Phys. Lett.* **2008**, *92*, 013503.
[15] T. Sakamoto, H. Sunamura, H. Kawaura, T. Hasegawa, T. Nakayama, M. Aono, *Appl. Phys. Lett.* **2003**, *82*, 3032.
[16] M. J. Rozenberg, I. H. Inoue, M. J. Sanchez, *Phys. Rev. Lett.* **2004**, *92*, 178302.
[17] B. Lei, W. L. Kwan, Y. Shao, Y. Yang, *Org. Electron.* **2009**, *10*, 1048.
[18] S. Baek, D. Lee, J. Kim, S. H. Hong, O. Kim, M. Ree, *Adv. Funct. Mater.* **2007**, *17*, 2637.
[19] Y. Yang, G. Peng, L. Li, X. Pan, X. S. Tappertzhofen, S. H. Choi, R. Waser, L. Valov, W. D. Lu, *Nat. Commun.* **2014**, *5*, 4232.
[20] C. Y. Chen, L. Goux, A. Fantini, S. Clima, R. Degraeve, A. Redolfi, Y. Y. Chen, G. Groeseneken, M. Jurczak, *Appl. Phys. Lett.* **2015**, *106*, 053501.
[21] V. Jousseaume, A. Fantini, J. F. Nodin, C. Guedj, A. Persico, J. Persico, J. Buckley, S. Tirano, P. Lorenzi, R. Vignon, H. Feldis, S. Minoret, H. Grampeix, A. Roule, S. Favier, E. Martinez, P. Calka, N. Rochat, G. Auvert, J. P. Barnes, P. Gonon, C. Vallee, L. Perniola, B. D. Salvo, *Solid-State Electron.* **2011**, *58*, 62.
[22] Y. Shi, C. Pan, V. Chen, N. Raghavan, K. L. Pey, F. M. Puglisi, E. Pop, H. S. P. Wong, M. Lanza, *IEEE Int. Electron Devices Meet.* **2017**, 5.4.1.
[23] Y. Yang, P. Sheridan, W. Lu, *Appl. Phys. Lett.* **2012**, *100*, 203112.
[24] H. Y. Lee, Y. S. Chen, P. S. Chen, P. Y. Gu, Y. Y. Hsu, S. M. Wang, W. H. Liu, C. H. Tsai, S. S. Sheu, P. C. Chiang, W. P. Lin, C. H. Lin, W. S. Chen, F. T. Chen, C. H. Lien, M. J. Tsai, *IEEE Int. Electron Devices Meet.* **2010**, 19.7.1.
[25] S. G. Hahm, S. Choi, S. H. Hong, T. J. Lee, S. Park, D. M. Kim, W. S. Kwon, K. Kim, O. Kim, M. Ree, *Adv. Funct. Mater.* **2008**, *18*, 3276.
[26] A. Chen, *Solid-State Electron.* **2016**, *125*, 25.
[27] A. Sawa, *Mater. Today* **2008**, *11*, 28.
[28] M. Moors, K. K. Adepalli, Q. Y. Lu, A. Wedig, C. Bäumer, K. Skaja, B. Aendt, H. L. Tuller, R. Dittmann, R. Waser, B. Yildiz, I. Valov, *ACS Nano* **2016**, *10*, 1481.
[29] S. Raoux, W. Wełnic, D. Ielmini, *Chem. Rev.* **2010**, *110*, 240.
[30] W. Shim, J. Yao, C. M. Lieber, *Nano Lett.* **2014**, *14*, 5430.
[31] S. H. Jo, K. H. Kim, W. Lu, *Nano Lett.* **2009**, *9*, 870.
[32] M. Holler, S. Tam, H. Castro, R. Benson, *Int. Jt. Conf. Neural Networks, Proc.* **1989**, *2*, 191.
[33] Web-Feet Research, http://www.webfeetresearch.com (accessed: September 2017).
[34] Crossbar Inc. website, https://www.crossbar-inc.com/en/ (accessed: September 2017).
[35] S. Yu, P. Y. Chen, *IEEE Solid-State Circuits Mag.* **2016**, *8*, 43.
[36] M. T. Ghoneim, M. M. Hussain, *Electronics* **2015**, *4*, 424.
[37] Website of Panasonic (Microcontrollers), https://na.industrial.panasonic.com/products/semiconductors/microcontrollers/8-bitlow-power-microcomputers-mn101l-series (accessed: September 2016).
[38] Website of Adesto Technologies, http://www.adestotech.com/products/mavriq/ (accessed: September 2016).
[39] Website of Nantero, http://nantero.com/technology/ (accessed: September 2016).
[40] D. Kuzum, S. Yu, H. S. P. Wong, *Nanotechnology* **2013**, *24*, 382001.
[41] R. Aitken, V. Chandra, J. Myers, B. Sandhu, L. Shifren, G. Yeric, *Symp. VLSI Technol. (VLSI-Technology): Digest of Technical Papers,* **2014**, pp. 1–4, https://doi.org/10.1109/VLSIT.2014.6894339.
[42] B. Wang, N. Xiao, C. Pan, Y. Shi, F. Hui, X. Jing, K. Zhu, B. Guo, M. A. Villena, E. Miranda, M. Lanza, *Cryst. Res. Technol.* **2018**, *53*, 1800006.
[43] Y. F. Ji, C. B. Pan, M. Y. Zhang, S. B. Long, X. J. Lian, F. Miao, F. Hui, Y. Y. Shi, L. Larcher, E. Wu, M. Lanza, *Appl. Phys. Lett.* **2016**, *108*, 012905.
[44] T. Erlbacher, V. Yanev, M. Rommel, A. J. Bauer, L. Frey, *J. Vac. Sci. Technol., B* **2011**, *29*, 01AB08.
[45] B. L. Weeks, M. W. Mark, *Langmuir* **2015**, *21*, 8096.
[46] O. Krause, *Conductive Atomic Force Microscopy: Application in Nanomaterials* (Ed: M. Lanza), ISBN: 978-3-527-69978-0, Wiley-VCH, Weinheim, Germany **2017**, pp. 29–44.
[47] Y. Shi, Y. Ji, F. Hui, V. Iglesias, M. Porti, M. Nafria, E. Miranda, G. Bersuker, M. Lanza, *ECS Trans.* **2014**, *64*, 19.
[48] M. Lanza, G. Bersuker, M. Porti, E. Miranda, M. Nafría, X. Aymerich, *Appl. Phys. Lett.* **2012**, *101*, 193502.
[49] M. Lanza, K. Zhang, M. Porti, M. Nafría, Z. Y. Shen, L. F. Liu, J. F. Kang, D. Gilmer, G. Bersuker, *Appl. Phys. Lett.* **2012**, *100*, 123508.
[50] A. Kawahara, R. Azuma, Y. Ikeda, K. Kawai, Y. Katoh, Y. Hayakawa, K. Tsuji, S. Yoneda, A. Himeno, K. Shimakawa, T. Takagi, T. Mikawa, K. Aono, *IEEE J. Solid-State Circuits* **2013**, *48*, 178.
[51] S. Park, H. Kim, M. Choo, J. Noh, A. Sheri, S. Jung, K. Seo, J. Park, S. Kim, W. Lee, J. Shin, D. Lee, G. Choi, J. Woo, E. Cha, J. Jang, C. Park, M. Jeon, B. Lee, B. H. Lee, H. Hwang, *IEEE Int. Electron Devices Meet.* **2012**, *12*, 231.
[52] B. Govoreanu, G. S. Kar, Y-Y. Chen, V. Paraschiv, S. Kubicek, A. Fantini, I. P. Radu, L. Goux, S. Clima, R. Degraeve, N. Jossart, O. Richard, T. Vandeweyer, K. Seo, P. Hendrickx, G. Pourtois, H. Bender, L. Altimime, D. J. Wouters, J. A. Kittl, M. Jurczak, *IEEE Electron Device Lett.* **2011**, *31*, 6.
[53] E. R. Hsieh, P. Y. Lu, S. S. Chung, K. Y. Chang, C. H. Liu, J. C. Ke, C. W. Yang, C. T. Tsai, *VLSI Technol.* **2014**, *1*, 2.
[54] M. Prezioso, F. Merrikh-Bayat, B. D. Hoskins, G. C. Adam, K. K. Likharev, D. B. Strukov, *Nature* **2015**, *521*, 61.
[55] M. Prezioso, F. Merrikh-Bayat, B. Hoskins, K. Likharev, D. Strukov, *Sci. Rep.* **2016**, *6*, 21331.
[56] J. Handy, presented at *Storage Developer Conference*, Santa Clara, September **2015**.
[57] F. M. Bayat, M. Prezioso, B. Chakrabarti, I. Kataeva, D. Strukov, arXiv preprint 1611.04465 [cs.ET] **2016**.
[58] L. Pietronero, H. J. Wiesmann, *Z. Phys. B: Condens. Matter* **1988**, *70*, 87.
[59] S. Kim, S. Choi, W. Lu, *ACS Nano* **2014**, *8*, 2369.
[60] T. H. Park, H. J. Kim, W. Y. Park, S. G. Kim, B. J. Choi, C. S. Hwang, *Nanoscale* **2017**, *9*, 6010.
[61] Y. Y. Shi, Y. F. Ji, H. Sun, F. Hui, J. C. Hu, Y. X. Wu, J. L. Fang, H. Lin, J. X. Wang, H. L. Duan, M. Lanza, *Sci. Rep.* **2015**, *5*, 11232.
[62] C. X. Hao, F. S. Wen, J. Y. Xiang, S. J. Yuan, B. C. Yang, L. Li, W. H. Wang, Z. M. Zeng, L. M. Wang, Z. Y. Liu, Y. J. Tian, *Adv. Funct. Mater.* **2016**, *26*, 2016.
[63] C. B. Pan, Y. F. Ji, N. Xiao, F. Hui, K. C. Tang, Y. Z. Guo, X. M. Xie, F. M. Puglisi, L. Larcher, E. Miranda, L. L. Jiang, Y. Y. Shi, I. Valov, P. C. McIntyre, R. Waser, M. Lanza, *Adv. Funct. Mater.* **2017**, *27*, 1604811.
[64] P. F. Cheng, K. Sun, Y. H. Hu, *Nano Lett.* **2016**, *16*, 572.
[65] M. Lanza, Y. Wang, T. Gao, A. Bayerl, M. Porti, M. Nafria, Y. B. Zhou, G. Y. Jin, Z. F. Liu, Y. F. Zhang, D. P. Yu, H. L. Duan, *Nano Res.* **2013**, *6*, 485.
[66] M. Lanza, M. Porti, M. Nafría, X. Aymerich, A. Sebastiani, G. Ghidini, A. Vedda, M. Fasoli, *IEEE Trans. Device Mater. Reliab.* **2009**, *9*, 529.

[67] Q. Liu, S. Long, W. Wang, Q. Zuo, S. Zhang, J. Chen, M. Liu, *IEEE Electron Device Lett.* **2009**, *30*, 1335.
[68] A. G. Scheuermann, J. D. Prange, M. Gunji, C. E. D. Chidsey, P. C. McIntyre, *Energy Environ. Sci.* **2013**, *6*, 2487.
[69] P. F. Carcia, R. S. McLean, M. H. Reilly, G. Nunes Jr., *Appl. Phys. Lett.* **2002**, *82*, 1117.
[70] H. Y. Lee, P. S. Chen, T. Y. Wu, Y. S. Chen, C. C. Wang, P. J. Tzeng, C. H. Lin, F. Chen, C. H. Lien, M. J. Tsai, *IEEE Int. Electron Devices Meet.* **2008**, 1.
[71] B. Hudec, C. W. Hsu, I T. Wang, W. L. Lai, C. C. Chang, T. Wang, K. Frohlich, C. H. Ho, C. H. Lin, T. H. Hou, *Sci. China Inform. Sci.* **2016**, *59*, 061403.
[72] S. H. Jo, T. Kumar, S. Narayanan, W. D. Lu, H. Nazarian, *IEEE Int. Electron Devices Meet.* **2014**, 6.7.1.
[73] C. S. Hwang, *Adv. Electron. Mater.* **2015**, *1*, 1400056.
[74] Y. Deng, H. Chen, B. Gao, S. Yu, S. Wu, L. Zhao, B. Chen, Z. Jiang, X. Liu, T. Hou, Y. Nishi, J. Kang, H.-S. P. Wong, *IEEE Int. Electron Devices Meet.* **2013**, 25.7.1.
[75] C. L. He, F. Zhuge, X. F. Zhou, M. Li, G. C. Zhou, Y. W. Liu, J. Z. Wang, B. Chen, W. J. Su, Z. P. Liu, Y. H. Wu, P. Cui, R. W. Li, *Appl. Phys. Lett.* **2009**, *95*, 232101.
[76] A. Hsu, H. Wang, K. K. Kim, J. Kong, T. Palacios, *IEEE Electron Device Lett.* **2011**, *32*, 1008.
[77] Y. Yu, C. Li, Y. Liu, L. Su, Y. Zhang, L. Cao, *Sci. Rep.* **2013**, *3*, 1866.
[78] L. H. Li, E. J. G. Santos, T. Xing, E. Cappelluti, R. Roldan, Y. Chen, K. Watanabe, T. Taniguchi, *Nano Lett.* **2015**, *15*, 218.
[79] L. Britnell, R. V. Gorbachev, R. Jalil, B. D. Belle, F. Schedin, M. I. Katsnelson, L. Eaves, S. V. Morozov, A. S. Mayorov, N. M. R. Peres, A. H. C. Neto, J. Leist, A. K. Geim, L. A. Ponomarenko, K. S. Novoselov, *Nano Lett.* **2012**, *12*, 1707.
[80] X. Li, W. Cai, J. An, S. kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, R. S. Ruoff. *Science* **2009**, *324*, 1312.
[81] K. K. H. Smithe, S. V. Suryavanshi, M. M. Rojo, A. D. Tedjarati, E. Pop, *ACS Nano* **2017**, *11*, 8456.
[82] K. K. H. Smithe, A. Krayev, C. S. Bailey, H. R. Lee, E. Yalon, Ö. B. Aslan, M. Muñoz Rojo, S. Krylyuk, P. Taheri, A. V. Davydov, T. F. Heinz, E. Pop, *ACS Appl. Nano Mater.* **2018**, *1*, 572.
[83] S. Li, S. Wang, D.-M. Tang, W. Zhao, H. Xu, L. Chu, Y. Bando, D. Golberg, G. Eda, *Appl. Mater. Today* **2015**, *1*, 60.
[84] S. M. Eichfeld, L. Hossain, Y.-C. Lin, A. F. Piasecki, B. Kupp, A. G. Birdwell, R. A. Burke, N. Lu, X. Peng, J. Li, A. Azcatl, S. McDonnell, R. M. Wallace, M. J. Kim, T. S. Mayer, J. M. Redwing, J. A. Robinson, *ACS Nano* **2015**, *9*, 2080.
[85] F. Hui, W. Fang, W. S. Leong, T. Kpulun, H. Wang, H. Y. Yang, M. A. Villena, G. L. Harris, J. Kong, M. Lanza, *ACS Appl. Mater. Interfaces* **2017**, *9*, 39895.
[86] L. Jiang, Y. Shi, F. Hui, K. Tang, Q. Wu, C. Pan, X. Jing, H. Uppal, F. Palumbo, G. Lu, T. Wu, H. Wang, M. A. Villena, X. Xie, P. C. McIntyre, M. Lanza, *ACS Appl. Mater. Interfaces* **2017**, *9*, 39758.
[87] G. Y. Lu, T. R. Wu, Q. H. Yuan, H. S. Wang, H. Wang, F. Ding, X. M. Xie, M. H. Jiang, *Nat. Commun.* **2015**, *6*, 6160.
[88] V. Dragoi, E. Pabo, J. Burggraf, G. Mittendorfer, *Microsyst. Technol.* **2012**, *18*, 1065.
[89] C. Yim, K. Lee, N. McEvoy, M. O'Brien, S. Riazimehr, N. C. Berner, C. P. Cullen, J. Kotakoski, J. C. Mayer, M. C. Lemme, G. S. Duesberg, *ACS Nano* **2016**, *10*, 9550.
[90] C. Yim, V. Passi, M. C. Lemme, G. S. Duesberg, C. Ó. Coileáin, E. Pallecchi, D. Fadil, N. McEvoy, *npj 2D Mater. Appl.* **2018**, *2*, 5.
[91] C. Yim, N. McEvoy, S. Riazimehr, D. S. Schneider, F. Gity, S. Monaghan, P. K. Hurley, M. C. Lemme, G. S. Duesberg, *Nano Lett.* **2018**, *18*, 1784.
[92] M. Hempel, A.-Y. Lu, F. Hui, T. Kpulun, M. Lanza, G. Harris, T. Palacios, J. Kong, *Nanoscale* **2018**, *10*, 5522.
[93] M. T. Ghoneim, C. E. Smith, M. M. Hussain, *Appl. Phys. Lett.* **2013**, *102*, 183115.
[94] J. D. Wood, G. P. Doidge, E. A. Carrion, J. C. Koepke, J. A. Kaitz, I. Datye, A. Behnam, J. Hewaparakrama, B. Aruin, Y. Chen, H. Dong, R. T. Haasch, J. W. Lyding, E. Pop, *Nanotechnology* **2015**, *26*, 055302.
[95] M. Lubben, P. Karakolis, V. I. Sougleridis, P. Normand, P. Dimitrakis, I. Valov, *Adv. Mater.* **2015**, *27*, 6202.
[96] X. Zhao, S. Liu, J. Niu, L. Liao, Q. Liu, X. Xiao, H. Lv, S. Long, W. Banerjee, W. Li, S. Si, M. Liu, *Small* **2017**, *13*, 1603948.
[97] K. Lee, I. Hwang, S. Lee, S. Oh, D, Lee, C. K. Kim, Y. Nam, S. Hong, C. Yoon, R. B. Morgan, H. Kim, S. Seo, S. Lee, B. H. Park, *Sci. Rep.* **2015**, *5*, 11279.
[98] J. Lee, C. Du, K. Sun, E. Kioupakis, W. D. Lu. *ACS Nano* **2016**, *10*, 3571.
[99] R. Ge, X. Wu, M. Kim, J. Shi, S. Sonde, L. Tao, Y. Zhang, J. C. Lee, D. Akinwande, *Nano Lett.* **2018**, *18*, 434.
[100] E. Parzinger, M. Hetzl, U. Wurstbauer, A. Holleitner, *npj 2D Mater. Appl.* **2017**, *1*, 40.
[101] C. L. Tan, Z. D. Liu, W. Huang, H. Zhang, *Chem. Soc. Rev.* **2015**, *44*, 2615.
[102] C. Pan, E. Miranda, M. A. Villena, N. Xiao, X. Jing, X. Xie, T. Wu, F. Hui, Y. Shi, M. Lanza, *2D Mater.* **2017**, *4*, 2.
[103] M. Lanza, Y. Wang, A. Bayerl, T. Gao, M. Porti, M. Nafria, H. Liang, G. Jing, Z. Liu, Y. Zhang, Y. Tong, H. Duan, *J. Appl. Phys.* **2013**, *113*, 104301.
[104] G. Lupina, J. Kitzmann, I. Costina, M. Lukosius, C. Wenger, A. Wolff, S. Vaziri, M. Ostling, I. Pasternak, A. Krajewska, W. Strupinski, S. Kataria, A. Gahoi, M. C. Lemme, G. Ruhl, G. Zoth, O. Luxenhofer, W. Mehr, *ACS Nano* **2015**, *9*, 4776.
[105] M. Belete, S. Kataria, U. Koch, M. Kruth, C. Engelhard, J. Mayer, O. Engstrom, M. C. Lemme, arxiv preprint 1807.07592, **2018**.
[106] B. Vermeire, L. Lee, H. G. Parks, *IEEE Trans. Semicond. Manuf.* **1998**, *11*, 232.
[107] S. Caneva, R. S. Weatherup, B. C. Bayer, B. Brennan, S. J. Spencer, K. Mingard, A. Cabrero-Vilatela, C. Baehtz, A. J. Pollard, S. Hofmann, *Nano Lett.* **2015**, *15*, 1867.
[108] K. Qian, R. Y. Tay, M.F. Lin, J. Chen, H. Li, J. Lin, J. Wang, G. Cai, V. C. Nguyen, E. H. T. Teo, T. Chen, P. S. Lee, *ACS Nano* **2017**, *11*, 1712.
[109] K. Qian, R. Y. Tay, V. C. Nguyen, J. Wang, G. Cai, T. Chen, E. H. T. Teo, P. S. Lee, *Adv. Funct. Mater.* **2016**, *26*, 2176.
[110] B. Standley, W. Z. Bao, H. Zhang, J. Bruck, C. N. Lau, M. Bockrath, *Nano Lett.* **2008**, *8*, 3345.
[111] T. J. Echtermeyer, M. C. Lemme, M. Baus, B. N. Szafranek, A. K. Geim, H. Kurz, *IEEE Electron Device Lett.* **2008**, *29*, 952.
[112] K. Sangwan, D. Jariwala, I. S. Kim, K. S. Chen, T. J. Marks, L. J. Lauhon, M. C. Hersam, *Nat. Nanotechnol.* **2015**, *10*, 403.
[113] V. K. Sangwan, H. S. Lee, H. Bergeron, I. Balla, M. E. Beck, K. S. Chen, Mark C. Hersam, *Nature* **2018**, *554*, 500.
[114] H. Y. Lee, P. S. Chen, T. Y. Wu, Y. S. Chen, C. C. Wang, P. J. Tzeng, C. H. Lin, F. Chen, C. H. Lien, M. J. Tsai, presented at *Proc. IEEE Int. Electron Devices Meet.*, San Francisco, CA, USA, December **2008**.
[115] H. Lv, X. Xu, H. Liu, R. Liu, Q. Liu, W. Banerjee, H. Sun, S. Long, L. Li, M. Liu, *Sci. Rep.* **2015**, *5*, 7764.
[116] J. J. Yang, M.-X. Zhang, J. P. Strachan, F. Miao, M. D. Pickett, R. D. Kelley, G. Medeiros-Ribeiro, R. S. Williams, *Appl. Phys. Lett.* **2010**, *97*, 232102.
[117] M. Wang, S. Cai, C. Pan, C. Wang, X. Lian, Y. Zhuo, K. Xu, T. Cao, X. Pan, B. Wang, S.-J. Liang, J. J. Yang, P. Wang, F. Miao, *Nat. Electron.* **2018**, *1*, 130.
[118] X. Yan, J. Zhao, S. Liu, Z. Zhou, Q. Liu, J. Chen, X. Y. Liu, *Adv. Funct. Mater.* **2018**, *28*, 1705320.

[119] D. B. Strukov, G. S. Snider, D. R. Stewart, R. S. Williams, *Nature* **2008**, *453*, 80.
[120] M. J. Lee, C. B. Lee, D. S. Lee, S. R. Lee, M. Chang, J. H. Hur, Y. B. Kim, C. J. Kim, D. H. Seo, S. Seo, U. I. Chung, I. K. Yoo, K. Kim, *Nat. Mater.* **2011**, *10*, 625.
[121] I G. Baek, M. S. Lee, S. Seo, M. J. Lee, D. H. Seo, D. S. Suh, J. C. Park, S. O. Park, H. S. Kim, I. K. Yoo, U. I. Chung, J. T. Moon, presented at *IEEE Int. Electron Device Meet.*, San Francisco, CA, USA, December **2004**.
[122] H. J. Uppal, I. Z. Mitrovic, S. Hall, B. Hamilton, V. Markevich, A. R. Peaker, *J. Vac. Sci. Technol., B* **2009**, *27*, 443.
[123] M. Lanza, M. Porti, M. Nafria, X. Aymerich, *IEEE Trans. Device Mater. Reliab.* **2009**, *9*, 529.
[124] Y. Y. Chen, M. Komura, R. Degraeve, B. Govoreanu, L. Goux, A. Fantini, N. Raghavan, S. Clima, L. Zhang, A. Belmonte, A. Redolfi, G. S. Kar, G. Groeseneken, D. J. Wouters, M. Jurczak, *IEEE Int. Electron Devices Meet.* **2013**, 10.1.1.
[125] Y. Y. Chen, L. Goux, S. Clima, B. Govoreanu, R. Degraeve, G. S. Kar, A. Fantini, G. Groeseneken, D. J. Wouters, M. Jurczak, *IEEE Trans. Electron Devices* **2013**, *60*, 1114.
[126] C. Cagli, D. Ielmini, F. Nardi, A. L. Lacaita, *IEEE Int. Electron Devices Meet.* **2008**, 1.
[127] C. H. Cheng, A. Chin, F. S. Yeh, *Symp. VLSI Technol.* **2010**, 85, https://doi.org/10.1109/VLSIT.2010.5556180.
[128] G. H. Buh, I. Hwang, B. H. Park, *Appl. Phys. Lett.* **2009**, *95*, 142101.
[129] Z. Wei, Y. Kanzawa, K. Arita, Y. Katoh, K. Kawai, S. Muraoka, S. Mitani, S. Fujii, K. Katayama, M. Iijima, T. Mikawa, T. Ninomiya, R. Miyanaga, Y. Kawashima, K. Tsuji, A. Himeno, T. Okada, R. Azuma, K. Shimakawa, H. Sugaya, T. Takagi, R. Yasuhara, K. Horiba, H. Kumigashira, M. Oshima, presented at *IEEE IEDM* San Francisco, USA, December **2008**.
[130] A. J. Bhattacharyya, J. Maier, *Adv. Mater.* **2004**, *16*, 9.
[131] Z. Wang, Z. Jiang, X. Zheng, S. Fong, H.-Y. Chen, H.-S. P. Wong, Y. Nishi, *IEEE Electron Device Lett.* **2017**, *38*, 863.
[132] B. Gao, H. Zhang, B. Chen, L. Liu, X. Liu, R. Han, J. Kang, Z. Fang, H. Yu, B. Yu, D.-L. Kwong, *IEEE Electron Device Lett.* **2011**, *32*, 276.
[133] L. G. Wang, X. Qian, Y. Q. Cao, Z. Y. Cao, G. Y. Fang, A. D. Li, D. Wu, *Nano Res. Lett.* **2015**, *10*, 135.
[134] Z. R. Wang, S. Joshi, Sergey E. Savel'ev, H. Jiang, R. Midya, P. Lin, M. Hu, N. Ge, J. P. Strachan, Z. Y. Li, Q. Wu, M. Barnell, G. L. Li, H. L. Xin, R. S. Williams, Q. F. Xia, J. Joshua Yang, *Nat. Mater.* **2017**, *16*, 101.
[135] Y. Shi, M. Lanza, X. Liang, B. Yuan, V. Chen, H. Li, F. Hui, Z. Yu, F. Yuan, E. Pop, H.-S. P. Wong, *Nat. Elect.* **2018**, *1*, 458.
[136] L. Goux, J. G. Lisoni, X. P. Wang, M. Jurczak, D. J. Wouters, *IEEE Trans. Electron Devices* **2009**, *56*, 2363.
[137] K. Kinoshita, K. Tsunoda, Y. Sato, H. Noshiro, S. Yagaki, M. Aoki, Y. Sugiyama, *Appl. Phys. Lett.* **2008**, *93*, 033506.
[138] L. Goux, A. Fantini, A. Redolfi, C. Y. Chen, F. F. Shi, R. Degraeve, Y. Y. Chen, T. Witters, G. Groeseneken, M. Jurczak, *VLSI Technol.* **2014**, 1, https://doi.org/10.1109/VLSIT.2014.6894401.
[139] A. Fantini, D. J. Wouters, R. Degraeve, L. Goux, L. Pantisano, G. Kar, Y.-Y. Chen, B. Govoreanu, J. A. Kittl, L. Altimime, M. Jurczak, *IEEE International Memory Workshop* **2012**, 1, https://doi.org/10.1109/IMW.2012.6213646.
[140] D. J. Wouters, L. Zhang, A. Fantini, R. Degraeve, L. Goux, Y. Y. Chen, B. Govoreanu, G. S. Kar, G. V. Groeseneken, M. Jurczak, *IEEE Electron Device Lett.* **2012**, *33*, 1186.
[141] L. Goux, K. Sankaran, G. Kar1, N. Jossart, K. Opsomer, R. Degraeve, G. Pourtois, G.-M. Rignanese, C. Detavernier, S. Clima1, Y.-Y. Chen, A. Fantini, B. Govoreanu, D. J. Wouters, M. Jurczak, L. Altimime, J. A. Kittl, *VLSI Technol.* **2012**, 69, https://doi.org/10.1109/VLSIT.2012.6242465.
[142] H. Lim, H.-W. Ahn, V. Kornijcuk, G. Kim, J. Y. Seok, I. Kim, C. S. Hwang, D. S. Jeong, *Nanoscale* **2016**, *8*, 9629.
[143] A. Fantini, L. Goux, A. Redolfi, R. Degraeve, G. Kar, Y. Y Chen, M. Jurczak, *VLSI Technol.* **2014**, 1, https://doi.org/10.1109/VLSIT.2014.6894433.
[144] Y. Y. Chen, R. Roelofs, A. Redolfi, R. Degraeve, D. Crotti, A. Fantini, S. Clima, B. Govoreanu, M. Komura, L. Goux, L. Zhang, A. Belmonte, Q. Xie, J. Maes, G. Pourtois, M. Jurczak, *VLSI Technol.* **2014**, 1, https://doi.org/10.1109/VLSIT.2014.6894403.
[145] A. Belmonte, W. Kim, B. T. Chan, N. Heylen, A. Fantini, M. Houssa, M. Jurczak, L. Goux, *IEEE Trans. Electron Devices* **2013**, *60*, 3690.
[146] G. H. Kim, H. Ju, M. K. Yang, D. K. Lee, J. W. Choi, J. H. Jang, S. G. Lee, I. S. Cha, B. K. Park, J. H. Han, T.-M. Chung, K. M. Kim, C. S. Hwang, Y. K. Lee, *Small* **2017**, *13*, 1701781.
[147] K. M. Kim, J. J. Yang, E. Merced, C. Graves, S. Lam, N. Davila, M. Hu, N. Ge, Z. Li, R. S. Williams, C. S. Hwang, *Adv. Electron. Mater.* **2015**, *1*, 1500095.
[148] J. H. Yoon, K. M. Kim, S. J. Song, J. Y. Seok, K. J. Yoon, D. E. Kwon, T. H. Park, Y. J. Kwon, X. Shao, C. S. Hwang, *Adv. Mater.* **2015**, *27*, 3811.
[149] T. H. Park, S. J. Song, H. J. Kim, S. G. Kim, S. Chung, B. Y. Kim, K. J. Lee, K. M. Kim, B. J. Choi, C. S. Hwang, *Sci. Rep.* **2015**, *5*, 15965.
[150] A. Fantini, G. Gorine, R. Degraeve, L. Goux, C. Y. Chen, A. Redolfi, S. Clima, A. Cabrini, G. Torelli, M. Jurczak, *IEEE Int. Electron Devices Meet.* **2015**, 7.
[151] F. Xiong, S. Deshmukh, S. Hong, Y. Dai, A. Behnam, F. Lian, E. Pop, *Nano Res.* **2016**, *9*, 2950.
[152] C.-L. Tsai, F. Xiong, E. Pop, M. Shim, *ACS Nano* **2013**, *7*, 5360.
[153] A. Mehonic, S. Cueff, M. Wojdak, S. Hudziak, C. Labbé, R. Rizk, A.J. Kenyon, *Nanotechnology* **2012**, *23*, 455201.
[154] M. Lanza, *Conductive Atomic Force Microscopy: Applications in Nanomaterials*, WILEY-VCH, Weinheim, Germany **2017**, Chap. 1, pp. 23–50.
[155] A. L. Vazquez de Parga, F. Calleja, B. Borca, M. C. G. Passeggi, J. J. Hinarejos, F. Guinea, R. Miranda, *Phys. Rev. Lett.* **2008**, *100*, 056807.
[156] Q. C. Li, X. L. Zou, M. X. Liu, J. Y. Sun, Y. B. Gao, Y. Qi, X. B. Zhou, B. I. Yakobson, Y. F. Zhang, Z. F. Liu, *Nano Lett.* **2015**, *15*, 5804.
[157] A. Mehonic, S. Cueff, M. Wojdak, S. Hudziak, C. Labbé, R. Rizk, A. J. Kenyon, *Nanotechnology* **2012**, *23*, 455201.
[158] A. Plecenik, M. Tomasek, T. Plecenik, M. Truchly, J. Noskovic, M. Zahoran, T. Roch, M. Belogolovskii, M. Spankova, S. Chromik, P. Kus, *Appl. Surf. Sci.* **2010**, *256*, 5684.
[159] V. Dubost, T. Cren, C. Vaju, L. Cario, B. Corraze, E. Janod, F. Debontridder, D. Roditchev, *Nano Lett.* **2013**, *13*, 3648.
[160] A. Gambardella, M. Prezioso, M. Cavallini, *Sci. Rep.* **2014**, *4*, 4196.
[161] M. K. Hota, M. K. Bera, C. K. Maiti, *Nanosci. Nanotechnol. Lett.* **2012**, *4*, 394.
[162] S. Chakrabarti, A. J. Pal, *Nanoscale* **2015**, *7*, 9886.
[163] M. Meyyappan, *J. Phys. D: Appl. Phys.* **2009**, *42*, 213001.
[164] O. A. Ageev, Y. F. Blinov, O. I. Il'in, A. S. Kolomiitsev, B. G. Konoplev, M. V. Rubashkina, V. A. Smirnov, A. A. Fedotov, *Tech. Phys.* **2013**, *58*, 1831.
[165] O. A. Ageev, Y. F. Blinov, O. I. Il'in, B. G. Konoplev, M. V. Rubashkina, V. A. Smirnov, A. A. Fedotov, *Phys. Solid-State* **2015**, *57*, 825.
[166] W. Frammelsberger, G. Benstetter, J. Kiely, R. Stamp, *Appl. Surf. Sci.* **2007**, *253*, 3615.
[167] L. Aguilera, M. Lanza, M. Porti, J. Grifoll, M. Nafría, X. Aymerich, *Rev. Sci. Instrum.* **2008**, *79*, 073701.
[168] L. Aguilera, M. Lanza, A. Bayerl, M. Porti, M. Nafría, X. Aymerich, *J. Vac. Sci. Technol., B* **2009**, *27*, 360.
[169] CSI, ResiScope Mode, http://www.csinstruments.eu/resiscope-mode-resistance-over-10-decades/ (accessed: November 2017).
[170] Hitachi, CAFM, SSRM mode, http://www.hitachi-hightech.com/global/products/science/tech//em/spm/descriptions/electro/ssrm.html (accessed: March 2018).
[171] M. Porti, M. Nafria, X. Aymerich, *IEEE Trans. Electron Devices* **2003**, *50*, 933.

[172] R. Garcia, R. V. Madrid, J. Martinez, *Chem. Soc. Rev.* **2006**, *35*, 29.
[173] X. Blasco, D. Hill, M. Nafria, X. Aymerich, *Nanotechnology* **2001**, *12*, 110.
[174] M. Abe, Y. Sugimoto, T. Namikawa, K. Morita, N. Oyabu, S. Morita, *Appl. Phys. Lett.* **2007**, *90*, 203103.
[175] M. Lanza, M. Reguant, G. J. Zou, P. Y. Lv, H. Li, R. Chin, H. Y. Liang, D. P. Yu, H. L. Duan, *Adv. Mater. Interfaces* **2014**, *1*, 1300101.
[176] W. H. Wang, R. X. Dong, X. L. Yan, B. Yang, X. L. An, *IEEE Trans. Nanotechnol.* **2012**, *11*, 1135.
[177] X. Sun, U. Ross, J. W. Gerlach, A. Lotnyk, B. Rauschenbach, *Adv. Electron. Mater.* **2017**, 1700283.
[178] V. Iglesias, M. Lanza, K. Zhang, A. Bayerl, M. Porti, M. Nafría, X. Aymerich, G. Benstetter, Z. Y. Shen, G. Bersuker, *Appl. Phys. Lett.* **2011**, *99*, 103510.
[179] M. Lanza, M. Porti, M. Nafría, X. Aymerich, E. Wittaker, B. Hamilton, *Rev. Sci. Instrum.* **2010**, *81*, 106110.
[180] M. Lanza, M. Porti, M. Nafría, X. Aymerich, E. Whittaker, B. Hamilton, *Microelectron. Reliab.* **2010**, *50*, 1312.
[181] A. Ranjan, N. Raghavan, J. Molina, S.J. O'Shea, K. Shubhakar, K. L. Pey, *Microelectron. Reliab.* **2016**, *64*, 172.
[182] O. Pirrotta, L. Larcher, M. Lanza, A. Padovani, M. Porti, M. Nafria, G. Bersuker, *J. Appl. Phys.* **2013**, *114*, 134503.
[183] C. Yoshida, K. Kentaro, Y. Takahiro, S. Yoshihiro, *Appl. Phys. Lett.* **2008**, *93*, 042106.
[184] R. Muenstermann, T. Menke, R. Dittmann, S. Mi, C. L. Jia, D. Park, J. Mayer, *J. Appl. Phys.* **2010**, *108*, 482.
[185] V. Iglesias, M. Lanza, A. Bayerl, M. Porti, M. Nafria, X. Aymerich, L. F. Liu, J.F. Kang, G. Bersuker, K. Zhang, Z. Y. Shen, *Microelectron. Reliab.* **2012**, *52*, 2110.
[186] F. Giannazzo, S. Sonde, V. Rainer, E. Rimini, *Appl. Phys. Lett.* **2010**, *95*, 263109.
[187] B. Singh, B. R. Mehta1, D. Varandani, A. V. Savu, J. Brugger, *Nanotechnology* **2012**, *23*, 495707.
[188] B. J. Choi, D. S. Jeong, S. K. Kim, C. Rohde, S. Choi, J. H. Oh, H. J. Kim, C. S. Hwang, K. Szot, R. Waser, B. Reichenberg, S. Tiedke, *J. Appl. Phys.* **2005**, *98*, 033715.
[189] Q. Wu, M. Porti, A. BayerJ, M. Lanza, J. M. Martinez, R. Rodriguez, M. Nafria, X. Aymerich, E. Simoen, *IEEE Trans. Electron Devices.* **2015**, *61*, 3118.
[190] U. Celano, *Metrology and Physical Mechanisms in New Generation Ionic Devices*, Springer International Publishing, Basel, Switzerland **2016**.
[191] R. Garcia, A. W. Knoll, E. Riedo, *Nat. Nanotechnol.* **2014**, *9*, 577.
[192] S. Chen, L. Jiang, M. Buckwell, X. Jing, Y. Ji, E. Grustan-Gutierrez, F. Hui, Y. Shi, G. Benstetter, A. J. Kenyon, M. Lanza, unpublished.
[193] K. C. Tang, A. C. Meng, F. Hui, Y. Y. Shi, T. Petach, C. Hitzman, A. L. Koh, D. G. Gordon, M. Lanza, P. C. McIntyre, *Nano Lett.* **2017**, *17*, 4390.
[194] M. Lanza, *Materials* **2014**, *7*, 2155.
[195] M. Lanza, U. Celano, F. Miao, *J. Electroceram.* **2017**, *3*, 1.
[196] E. Yalon, S. Cohen, A. Gavrilov, D. Ritter, *Nanotechnology* **2012**, *23*, 465201.
[197] M. Witzleben, K. Fleck, C. Funck, B. Baumkötter, M. Zuric, A. Idt, T. Breuer, R. Waser, U. Böttger, S. Menzel, *Adv. Electron. Mater.* **2017**, *3*, 1700294.
[198] E. Yalon, A. A. Sharma, M. Skowronski, J. A. Bain, D. Ritter, I. V. Karpov, *IEEE Trans. Electron Devices.* **2015**, *69*, 2792.
[199] A. A. Sharma, M. Noman, M. Skowronski, J. A. Bain, presented at IEEE International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), Hsinchu, Taiwan, **2014**.
[200] A. Majumdar, *Annu. Rev. Mater. Sci.* **1999**, *29*, 505.
[201] E. Yalon, S. Deshmukh, M. M. Rojo, F. Lian, C. M. Neumann, F. Xiong, E. Pop, *Sci. Rep.* **2017**, *7*, 15360.
[202] B. Magyari-Köpe, Y. Nishi, *Intelligent Integrated Systems: Devices, Technologies, and Architectures*, (Ed: S. Deleonibus), ISBN 9789814411424, Stanford, USA **2014**, 325.
[203] K. Kamiya, M. Yang, S. G. Park, B. Magyari-Köpe, Y. Nishi, M. Niwa, K. Shiraishi, *Appl. Phys. Lett.* **2012**, *100*, 073502.
[204] D. Duncan, B. Magyari-Köpe, Y. Nishi, *IEEE Electron Device Lett.* **2016**, *37*, 400.
[205] L. Zhao, B. Magyari-Köpe, Y. Nishi, *Phys. Rev. B* **2017**, *95*, 054104.
[206] D. Duncan, B. Magyari-Köpe, Y. Nishi, *Phys. Rev. Appl.* **2017**, *7*, 034020.
[207] L. Zhao, S. Clima, B. Magyari-Köpe, M. Jurczak, Y. Nishi, *Appl. Phys. Lett.* **2015**, *107*, 013504.
[208] K. Jung, B. Magyari-Köpe, Y. Nishi, *IEEE Electron Device Lett.* **2017**, *38*, 728.
[209] M. A. Villena, J. B. Roldán, F. Jiménez-Molinos, E. Miranda, J. Suñé, M. Lanza, *J. Comput. Electron.* **2017**, *16*, 1095.
[210] U. Russo, D. Ielmini, C. Cagli, A. L. Lacaita, *IEEE Trans. Electron Devices* **2009**, *56*, 193.
[211] M. A. Villena, F. Jimenez- Molinos, J. B. Roldan, J. Sune, S. Long, X. Lian, F. Gamiz, M. Liu, *J. Appl. Phys.* **2013**, *114*, 144505.
[212] M. A. Villena, M. B. González, J. B. Roldan, F. Campabadal, F. Jimenez-Molinos, F. M. Gómez-Campos, J. Suñé, *Solid-State Electron.* **2015**, *111*, 47.
[213] S. Long, L. Perniola, C. Cagli, J. Buckley, X. Lian, E. Miranda, F. Pan, M. Liu, J. Suñé, *Sci. Rep.* **2013**, *3*, 2929.
[214] M. A. Villena, J. B. Roldán, P. García-Fernández, F. Jiménez-Molinos, *J. Vac. Sci. Technol., B* **2017**, *35*, 01A105.
[215] S. Menzel, P. Kaupmann, R. Waser, *Nanoscale* **2015**, *7*, 12673.
[216] S. Aldana, P. García-Fernández, A. Rodríguez-Fernández, R. Romero-Zaliz, M. B. González, F. Jiménez-Molinos, F. Campabadal, F. Gómez-Campos, J. B. Roldán, *J. Phys. D: Appl. Phys.* **2017**, *50*, 335103.
[217] L. Larcher, A. Padovani, *J. Comput. Electron.* **2017**, *16*, 1077.
[218] A. Padovani, L. Larcher, J. Woo, H. Hwang, in *17th Non-Volatile Memory Technology Symposium (NVMTS)*, Aachen, Germany **2017**, p. 1, https://doi.org/10.1109/NVMTS.2017.8171306.
[219] M. A. Villena, M. B. González, F. Jimenez-Molinos, F. Campabadal, J. B. Roldan, J. Suñe, E. Romera, E. Miranda, *J. Appl. Phys.* **2014**, *115*, 214504.
[220] F. M. Puglisi, L. Larcher, C. Pan, N. Xiao, Y. Shi, F. Hui, M. Lanza, *Int. Electron Devices Meet.* **2016**, 34.8.1.
[221] P. Huang, Y. Deng, B. Gao, B. Chen, F. Zhang, D. Yu, L. Liu, G. Du, J. Kang, X. Liu, *Jpn. J. Appl. Phys.* **2013**, *52*, 04CD04.
[222] G. González-Cordero, J. B. Roldan, F. Jiménez-Molinos, J. Suñé, S. Long, M. Liu, *Semicond. Sci. Technol.* **2016**, *31*, 115013.
[223] X. Guan, S. Yu, H-S. P. Wong, *IEEE Electron Device Lett.* **2012**, *33*, 1405.
[224] F. M. Puglisi, N. Zagni, L. Larcher, P. Pavan, *47th European Solid-State Device Research Conference (ESSDERC)*, Leuven, Belgium **2017**, p. 204, https://doi.org/10.1109/ESSDERC.2017.8066627.
[225] P. Y. Chen, S. Yu, *IEEE Trans. Electron Devices* **2015**, *62*, 4022.
[226] P. Huang, X. Y. Liu, B. Chen, H. T. Li, Y. J. Wang, Y. X. Deng, K. L. Wei, L. Zeng, B. Gao, G. Du, X. Zhang, J. F. Kang, *IEEE Trans. Electron Devices* **2013**, *60*, 4090.
[227] J. F. Kang, B. Gao, P. Huang, Z. Chen, Y. D. Zhao, C. Liu, H. T. Li, X. Y. Liu, *IEEE Int. Electron Devices Meet.* **2015**, 5.4.1.
[228] G. A. Patterson, J. Suñé, E. Miranda, *Int. J. Circuit Theory Appl.* **2018**, *46*, 39.
[229] I. Vourkas, A. Batsos, G. C. Sirakoulis, *Int. J. Circuit Theory Appl.* **2015**, *43*, 553.
[230] F. Jimenez-Molinos, M. A. Villena, J. B. Roldan, A. M. Roldan, *IEEE Trans. Electron Devices* **2015**, *62*, 955.
[231] M. Bocquet, D. Deleruyelle, H. Aziza, C. Muller, J. M. Portal, *IEEE Faible Tension Faible Consommation*, Paris, France **2013**, p. 1, https://doi.org/10.1109/FTFC.2013.6577779.
[232] M. Bocquet, D. Deleruyelle, H. Aziza, C. Muller, J. M. Portal, T. Cabout, E. Jalaguier, *IEEE Trans. Electron Devices* **2014**, *61*, 674.

[233] K. Szot, W. Speier, G. Bihlmayer, R. Waser, *Nat. Mater.* **2006**, *5*, 312.
[234] Y. C. Yang, W. D. Lu, *IEEE Trans. Nanotechnol.* **2016**, *15*, 465.
[235] W. A. Hubbard, A. Kerelsky, G. Jasmin, E. R. White, J. Lodico, M. Mecklenburg, B. C. Regan, *Nano Lett.* **2015**, *15*, 3983.
[236] Y. Song, B. Magyari-Kope, Y. Lin, Y. Nishi, *IEEE International Memory Workshop* **2017**, 1, https://doi.org/10.1109/IMW.2017.7939089.
[237] J. L. Gavartin, D. M. Ramo, A. L. Shluger, *Appl. Phys. Lett.* **2006**, *89*, 082908.
[238] A. Padovani, L. Larcher, O. Pirrotta, L. Vandelli, G. Bersuker, *IEEE Trans. Electron Devices* **2015**, *62*, 1998.
[239] D. Ielmini, F. Nardi, C. Cagli, *IEEE Trans. Electron Devices* **2011**, *58*, 3246.
[240] M. Bocquet, D. Deleruyelle, C. Muller, J.-M. Portal, *Appl. Phys. Lett.* **2011**, *98*, 263507.
[241] H.-S. P. Wong, H. Y. Lee, S. Yu, Y. S. Chen, Y. Wu, P. S. Chen, B. Lee, F. T. Chen, M. J. Tsai, *Proc. IEEE* **2012**, *100*, 1951.
[242] M. C. Wu, Y. W. Lin, W. Y. Jang, C. H. Lin, T. Y. Tseng, *IEEE Electron Device Lett.* **2011**, *32*, 1026.
[243] C. Ahn, Z. Jiang, C. S. Lee, H. Y. Chen, J. Liang, L. S. Liyanage, H. S. P. Wong, *IEEE Trans. Electron Devices* **2015**, *62*, 2197.
[244] Y. B. Kim, S. R. Lee, D. Lee, C. B. Lee, M. Chang, J. H. Hur, M. J. Lee, G. S. Park, C. J. Kim, U. Chung, I. K. Yoo, K. Kim, in *2011 Symp. on VLSI Technology - Digest of Technical Papers*, IEEE, Honolulu, HI, USA **2011**, 52.
[245] V. K. Nagareddy, A. K. Ott, C. Dou, T. Tsvetkova, M. Sandulov, M. F. Craciun, A. C. Ferrari, C. D. Wright, unpublished.
[246] X. Cao, X. M. Li, X. D. Gao, W. D. Yu, X. J. Liu, Y. W. Zhang, L. D. Chen, X. H. Cheng, *J. Appl. Phys.* **2009**, *106*, 073723.

