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High-Field Transport and Velocity Saturation in Synthetic Monolayer MoS_2

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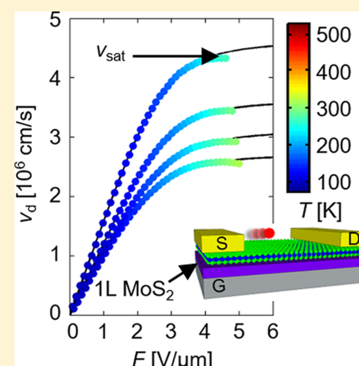
Supporting Information

ABSTRACT: Two-dimensional semiconductors such as monolayer MoS_2 are of interest for future applications including flexible electronics and end-of-roadmap technologies. Most research to date has focused on low-field mobility, but the peak current-driving ability of transistors is limited by the high-field saturation drift velocity, v_{sat}. Here, we measure high-field transport as a function of temperature for the first time in high-quality synthetic monolayer MoS_2. We find that in typical device geometries (e.g. on SiO_2 substrates) self-heating can significantly reduce current drive during high-field operation. However, with measurements at varying ambient temperature (from 100 to 300 K), we extract electron $v_{sat} = (3.4 \pm 0.4) \times 10^6$ cm/s at room temperature in this three-atom-thick semiconductor, which we benchmark against other bulk and layered materials. With these results, we estimate that the saturation current in monolayer MoS_2 could exceed 1 mA/μm at room temperature, in digital circuits with near-ideal thermal management.



KEYWORDS: *MoS_2, 2D materials, chemical vapor deposition (CVD), saturation velocity, transfer length method, high-field transport*

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Two-dimensional (2D) materials are interesting for specialized electronics due to several features uncommon among three-dimensional (3D) bulk materials, including transparency,[1,2] flexibility,[3−5] and the ability to easily manipulate spin and valley polarizations.[6−8] To date, however, most electronic studies of 2D materials have focused on their contacts and properties at low (lateral) electric fields. While these represent an important starting point, the performance of nanoscale transistors is not necessarily limited by low-field parameters such as the mobility.

As lateral electric fields in a field-effect transistor (FET) increase, the average drift velocity of charge carriers (v_d) approaches a saturation value (v_{sat}) due to increased scattering with phonons.[9] For example, in silicon and many other semiconductors, velocity saturation occurs at lateral fields in excess of ∼1 V/μm, which are easily achievable in submicron transistors.[10−13] This is important because the peak current-driving ability of such devices has less dependence on the low-field mobility and is instead proportional to v_{sat}. For example, v_{sat} limits the maximum intrinsic frequency at which a FET can switch, $f_T \sim v_{sat}/(2\pi L)$,[10,14] where L is the channel length of the device. Even in nanoscale FETs, where velocity overshoot or quasi-ballistic effects become important, a subset of charge carriers are ultimately limited by velocity saturation effects.

Among 3D bulk semiconductors, these high-field properties have been explored since the 1950s,[15,16] and researchers have generally found that v_{sat} scales as $(\hbar\omega_{OP}/m^*)^{1/2}$, illustrating its dependence on optical phonon energy ($\hbar\omega_{OP}$) and electron or hole effective mass (m^*).[10] In contrast, little is known about drift velocity saturation in 2D semiconductors. For 2D monolayer graphene (a semimetal), v_{sat} has been measured up to 3×10^7 cm/s on SiO_2[17] and up to 6×10^7 cm/s on hexagonal boron nitride (h-BN) substrates[18] at room temperature and has been found to scale inversely with the square root of carrier density. In comparison, $v_{sat} \approx 10^7$ cm/s in bulk Si[13,19,20] and ∼7×10^6 cm/s in bulk Ge,[21] for electrons. Among 2D layered semiconductors, indirect v_{sat} estimates exist for electrons in few-layer MoS_2 (∼2.8×10^6 cm/s)[22] and monolayer MoS_2 (∼3.8×10^6 cm/s).[23] However, these were achieved by simultaneous fitting of v_{sat} to electrical data along with the contact resistance (R_C) and effective mobility (μ_{eff}). Another way of estimating v_{sat} is through radio frequency (RF) measurements of f_T, which have been utilized to estimate $v_{sat} \approx 1.1 \times 10^6$ cm/s in monolayer MoS_2[14] and ∼5.5×10^6 cm/s in relatively thick (>10 nm) black phosphorus.[24]

In this work, we perform the first direct measurements of drift velocity saturation in technologically relevant large-area synthetic monolayer (1L) MoS_2. We perform high-field measurements as a function of ambient temperature, from 100 to 300 K, while carefully accounting for contact resistance and self-heating effects. We uncover a saturation velocity of ∼3.4×10^6 cm/s at room temperature in this three-atom-thick semiconductor, once self-heating effects are taken into account. We also place these results in context, both in terms of their significance for 2D transistors as well as in comparison to representative bulk, 3D materials.

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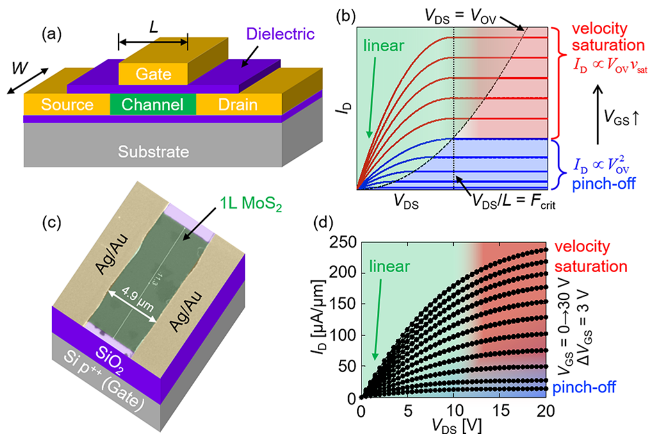

Figure 1. (a) Diagram of a typical semiconductor-on-insulator FET. (b) Illustration of I_D versus V_{DS} characteristics (increasing V_{GS} with constant steps) for an n-type FET including velocity saturation. Saturation current scales quadratically with V_{OV} ($= V_{GS} - V_T$) for a pinched-off channel but linearly with V_{OV} when the drift velocity saturates. Importantly, I_D can be limited by velocity saturation even when the FET is not pinched-off. (c) False-color SEM image of a back-gated 1L MoS_2 FET on 30 nm SiO_2 with 4.9 μm channel length. These dimensions are appropriate for seeing both pinch-off and velocity saturation in one set of I_D-V_{DS} measurements. (d) The DC forward and backward I_D-V_{DS} measurements of the device in (c), showing negligible hysteresis. The bottom curves saturate for $V_{DS} > V_{OV}$ due to pinch-off, but the upper curves also saturate despite all $V_{DS} < V_{OV}$ due to velocity saturation.

In an ideal long-channel n-type FET (Figure 1a,b) when the drain-to-source voltage (V_{DS}) exceeds the overdrive voltage ($V_{OV} = V_{GS} - V_T$, where V_{GS} and V_T are the gate-to-source and threshold voltages[25]), the carrier density in the channel becomes pinched-off near the drain, and the current (I_D) saturates to[11]

$$I_{D,sat} \approx \frac{W\mu_{eff} C_{ox} {V_{OV}}^2}{2L} \tag{1}$$

where W and L are the channel width and length, and C_{ox} is the gate oxide capacitance. However, at lateral fields greater than a critical field strength ($F_{crit} \sim 1$ V/μm in many semiconductors[10−12]), v_d approaches v_{sat} and the current is limited to a maximum of[11]

$$I_{D,vsat} \approx (WC_{ox}V_{OV})v_{sat} \tag{2}$$

Comparing these two expressions, we note that a crossover between these regimes will occur when the average lateral field $V_{OV}/L \approx 2v_{sat}/\mu_{eff}$[26] and a properly designed device will be able to saturate by either mechanism depending on biasing.

These two saturation regimes and their crossover point are represented schematically in Figure 1b. Note that there are three regions of operation: linear (also known as triode, green region), pinch-off (blue region), and velocity saturation (red region). In the triode regime, the current first increases linearly with both V_{DS} and V_{GS} and begins to bend over as $V_{DS} \rightarrow V_{OV}$. For lower overdrives, the current saturates due to channel pinch-off near the drain, and $I_{D,sat}$ has a quadratic relationship with V_{OV}, as shown in eq 1 and in the blue region of Figure 1b. For higher overdrives, carrier velocity saturates at lateral V_{DS} (and average lateral fields) lower than required to cause pinch-off. In this case, $I_{D,vsat}$ scales only linearly with V_{OV} (eq 2 and red region of Figure 1b), and the spacing between measured I_D curves becomes constant.

Figure 1c shows a scanning electron microscope (SEM) image of a MoS_2 FET designed to demonstrate the behavior described above. We fabricated devices several microns long with single-crystal 1L MoS_2 grown by large-area chemical vapor deposition (CVD)[27] directly on t_{ox} = 30 nm SiO_2/Si (p^+) substrates, which also serve as back-gates. Grain sizes are ∼100 μm, much larger than the devices measured here.[28] We use Ag/Au contacts[14] deposited under high vacuum[29] such that the total contact resistance ($2R_C$) is <5% of the total device resistance (R_{TOT}, discussed later). Gentle O_2 plasma is employed to etch the channels into a controlled width while minimizing resist residues.[28]

Measured forward and backward I_D-V_{DS} characteristics of such a device are shown in Figure 1d (I_D-V_{GS} can be found in Supporting Information A, revealing $V_T \approx -1$ V). Note that for the lower curves, $V_{OV} < V_{DS}$ and the device achieves classical pinch-off at high V_{DS}, where I_D saturates with output resistance up to $r_0 \equiv \partial I_D/\partial V_{DS}$ = 36 M$\Omega \cdot \mu$m. However, for the upper curves, $V_{OV} > V_{DS}$ and the device is in the linear regime, yet I_D continues to show saturation-like behavior. The approximately constant spacing between I_D-V_{DS} curves of varying V_{GS} also confirms the device behavior is limited by v_{sat} as previously discussed, and from this relationship we can estimate $v_{sat} \geq 0.9 \times 10^6$ cm/s. However, as we will show, this device experiences significant self-heating at these voltage and current levels (even causing sublinear behavior of $\partial I_{D,sat}/\partial V_{OV}$ for the highest levels of I_D) and thus a more careful approach is required to estimate v_{sat} from experimental data.

To this end, we perform rigorous measurements of v_d versus lateral electric field (F) in 1L MoS_2 for the first time. Additionally, through temperature-dependent measurements and detailed modeling, we decouple the effects of temperature and electric field on high-field transport. We measure electron v_d at various ambient temperatures by biasing long-channel devices in the linear regime such that the lateral field ($F = |V_{DS}'|/L$) is nearly constant along the channel and the measured current is[30,31]

$$I_D = W|Q_{eff}|v_d \tag{3}$$

where V_{DS}' is the intrinsic drain-to-source voltage (after subtracting contact resistance, which is $<0.05R_{TOT}$) and $Q_{eff} \approx -C_{ox}(V_{OV} - V_{DS}'/2)$, is the effective charge in the channel. The term $V_{DS}'/2$ accounts for the average carrier density between the source and drain.

Low-Field Measurements and Contacts. In order to obtain V_{DS}' for accurate extractions of F and Q_{eff}, it is necessary to have an accurate measurement of R_C. To this end, we fabricate transfer length method (TLM) structures on the same CVD-grown 1L MoS_2. Electron-beam lithography is used to pattern Ag/Au contacts with varying channel lengths down to 72 nm to ensure an accurate extraction of R_C,[29] as shown in the SEM image of Figure 2a. For all data discussed in this paper, devices are measured in vacuum (∼10^{-5} Torr) following a 2 hour *in situ* anneal at 250 °C to drive off adsorbates that can cause hysteresis.[32]

As described elsewhere,[27,29] we measure the I_D-V_{GS} relationship of each of these devices and plot the total resistance R_{TOT} versus L for various values of carrier density $n \approx C_{ox}V_{OV}/q$ (see Figure 2b and Supporting Information B). From this TLM plot, reliable values for R_C and μ_{eff} can be estimated as a function of n, as depicted in Figures 2c,d. V_{DS} =

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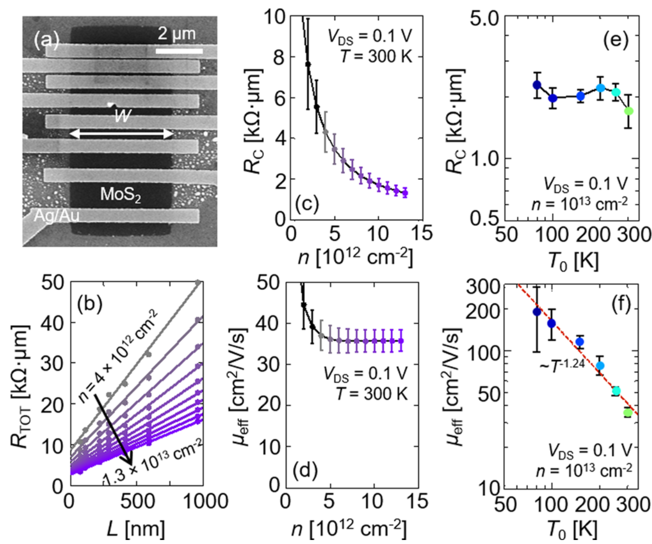

Figure 2. Low-field mobility and contact resistance of 1L MoS_2 devices. (a) SEM image of the TLM structures, on SiO_2 substrate. L and W were measured with higher resolution SEM images similar to this. (b) TLM plot generated using data (symbols) from all devices at T_0 = 300 K. The ordinate intercept of the fit (lines) is $2R_C$ and the slope of each line is inversely proportional to μ_{eff}. (c) R_C versus n, revealing a minimum value of 1.3 ± 0.2 kΩ·µm at $n = 1.3 \times 10^{13}$ cm^{-2}. Purple color gradient is indicative of increasing n, and can be fit with a simple power law, $R_C = An^B + C$. (d) μ_{eff} versus n, approaching 35.7 ± 2.6 $cm^2/V/s$ at high carrier density. Error bars reflect confidence intervals of 95% from least-squares fitting. (e) Contact resistance R_C versus ambient temperature T_0, showing that R_C is approximately constant within the error bars. This is likely caused by competing effects of increased thermionic emission and decreased μ_{eff} in the MoS_2 underneath the contacts, counteracting each other as a function of T_0.[29] (f) μ_{eff} versus T_0, revealing a phonon-limited dependence $\propto T_0^{-1.24}$.

0.1 V is kept deliberately low to avoid self-heating and to ensure reliable extractions for these measurements. Here, we obtain lowest values of R_C and μ_{eff} of 1.3 ± 0.2 kΩ·µm and 35.7 ± 2.6 $cm^2/V/s$, respectively, at 300 K and $n \approx 1.3 \times 10^{13}$ cm^{-2}. With the transmission line model,[33] we also estimate a lowest specific contact resistivity $\rho_C = 1.3 \times 10^{-6}$ Ω·cm^2 and current transfer length $L_T \approx 100$ nm, as detailed in Supporting Information C.

We perform identical measurements as a function of ambient temperature, T_0, to provide us with similar information at lower temperatures. Figure 2e shows that to first order R_C is largely independent of T_0 and can be approximated as a function of only n by fitting with a simple power law. Conversely, we observe μ_{eff} to be independent of n but to scale as $T_0^{-1.24}$ in Figure 2f, reaching ~191 $cm^2/V/s$ at 80 K. This mobility value is a factor of two higher than previous reports for synthetic 1L MoS_2 on SiO_2,[34] attesting to the high quality of our films. However, the temperature exponent is lower than the theoretically predicted value of 1.69,[35] indicating scattering contributions from both intrinsic MoS_2 and SiO_2 substrate phonons, limiting the mobility. We also note that our μ_{eff} does not plateau at the lowest T_0 probed here, suggesting that Coulomb scattering with charged impurities is not dominant,[36,37] at least at $T_0 \geq 80$ K. Finally, we note that our μ_{eff} is about two-thirds the Hall mobility (μ_{Hall}) of 1L CVD-grown MoS_2 sandwiched between h-BN at these temperatures.[38] This is unsurprising since, as a substrate, h-BN will cause less scattering than SiO_2, and μ_{eff} is additionally expected to be lower than μ_{Hall} by a factor dependent on the effective scattering time of carriers.[10,39]

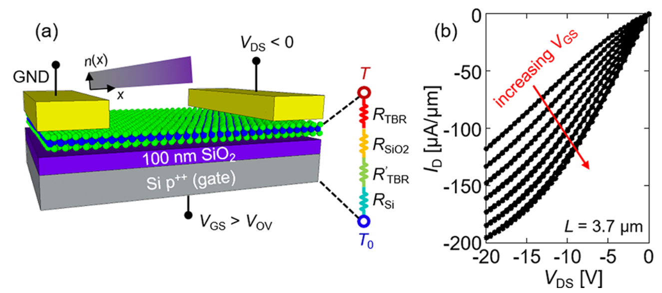

Figure 3. (a) Device schematic showing carrier density and thermal resistances accounted for in our model. On 100 nm SiO_2, the TBR at the MoS_2−SiO_2 interface[40] accounts for ~36% of the total thermal resistance, at room temperature. R'_{TBR} is the (small) thermal resistance of the SiO_2−Si interface. (See Supporting Information E for additional details.) (b) I_D versus V_{DS} curves of a 1L MoS_2 FET measured with pulse widths of 100 µs.[50,51] Sweeping $V_{DS} < 0$ ensures the device does not enter pinch-off and the electric field is nearly constant along the channel. V_{GS} = 0 to 30 V with ΔV_{GS} = 5 V.

High-Field Measurements and Modeling. For our high-field measurements, we use long-channel FETs[28] (as in Figure 1c) with the same contacts as the TLM structures. Devices with $L > 3$ µm are chosen such that device performance is dominated by the channel, even at very high n ($2R_C/R_{TOT} \leq 0.05$, see Supporting Information D), yet lateral electric fields can reach $F > 5$ V/µm without gate leakage. A schematic of this device is illustrated in Figure 3a along with the thermal resistance network used to calculate the *in operando* device temperature (T). This thermal model was independently confirmed by Raman thermometry[40] and includes the non-negligible thermal boundary resistance of the MoS_2−SiO_2 interface (TBR ~ 7×10^{-8} m^2K/W at 300 K).[41] The average device temperature can be calculated as

$$T = T_0 + \left(\frac{I_D}{W}\right) F R_{th} \left[1 - \frac{2L_H \tanh\left(\frac{L}{2L_H}\right)}{L}\right] \quad (4)$$

where R_{th} is the "vertical" thermal resistance per unit area[42−47] separating the MoS_2 channel (at T) and the Si substrate (at T_0),[48,49] while the term in square brackets accounts for lateral heat loss to the contacts. Here L_H is the thermal healing length along the MoS_2 (~50 to 100 nm for these devices).[41] For a more in-depth discussion of thermal resistance modeling, see Supporting Information E.

In order to measure v_d at higher values of lateral F, 1L MoS_2 was grown by CVD on t_{ox} = 100 nm SiO_2, such that if a device under test were to fail, breakdown would occur in the channel near the drain instead of at the gate (see Supporting Information F). For these measurements, we bias the device in the linear and strong accumulation regimes ($V_{GS} > V_T$, $V_{DS} < 0$) such that the charge in the channel is approximately uniform and F is nearly constant throughout the channel. Although hysteresis is very small at room temperature, pulsed measurements are utilized for these experiments (with pulse widths τ_p = 100 µs),[50,51] because residual water vapor and other adsorbates begin to settle on the channel at low T_0 and can cause some hysteresis in direct current (DC) measurements.[32,52] These measurements produce negative I_D versus

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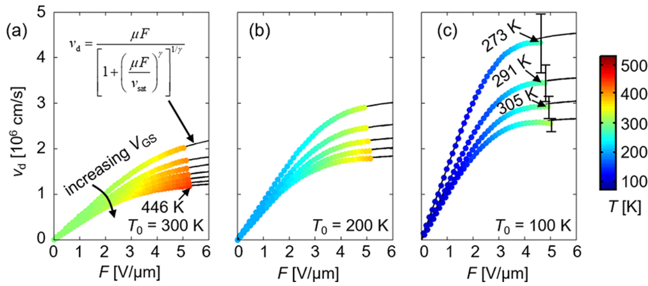

Figure 4. Extracted velocity-field relationships at (a) T_0 = 300 K ambient, from the raw data in Figure 3b. Similar data are extracted at (b) T_0 = 200 K and (c) 100 K ambient. Symbols are data points with colors indicative of device operating T from eq 4, and black lines are empirical fits using eq 5. Error bars are calculated as explained in Supporting Information J. The device self-heats by ΔT up to ~200 K at lateral fields in the velocity saturation regime. v_d and hence v_{sat} increase at lower T, as expected.

V_{DS} data as shown in Figure 3b and Supporting Information G. Note that the data remain linear for most of the curve (these measurements are taken in the linear regime, as opposed to Figure 1d) but do begin to saturate at higher $|V_{DS}|$ due to self-heating effects and the onset of velocity saturation.

From these data, we extract v_d directly with eq 3 and $V_{DS}' = V_{DS} - (I_D/W)(R_{CS} + R_{CD})$, where R_{CS} and R_{CD} are the contact resistance at the source and drain for their respective n, as calculated from the TLM data in Figure 2. V_T is estimated by linear extrapolation from independent I_D versus V_{GS} measurements, also shown in Supporting Information G. Following this, we plot v_d versus F and fit these data with the well-known Caughey-Thomas model[17,20,30,31,53,54]

$$v_d = \frac{\mu_{LF}F}{\left[1 + \left(\frac{\mu_{LF}F}{v_{sat}}\right)^{\gamma}\right]^{1/\gamma}} \tag{5}$$

Here, the low-field mobility $\mu_{LF} \equiv (\partial v_d/\partial F)|_{F\to 0}$ is taken from the slope of v_d versus F, γ is an empirical fitting parameter, and v_{sat} is fit to the high-field region. Figure 4a shows data and fits of v_d versus F at T_0 = 300 K, corresponding to the measurements in Figure 3b. The color of each symbol indicates its operating temperature at each bias, from eq 4. To verify again that R_C plays a very small role in our device behavior, we first examine $\mu_{LF} \approx 36.7$ cm^2/V/s at 300 K, in excellent agreement with μ_{eff} and the field-effect mobility, μ_{FE} (see Supporting Information H). Unlike in Si, however, where commonly $\gamma \approx 2$ for electrons and ~1 for holes,[55] here we allow γ to take its best fit value (ranging from 2.8 to 4.8) due to the large and varying amounts of self-heating observed for each curve (similar to previous work on silicon-on-insulator [SOI] devices[30]).

Our observed values of v_d as they begin to saturate fall in the range of 1 to 2 × 10^6 cm/s, and the Caughey-Thomas model fits return v_{sat} from 1.3 to 2.5 × 10^6 cm/s. While these values are over four times lower than v_{sat} in bulk Si,[19,56] to a large degree they are limited by both the heavier electron effective mass and by lower phonon energies in MoS_2 and could also be influenced by the SiO_2 substrate. Moreover, these MoS_2 devices self-heat significantly at the high fields measured here due to the thermal resistance of the MoS_2−SiO_2 interface,[40,41] that of the SiO_2 substrate, and to a lesser degree that of the Si wafer. These aspects are all captured by the thermal model described earlier.[48,49]

To distinguish the effects of self-heating on v_{sat}, we perform similar measurements at lower ambient temperature (T_0 = 200 and 100 K) as shown in Figures 4b,c (other temperatures can be found in Supporting Information I along with a plot of estimated v_{sat} versus T). Our devices self-heat by up to $\Delta T \sim$ 200 K at the highest carrier densities (>10^{13} cm^{-2}) and electric fields probed. Thus, by lowering the ambient temperature during measurement, the device temperature will likewise be reduced ($T = T_0 + \Delta T$), enabling the extraction of v_{sat} near 300 K. The color bar and colored data points in Figure 4 illustrate the temperatures reached during device operation. In Figure 4c, we observe that when the device self-heats to $T \approx 291$ K (the second curve), v_d saturates near $v_{sat} \approx (3.4 \pm 0.4) \times 10^6$ cm/s. (For a discussion of uncertainty values, see Supporting Information J.) This value is in good agreement with recent density functional theory (DFT)[57,58] and Monte Carlo simulations.[59]

Finally, from our high-field measurements we can estimate the maximum saturation current ($I_{sat} = qnv_{sat}$) expected in such a three-atom-thick semiconductor. Without self-heating, we calculate that I_{sat} could exceed 1 mA/μm for $n \geq 2 \times 10^{13}$ cm^{-2} when limited only by v_{sat} at room temperature. This is an important metric, comparable to mature transistor technologies like Si or GaN, and to International Technology Roadmap for Semiconductors (ITRS) requirements.[60] High saturation current is essential for fast circuit operation, because the intrinsic delay of transistors scales as CV/I_{sat}, where C is the load capacitance and V is the operating voltage.

Although we do not expect $I_{sat} \geq 1$ mA/μm for 1L MoS_2 FETs in DC operation due to self-heating, such current drives could be realized in digital circuits, where switching times are significantly faster than the device thermal time constants, τ_{th}. For 1L MoS_2 (or any 2D semiconductor-on-insulator device), τ_{th} is strongly dependent on device geometry and is expected to be at least ten and up to several hundreds of nanoseconds.[61] Therefore, devices operating at frequencies in the gigahertz regime (<1 ns) should not experience significant self-heating on their own. This is very similar to what has already been demonstrated in SOI devices, where τ_{th} has been measured to be several tens of nanoseconds[62] and thus device temperatures during digital operation remain much lower than would otherwise be expected for DC power dissipation.[63−65]

Before concluding, we put our measurements for monolayer MoS_2 into context by plotting v_{sat} for several materials versus their band gaps in Figure 5. (A table of values is provided in Supporting Information K.) Among 2D layered materials, v_{sat} has only been measured or estimated for electrons in 1L graphene[17,18] and for holes in thicker flakes (>10 nm) of black phosphorus (BP).[24] Although v_{sat} values reported for these materials are somewhat higher than our results for 1L MoS_2, graphene and thick BP have very small band gaps (0 and <0.3 eV,[66] respectively) and are therefore not well-suited for logic applications. By contrast, the other materials[21,67−72] shown in Figure 5 have only been measured in regimes where they maintain their bulk properties (i.e., thicknesses ≫ 1 nm) and so can only be indirectly compared to 1L MoS_2. Thus, our measurements of v_{sat} in monolayer MoS_2 provide promising results for logic transistor applications of atomically thin 2D materials.

In summary, we performed measurements of electron drift velocity in monolayer MoS_2 transistors, where contact

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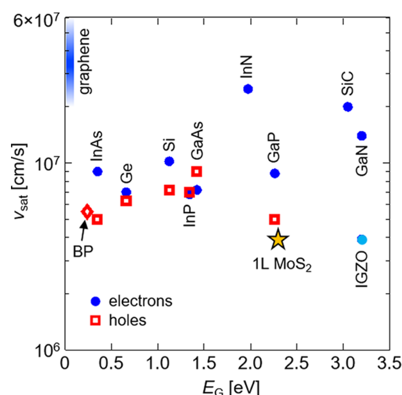

Figure 5. Summary of saturation velocity versus band gap for various bulk and a few layered materials at room temperature.[21,67−72] With the exception of graphene, which lacks a band gap, 1L MoS_2 is the only atomically thin (sub-1 nm) material shown, yet retains appreciable v_{sat}. (Note the electronic band gap of 1L MoS_2 is greater than the optical gap typically obtained from photoluminescence experiments.[73]) 1L graphene v_{sat} scales with the inverse square root of carrier density in the range shown on SiO_2 or h-BN substrates.[17,18] BP = black phosphorus (∼10 nm thick).[24] For some materials (e.g., GaAs, GaN, InN) the peak electron drift velocity can be ∼50% higher than the saturation velocity shown.[67,69,70] The *c*-axis-aligned crystalline IGZO saturation velocity is an estimate based on simulations.[68]

resistance and self-heating effects were carefully measured and accounted for. Using a thermal model calibrated against previous experiments, we found that MoS_2 devices on 100 nm SiO_2 (on Si) self-heat by up to ∼200 K in the regime necessary to observe clear velocity saturation effects. With measurements carried out in 100 K ambient, we estimated $v_{sat} \approx 3.4 \times 10^6$ cm/s in this three-atom-thick material when the device is operating near room temperature. In practice and under DC operation, the saturation velocity is severely limited by self-heating. However, our results suggest that current drives in MoS_2 digital circuits could exceed 1 mA/μm if self-heating can be mitigated by fast switching speeds. This knowledge of v_{sat} will be useful for all future applications involving atomically thin MoS_2, including flexible, transparent, and high-performance devices.

During review, we became aware of a new study of saturation velocity in thick (∼10 nm) multilayer BP encapsulated by h-BN at low carrier densities.[74]

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.8b01692.

> Long-channel transfer characteristics, transfer and output characteristics for a 72 nm device, contact resistivity and transfer length, device measurement considerations, thermal resistance modeling, device breakdown at high fields, transfer and output characteristics, clarification of mobility definitions, drift velocity data for additional temperatures, measurement and modeling uncertainty, comparison with saturation velocity in other semiconductors and graphene, electron temperature estimates (PDF)

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Notes

The authors declare no competing financial interest.

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■ REFERENCES

(1) Lee, G.-H.; et al. Flexible and Transparent MoS_2 Field-Effect Transistors on Hexagonal Boron Nitride-Graphene Heterostructures. *ACS Nano* **2013**, *7* (9), 7931−7936.

(2) Park, J.; Choudhary, N.; Smith, J.; Lee, G.; Kim, M.; Choi, W. Thickness modulated MoS_2 grown by chemical vapor deposition for transparent and flexible electronic devices. *Appl. Phys. Lett.* **2015**, *106* (1), 012104.

(3) Chang, H.; et al. High-Performance, Highly Bendable MoS_2 Transistors with High-K Dielectrics for Flexible Low-Power. *ACS Nano* **2013**, *7*, 5446−5452.

(4) Zhao, J.; Chen, W.; Meng, J.; Yu, H.; Liao, M.; Zhu, J.; Yang, R.; Shi, D.; Zhang, G. Integrated Flexible and High-Quality Thin Film Transistors Based on Monolayer MoS_2. *Adv. Electron. Mater.* **2016**, *2* (3), 1500379.

(5) Chang, H.-Y.; Yogeesh, M. N.; Ghosh, R.; Rai, A.; Sanne, A.; Yang, S.; Lu, N.; Banerjee, S. K.; Akinwande, D. Large-Area Monolayer MoS_2 for Flexible Low-Power RF Nanoelectronics in the GHz Regime. *Adv. Mater.* **2016**, *28* (9), 1818−1823.

(6) Xiao, D.; Liu, G.-B; Feng, W.; Xu, X.; Yao, W. Coupled spin and valley physics in monolayers of MoS_2 and other group-VI dichalcogenides. *Phys. Rev. Lett.* **2012**, *108* (19), 196802.

(7) Zeng, H.; Dai, J.; Yao, W.; Xiao, D.; Cui, X. Valley polarization in MoS_2 monolayers by optical pumping. *Nat. Nanotechnol.* **2012**, *7* (8), 490−493.

(8) Mak, K. F.; He, K.; Shan, J.; Heinz, T. F. Control of valley polarization in monolayer MoS_2 by optical helicity. *Nat. Nanotechnol.* **2012**, *7* (8), 494−498.

(9) Pop, E.; Dutton, R. W.; Goodson, K. E. Monte Carlo simulation of Joule heating in bulk and strained silicon. *Appl. Phys. Lett.* **2005**, *86* (8), 082101.

(10) Sze, S. M.; Ng, K. K. *Physics of Semiconductor Devices*, 3rd ed.; John Wiley & Sons: Hoboken, NJ, 2007.

(11) Taur, Y.; Ning, T. H. *Fundamentals of Modern VLSI Devices*, 2nd ed.; Cambridge University Press: Cambridge, 2009.

(12) Jacoboni, C.; Canali, C.; Ottaviani, G.; Alberigi Quaranta, A. A review of some charge transport properties of silicon. *Solid-State Electron.* **1977**, *20*, 77−89.

(13) Canali, C.; Jacoboni, C.; Nava, F.; Ottaviani, G.; Alberigi-Quaranta, A. Electron drift velocity in silicon. *Phys. Rev. B* **1975**, *12* (6), 2265−2284.
(14) Sanne, A.; et al. Radio Frequency Transistors and Circuits Based on CVD MoS_2. *Nano Lett.* **2015**, *15*, 5039−5045.
(15) Shockley, W. Hot Electrons in Germanium and Ohm's Law. *Bell Syst. Tech. J.* **1951**, *30* (4), 990−1034.
(16) Ryder, E. J. Mobility of Holes and Electrons in High Electric Fields. *Phys. Rev.* **1953**, *90* (5), 766−769.
(17) Dorgan, V. E.; Bae, M. H.; Pop, E. Mobility and saturation velocity in graphene on SiO_2. *Appl. Phys. Lett.* **2010**, *97* (8), 082112.
(18) Yamoah, M. A.; Yang, W.; Pop, E.; Goldhaber-Gordon, D. High-Velocity Saturation in Graphene Encapsulated by Hexagonal Boron Nitride. *ACS Nano* **2017**, *11* (10), 9914−9919.
(19) Norris, C. B.; Gibbons, J. F. Measurement of High-Field Carrier Drift Velocities in Silicon by a Time-of-Flight Technique. *IEEE Trans. Electron Devices* **1967**, *14* (1), 38−43.
(20) Cooper, J. A.; Nelson, D. F. High-field drift velocity of electrons at the Si-SiO_2 interface as determined by a time-of-flight technique. *J. Appl. Phys.* **1983**, *54* (3), 1445−1456.
(21) Quay, R.; Moglestue, C.; Palankovski, V.; Selberherr, S. A temperature dependent model for the saturation velocity in semiconductor materials. *Mater. Sci. Semicond. Process.* **2000**, *3* (1−2), 149−155.
(22) Fiori, G.; Szafranek, B. N.; Iannaccone, G.; Neumaier, D. Velocity saturation in few-layer MoS_2 transistor. *Appl. Phys. Lett.* **2013**, *103*, 233509.
(23) He, G.; et al. Conduction Mechanisms in CVD-Grown Monolayer MoS_2 Transistors: From Variable-Range Hopping to Velocity Saturation. *Nano Lett.* **2015**, *15* (8), 5052−5058.
(24) Zhu, W.; Park, S.; Yogeesh, M. N.; McNicholas, K. M.; Bank, S. R.; Akinwande, D. Black Phosphorus Flexible Thin Film Transistors at Gighertz Frequencies. *Nano Lett.* **2016**, *16* (4), 2301−2306.
(25) Ortiz-Conde, A.; García Sánchez, F. J.; Liou, J. J.; Cerdeira, A.; Estrada, M.; Yue, Y. A review of recent MOSFET threshold voltage extraction methods. *Microelectron. Reliab.* **2002**, *42*, 583−596.
(26) This simple discussion refers to average lateral fields; however, the electric field distribution along the channel of a typical MOSFET is peaked near the drain. Thus, as V_{DS} increases, velocity saturation first occurs near the drain and then gradually along the entire channel; see, for example, refs 10 and 11.
(27) Smithe, K. K. H.; English, C. D.; Suryavanshi, S. V.; Pop, E. Intrinsic electrical transport and performance projections of synthetic monolayer MoS_2 devices. *2D Mater.* **2017**, *4*, 011009.
(28) Smithe, K. K. H.; Suryavanshi, S. V.; Muñoz Rojo, M.; Tedjarati, A. D.; Pop, E. Low Variability in Synthetic Monolayer MoS_2 Devices. *ACS Nano* **2017**, *11* (8), 8456−8463.
(29) English, C. D.; Shine, G.; Dorgan, V. E.; Saraswat, K. C.; Pop, E. Improved Contacts to MoS_2 Field-Effect Transistors by Ultra-High Vacuum Metal Deposition. *Nano Lett.* **2016**, *16* (6), 3824−3830.
(30) Assaderaghi, F.; Sinitsky, D.; Bokor, J.; Ko, P. K.; Gaw, H.; Hu, C. High-Field Transport of Inversion-Layer Electrons and Holes Including Velocity Overshoot. *IEEE Trans. Electron Devices* **1997**, *44* (4), 664−671.
(31) Sodini, C. G.; Ko, P. K.; Moll, J. L. The Effect of High Fields on MOS Device and Circuit Performance. *IEEE Trans. Electron Devices* **1984**, *31* (10), 1386−1393.
(32) Illarionov, Y. Y.; Smithe, K. K. H.; Waltl, M.; Knobloch, T.; Pop, E.; Grasser, T. Improved Hysteresis and Reliability of MoS_2 FETs with High-Quality CVD Growth and Al_2O_3 Encapsulation. *IEEE Electron Device Lett.* **2017**, *38* (12), 1763−1766.
(33) Berger, H. H. Models for contacts to planar devices. *Microelectron. Reliab.* **1972**, *15* (2), 145−158.
(34) Kang, K.; Xie, S.; Huang, L.; Han, Y.; Huang, P. Y.; Mak, K. F.; Kim, C.-J.; Muller, D.; Park, J. High-mobility three-atom-thick semiconducting films with wafer-scale homogeneity. *Nature* **2015**, *520* (7549), 656−660.
(35) Kaasbjerg, K.; Thygesen, K. S.; Jacobsen, K. W. Phonon-limited mobility in n-type single-layer MoS_2 from first principles. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2012**, *85* (11), 115317.
(36) Zeng, L.; Xin, Z.; Chen, S.; Du, G.; Kang, J.; Liu, X. Remote phonon and impurity screening effect of substrate and gate dielectric on electron dynamics in single layer MoS_2. *Appl. Phys. Lett.* **2013**, *103*, 113505.
(37) Davies, J. *The Physics of Low-Dimensional Semiconductors*; Cambridge University Press, 1998.
(38) Cui, X.; et al. Multi-terminal transport measurements of MoS_2 using a van der Waals heterostructure device platform. *Nat. Nanotechnol.* **2015**, *10*, 534−540.
(39) Lundstrom, M. *Modular Series on Solid State Devices, Vol. X*; Neudeck, G. W., Pierret, R. F., Eds.; Addison-Wesley: Reading, MA, 1990.
(40) Yalon, E.; et al. Temperature-Dependent Thermal Boundary Conductance of Monolayer MoS_2 by Raman Thermometry. *ACS Appl. Mater. Interfaces* **2017**, *9* (49), 43013−43020.
(41) Yalon, E.; et al. Energy Dissipation in Monolayer MoS_2 Electronics. *Nano Lett.* **2017**, *17* (6), 3429−3433.
(42) Yamane, T.; Nagai, N.; Katayama, S.; Todoki, M. Measurement of thermal conductivity of silicon dioxide thin films using a 3 omega method. *J. Appl. Phys.* **2002**, *91* (12), 9772−9776.
(43) Andersson, S.; Dzhavadov, L. Thermal conductivity and heat capacity of amorphous SiO_2: pressure and volume dependence. *J. Phys.: Condens. Matter* **1992**, *4*, 6209−6216.
(44) Chien, H. C.; Yao, D. J.; Huang, M. J.; Chang, T. Y. Thermal conductivity measurement and interface thermal resistance estimation using SiO_2 thin film. *Rev. Sci. Instrum.* **2008**, *79* (5), 054902.
(45) Yovanovich, M. M.; Culham, J. R.; Teertstra, P. Analytical Modeling of Spreading Resistance in Flux Tubes, Half Spaces, and Compound Disks. *IEEE Trans. Compon., Packag., Manuf. Technol., Part A* **1998**, *21* (1), 168−176.
(46) Asheghi, M.; Kurabayashi, K.; Kasnavi, R.; Goodson, K. E. Thermal conduction in doped single-crystal silicon films. *J. Appl. Phys.* **2002**, *91* (8), 5079−5088.
(47) Asheghi, M.; Touzelbaev, M. N.; Goodson, K. E.; Leung, Y. K.; Wong, S. S. Temperature-Dependent Thermal Conductivity of Single-Crystal Silicon Layers in SOI Substrates. *J. Heat Transfer* **1998**, *120*, 30−36.
(48) Mleczko, M. J.; Xu, R. L.; Okabe, K.; Kuo, H.-H.; Fisher, I. R.; Wong, H.-S. P.; Nishi, Y.; Pop, E. High Current Density and Low Thermal Conductivity of Atomically Thin Semimetallic WTe_2. *ACS Nano* **2016**, *10* (8), 7507−7514.
(49) Suryavanshi, S. V.; Pop, E. S2DS: Physics-based compact model for circuit simulation of two-dimensional semiconductor devices including non-idealities. *J. Appl. Phys.* **2016**, *120*, 224503.
(50) Datye, I. M.; Gabourie, A. J.; English, C. D.; Wang, N. C.; Pop, E. Reduction of Hysteresis in MoS_2 Transistors Using Pulsed Voltage Measurements. *IEEE Device Res. Conf.* **2016**, 1−2.
(51) Pulse widths sufficiently short to eliminate self-heating (∼1 ns) are impractical with our setup, requiring insulating substrates (without the ability to back-gate) to reduce parasitic capacitance contributions.
(52) Illarionov, Y. Y.; Rzepa, G.; Waltl, M.; Knobloch, T.; Grill, A.; Furchi, M. M.; Mueller, T.; Grasser, T. The role of charge trapping in MoS_2/SiO_2 and MoS_2/hBN field-effect transistors. *2D Mater.* **2016**, *3* (3), 035004.
(53) Sinitsky, D.; Assaderaghi, F.; Hu, C.; Bokor, J. High-Field Hole Velocity and Velocity Overshoot in Silicon Inversion Layers. *IEEE Electron Device Lett.* **1997**, *18* (2), 54−56.
(54) Caughey, D. M.; Thomas, R. E. Carrier Mobilities in Silicon Empircally Related to Doping and Field. *Proc. IEEE* **1967**, *55* (12), 2192−2193.
(55) Thornber, K. K. Relation of drift velocity to low-field mobility and high-field saturation velocity. *J. Appl. Phys.* **1980**, *51* (4), 2127−2136.
(56) Fang, F. F.; Fowler, A. B. Hot electron effects and saturation velocities in silicon inversion layers. *J. Appl. Phys.* **1970**, *41* (4), 1825−1831.

DOI: 10.1021/acs.nanolett.8b01692
Nano Lett. 2018, 18, 4516−4522

(57) Li, X.; Mullen, J. T.; Jin, Z.; Borysenko, K. M.; Buongiorno Nardelli, M.; Kim, K. W. Intrinsic electrical transport properties of monolayer silicene and MoS_2 from first principles. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2013**, *87* (11), 115418.
(58) Jin, Z.; Li, X.; Mullen, J. T.; Kim, K. W. Intrinsic transport properties of electrons and holes in monolayer transition-metal dichalcogenides. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2014**, *90* (4), 045422.
(59) Ferry, D. K. Electron velocity saturation and intervalley transfer in monolayer MoS_2. *Semicond. Sci. Technol.* **2016**, *31* (11), 11LT01.
(60) International Technology Roadmap for Semiconductors (ITRS). High Performance (HP) and Low Power (LP) PIDS Tables. URL: http://www.itrs2.net/itrs-reports.html.
(61) Islam, S.; Li, Z.; Dorgan, V. E.; Bae, M. H.; Pop, E. Role of joule heating on current saturation and transient behavior of graphene transistors. *IEEE Electron Device Lett.* **2013**, *34* (2), 166−168.
(62) Polonsky, S.; Jenkins, K. A. Time-Resolved Measurements of Self-Heating in SOI and Strained-Silicon MOSFETS Using Photon Emission Microscopy. *IEEE Electron Device Lett.* **2004**, *25* (4), 208−210.
(63) Takahashi, T.; Beppu, N.; Chen, K.; Oda, S.; Uchida, K. Self-heating effects and analog performance optimization of fin-type field-effect transistors. *Jpn. J. Appl. Phys.* **2013**, *52*, 04CC03.
(64) Takahashi, T.; Matsuki, T.; Shinada, T.; Inoue, Y.; Uchida, K. Comparison of self-heating effect (SHE) in short-channel bulk and ultra-thin BOX SOI MOSFETs: Impacts of doped well, ambient temperature, and SOI/BOX thicknesses on SHE. *IEEE Int. Electron Devices Meet.* **2013**, 184−187.
(65) Takahashi, T.; Matsuki, T.; Shinada, T.; Inoue, Y.; Uchida, K. Direct evaluation of self-heating effects in bulk and ultra-thin BOX SOI MOSFETs using four-terminal gate resistance technique. *IEEE J. Electron Devices Soc.* **2016**, *4* (5), 365−373.
(66) Qiao, J.; Kong, X.; Hu, Z.-X.; Yang, F.; Ji, W. High-mobility transport anisotropy and linear dichroism in few-layer black phosphorus. *Nat. Commun.* **2014**, *5*, 4475.
(67) Anwar, A. F. M.; Wu, S.; Webster, R. T. Temperature Dependent Transport Properties in GaN, $Al_xGa_{1-x}N$, and $In_xGa_{1-x}N$ Semiconductors. *IEEE Trans. Electron Devices* **2001**, *48* (3), 567−572.
(68) Matsuda, S.; Kikuchi, E.; Yamane, Y.; Okazaki, Y.; Yamazaki, S. Channel length dependence of field-effect mobility of c-axis-aligned crystalline In−Ga−Zn−O field-effect transistors. *Jpn. J. Appl. Phys.* **2015**, *54* (4), 041103.
(69) Polyakov, V. M.; Schwierz, F. Low-field electron mobility in wurtzite InN. *Appl. Phys. Lett.* **2006**, *88* (3), 032101.
(70) Rodilla, H.; González, T.; Pardo, D.; Mateos, J. High-mobility heterostructures based on InAs and InSb: A Monte Carlo study. *J. Appl. Phys.* **2009**, *105* (11), 113705.
(71) Roschke, M.; Schwierz, F. Electron mobility models for 4H, 6H, and 3C SiC. *IEEE Trans. Electron Devices* **2001**, *48* (7), 1442−1447.
(72) Modelli, A.; Manzini, S. High-field drift velocity of electrons in silicon inversion layers. *Solid-State Electron.* **1988**, *31* (1), 99−104.
(73) Huang, Y. L.; et al. Bandgap tunability at single-layer molybdenum disulphide grain boundaries. *Nat. Commun.* **2015**, *6*, 6298.
(74) Chen, X.; et al. Large-Velocity Saturation in Thin-Film Black Phosphorus Transistors. *ACS Nano* **2018**, *12* (5), 5003−5010.

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SUPPORTING INFORMATION

High-Field Transport and Velocity Saturation in Synthetic Monolayer MoS_2

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A. Long Channel Transfer Characteristic

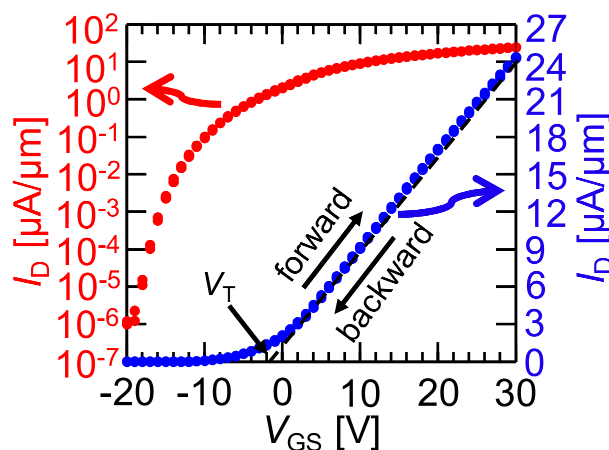


Figure S1. Forward and backward I_D-V_{GS} curves (linear and log scale) taken with direct current (DC) measurements at T_0 = 300 K ambient, in vacuum (~10^{-5} Torr), for the device depicted in Figure 1c (L = 4.9 μm, t_{ox} = 30 nm). We find $I_{MAX}/I_{MIN} \geq 10^7$ and negligible hysteresis (~150 mV on 30 nm SiO_2 thickness). The field effect mobility $\mu_{FE} \equiv L(\partial I_D/\partial V_{GS})/(WC_{ox}V_{DS}) \approx 33.7$ cm^2/V/s extracted from these data, very close to μ_{eff}, indicates that R_C does not contribute much to R_{TOT} for these devices.[1]

B. Transfer and Output Characteristics for a 72 nm Device

We analyze data of ordinary *I*-*V* measurements on the L = 72 nm device from the TLM structure in Figure 2, at both low- and high-field regimes. Figure S2a shows the forward-backward I_D-V_{GS} sweeps at V_{DS} = 0.1 V (F < 0.3 V/μm when accounting for R_C). In addition to retaining very small hysteresis, we measure $I_{MAX}/I_{MIN} > 10^8$, which attests to the robustness of 2D materials against short channel effects. In Figure S2b, we perform forward-backward I_D-V_{DS} sweeps and fit these curves with our 2D transistor model.[2,3] Despite this device being ~80% dominated by R_C at T_0 = 300 K, it experiences lateral fields in excess of 7 V/μm at high V_{DS} and even shows signs of negative differential conductance (NDC), indicative of significant self-heating in the channel. This is also captured in the curve fits by our compact model, which return values of R_C = 1.4 to 5.5 kΩ·μm with μ_{eff} = 35.0 cm^2/V/s at moderate n, well in agreement with our experimental observations. Additionally, the model gives v_{sat} up to 1.5×10^6 cm/s for low V_{GS} and falling to 0.4×10^6 cm/s for high V_{GS}, these values being limited by the significant device self-heating.

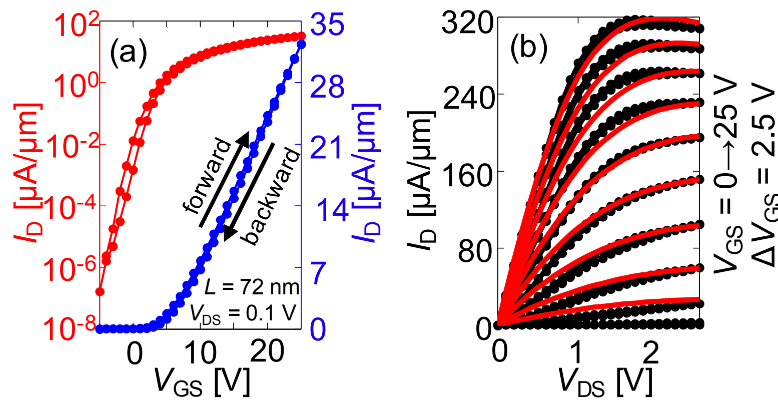


Figure S2. (a) Linear- and log-scale I_D-V_{GS} curves of the L = 72 nm device from the TLM structure (V_{DS} = 0.1 V). Note that this device maintains an extremely high I_{MAX}/I_{MIN} ratio (>10^8) despite how short it is. (b) High-field measured I_D-V_{DS} curves of the L = 72 nm device at T_0 = 300 K ambient (black symbols) along with compact model fits (red lines). V_{GS} = 0 to 25 V with ΔV_{GS} = 2.5 V. Both the model and the data suggest that at extremely high fields, NDC occurs due to a combination of self-heating and velocity saturation.

C. Specific Contact Resistivity and Current Transfer Length

Using the transmission line model,[4,5] we estimate the specific contact resistivity (ρ_C) from

$$R_C = \frac{\rho_C}{L_T}\coth\left(\frac{L_C}{L_T}\right) \approx \sqrt{\rho_C R_{SH}}\,, \quad \text{(Eq. S1)}$$

where L_C = 1 μm is the length of the contacts and L_T is the current transfer length. We note that the approximation in Eq. S1 is only valid when $L_T < L_C$, in which case $\coth(L_C/L_T) \approx 1$, and we can rearrange to give

$$L_T \approx \sqrt{\frac{\rho_C}{R_{SH}}} \approx \frac{R_C}{R_{SH}} \quad \text{(Eq. S2)}$$

whereby we extract $L_T \approx 100$ nm $\ll L_C$ at 300 K, justifying our use of the approximation.

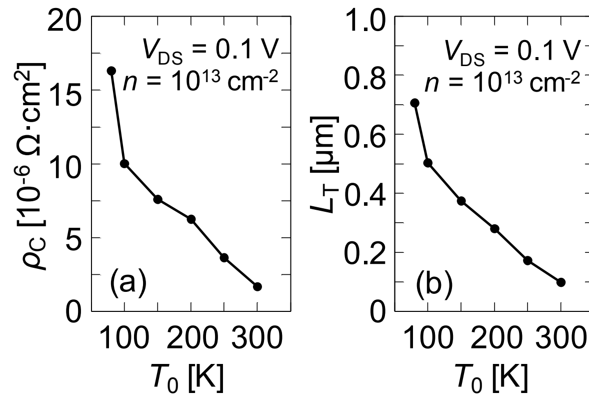


Figure S3. (a) Specific contact resistivity ρ_C vs. ambient T_0, showing a minimum of 1.7×10^{-6} Ω·cm^2 at 300 K and $n = 10^{13}$ cm^{-2}. ρ_C falls to 1.3×10^{-6} Ω·cm^2 at $n = 1.3 \times 10^{13}$ cm^{-2}. (b) Transfer length L_T vs. T_0, with a minimum of ~98 nm at 300 K.

D. Contribution from Device Contacts

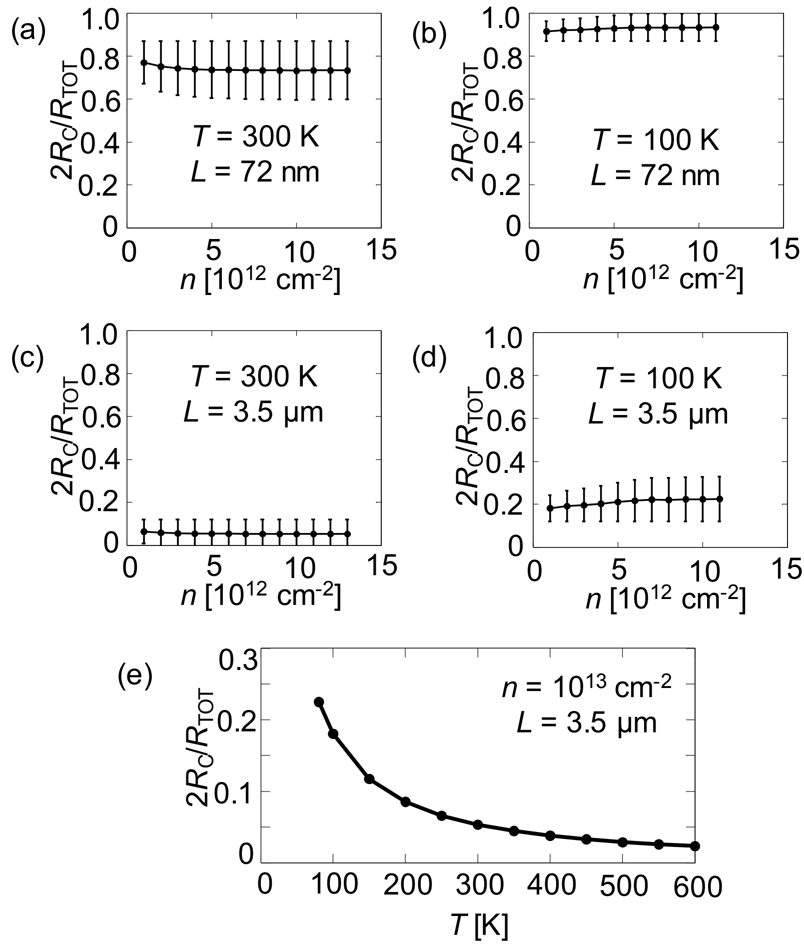


Figure S4. Calculations of total contact resistance as a fraction of the total device resistance ($2R_C/R_{TOT}$) vs. n, corresponding to μ_{eff} and R_C in Figure 2 of the main text. Error bars reflect the same 95% confidence intervals. (a) The shortest device with L = 72 nm at ambient T_0 = 300 K. (b) L = 72 nm, T_0 = 100 K. (c) A long channel L = 3.5 μm at T_0 = 300 K. (d) L = 3.5 μm, T_0 = 100 K. (e) $2R_C/R_{TOT}$ vs. device T for L = 3.5 μm and $n = 10^{13}$ cm^{-2}. Note that $2R_C/R_{TOT}$ is always smaller at higher T_0 due to the decreased μ_{eff}, and so even for low T_0, devices biased at high fields where the device $T \geq 300$ K will still have $2R_C/R_{TOT} \leq 0.05$.

E. Thermal Resistance Modeling

To account for self-heating and power dissipation in these devices, the heat diffusion equation was utilized in the form of Eq. S3 for steady-state conditions:

$$\frac{\partial^2 T}{\partial x^2} + \frac{(I_D/W)F(x)}{k_{MoS_2} t_{MoS_2}} - \frac{\left(T(x) - T_0\right)}{R_{th} k_{MoS_2} t_{MoS_2}} = 0 \quad \text{(Eq. S3)}$$

In Eq. S3, k_{MoS2} = 34.5 W/m/K is the in-plane thermal conductivity of 1L MoS_2,[6] and t_{MoS2} = 6.15 Å is the thickness of the 1L. x is the variable of distance along the channel from source to drain (see Figure S5), and $F(x)$ is the field along the channel, which in our case is approximately constant. R_{th} is the total thermal resistance per unit area for a long-channel device ($L \gg L_H$, the thermal healing length, see Eq. S5) as shown in Figure 3a, a simple sum of the contributions from: 1) the MoS_2-SiO_2 thermal boundary resistance (TBR = 1/TBC, where the measured[7,8] temperature-dependent TBC ≈ $14\times(T/[300\text{ K}])^{0.65}$ $MW/m^2/K$ and TBC is the thermal boundary conductance); 2) the SiO_2 thermal resistance, $R_{SiO2} = t_{ox}/k_{ox}$ (where t_{ox} = 100 nm and $k_{ox} \approx 0.52\times\ln([T+T_0]/2) - 1.6$ W/m/K are the thickness and average temperature-dependent thermal conductivity of the SiO_2 substrate[9,10]); 3) the SiO_2-Si TBR (estimated[11] at $\sim 2\times10^{-9}$ m^2K/W); and 4) the thermal spreading resistance of the underlying Si substrate, given by[12] $R_{Si} = (A)^{1/2}(2k_{Si})^{-1}$ (where $A = LW$ is the channel area and $k_{Si} \approx 3\times10^4/T_0$ W/m/K is the thermal conductivity of the semi-infinite highly-doped Si substrate[8,13,14]).

By assuming boundary conditions of perfect heat sinks at the source, drain, and bottom silicon substrate [$T(\pm L/2) = T_0$], the temperature distribution can be easily solved and simplified to

$$T(x) = T_0 + (I_D/W)FR_{th}\left(1 - \frac{\cosh(x/L_H)}{\cosh(L/(2L_H))}\right). \quad \text{(Eq. S4)}$$

For additional simplification, we take the spatially averaged value of this solution to be indicative of the temperature of the device as a whole, which results in the closed-form expression given in Eq. 4 of the main text. Temperature calculations and temperature-dependent values for TBC and k_{ox} are performed iteratively until values for T converge to within 1 K. The thermal healing length, L_H, is simply the square root of the denominator of the last term in Eq. S3:

$$L_H = \sqrt{R_{th} k_{MoS_2} t_{MoS_2}}\ . \quad \text{(Eq. S5)}$$

For our devices, $L_H \sim 70$ nm. We note that since $L \gg L_H$ (in our long channel devices) we could have assumed that $T \approx T_0 + (I_D/W)FR_{th}$, and our calculations for T would not have changed by more than a few percent, as shown in Figure S5.

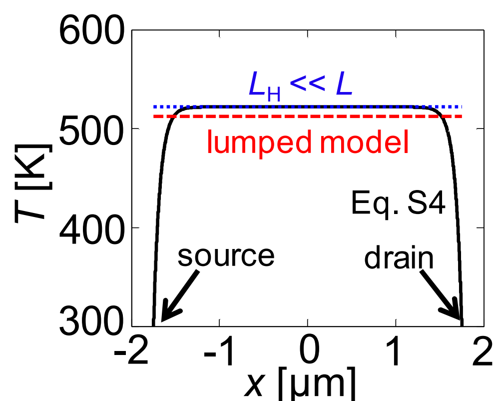


Figure S5. Calculated T vs. x along the channel of a L = 3.5 μm device at T_0 = 300 K (for simplicity, t_{ox} = 100 nm, W = 5 μm, TBR ≈ 7×10^{-8} m^2K/W, k_{ox} = 1 W/m/K, and k_{Si} = 95 W/m/K). In this example, F = 5 V/μm and I_D/W = 200 μA/μm. The solid black line follows Eq. S4; the dashed red line is given by Eq. 4 in the main text; and the dotted blue line is given by the simple model $T \approx T_0 + (I_D/W)FR_{th}$.

F. Device Breakdown at High Lateral Fields

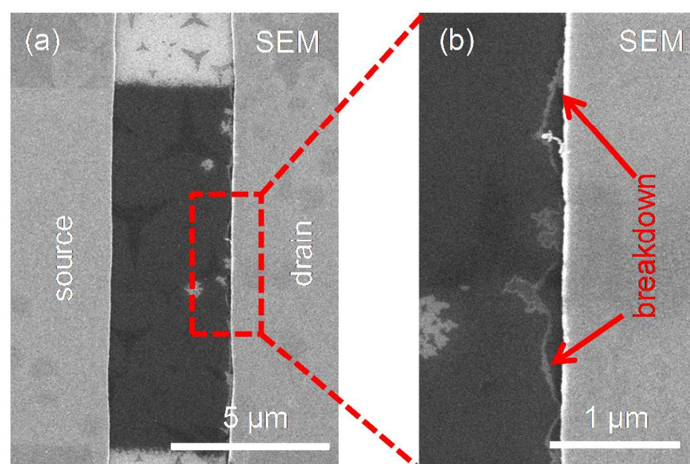
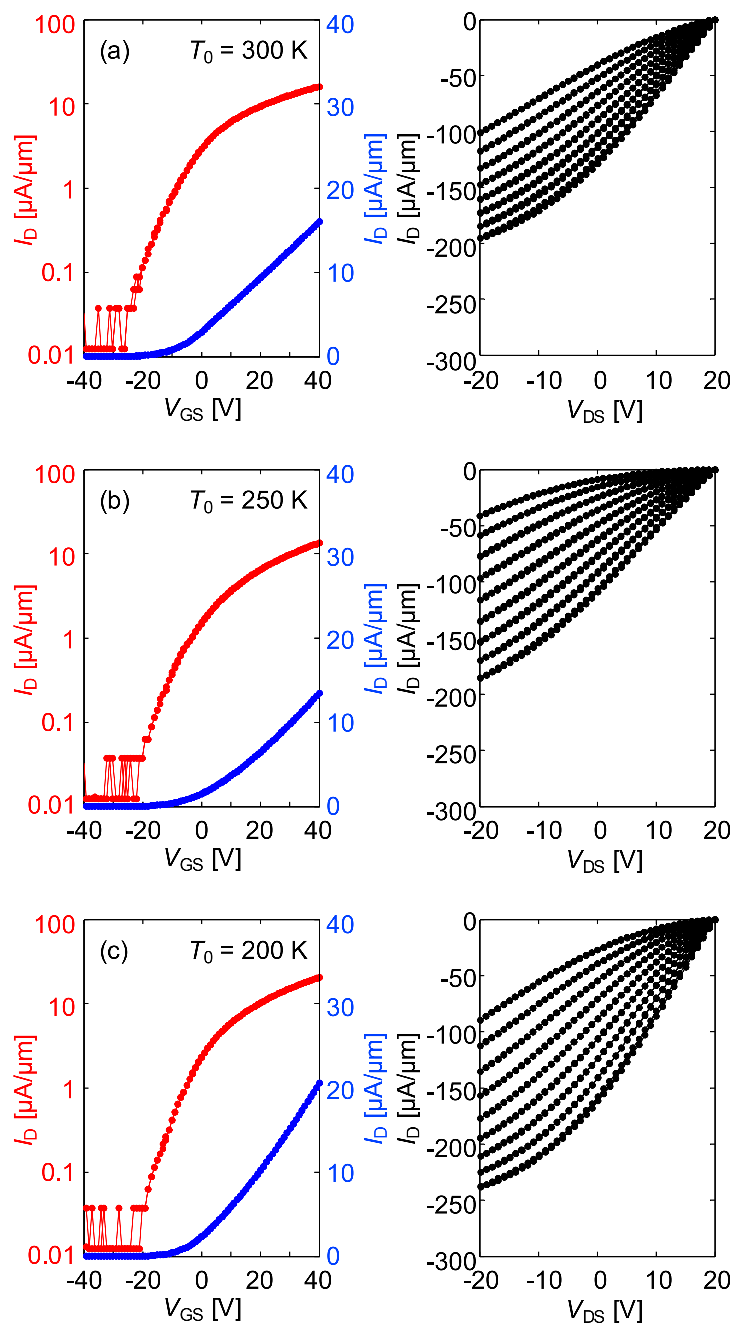


Figure S6. Top view SEM images of a device that failed during testing. The MoS_2 appears to break down due to localized self-heating at lateral fields exceeding 6 V/μm, and the corresponding voltages put at most 0.8 V/nm (vertically) across the SiO_2 gate dielectric. Destruction of the MoS_2 channel can clearly be seen near the drain contact.

G. Transfer and Output Characteristics



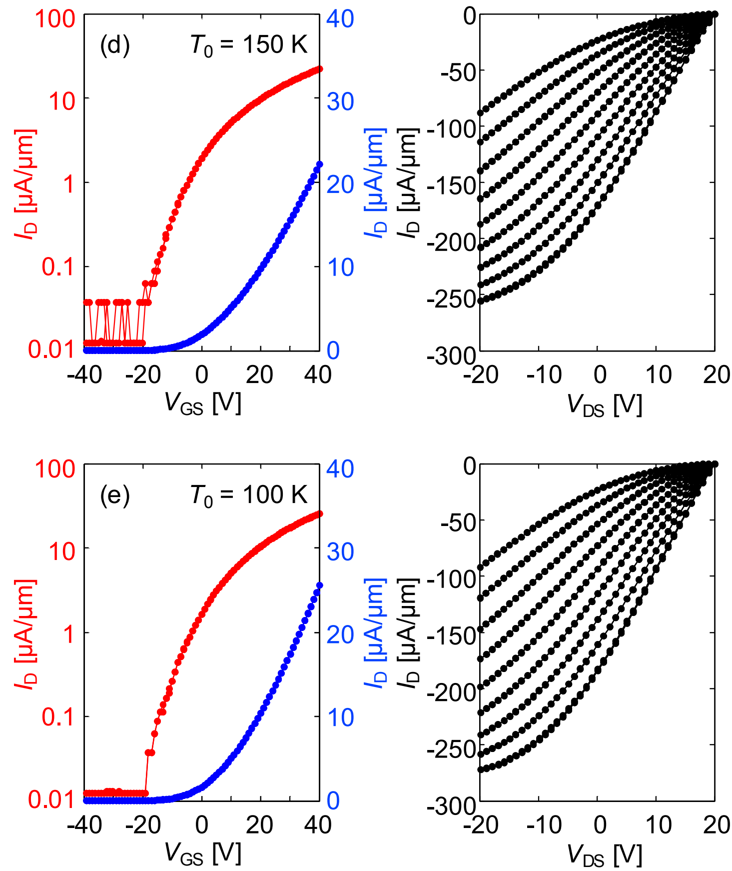


Figure S7. Forward and backward I_D-V_{GS} and negative I_D-V_{DS} data taken with pulsed measurements (τ_{pulse} = 100 µs) at ambient temperatures of (a) 300 K, (b) 250 K, (c), 200 K, (d) 150 K, and (e) 100 K. t_{ox} = 100 nm, L = 3.7 µm. For the I_D-V_{GS} sweeps, V_{DS} = 1.0 V; for the I_D-V_{DS} sweeps, V_{GS} = -10 → 30 V with ΔV_{GS} = 5 V. Note that the threshold voltage tends to become more positive at lower temperatures due to adsorbates settling on the channel. In general, there are more I_D-V_{DS} sweeps than there are v_d-F curves in Figures 4 and S9 because we only analyze the data taken with $V_{GS} > V_T$ such that the linear approximation for Q_{eff} is accurate (uncertainty is discussed in Supporting Information J).

H. Clarification of Mobility Definitions

We wish to further elucidate the differences between the three definitions of mobility explored in the main text: the effective mobility, μ_{eff}; the field-effect mobility, μ_{FE}; and the low-field mobility, μ_{LF}. Figure S8 shows a comparison of these extracted mobilities for our short- and long-channel devices.

The first, μ_{eff}, is strictly a channel parameter with effects from the contacts removed.[15,16] Although the TLM extraction overestimates the value of μ_{eff} at low V_{OV} (= $V_{GS} - V_T$) due to underestimation of n from the linear threshold extrapolation, when $n > 4\times10^{12}$ cm^{-2}, μ_{eff} approaches a lowest, constant value (see Figure 2d). We take this lowest number to be the true μ_{eff} of the material for all n, and this is the type of mobility best suited for use in compact models and other simulations.

The second, μ_{FE}, is extracted from two-terminal I_D-V_{GS} measurements for low V_{DS}. This necessarily means that μ_{FE} is a function of V_{GS} (and in most cases, also R_C), but would ideally approach μ_{eff} for high n in the limit of negligible contact resistance. This is what we observe for long-channel devices (Figure S8b), but not for short-channel devices (Figure S8a) which are dominated by contact resistance. We note that μ_{FE} is not the appropriate device parameter for our analysis, since it must be extracted at low lateral electric fields for the approximation to be valid, and here we are interested in high-field transport.

The last, μ_{LF}, is extracted from v_d vs. F data as explained in the main text. Similar to μ_{eff}, this parameter is overestimated for low n, but approaches a lowest value as n increases, ideally congruent with both μ_{eff} and μ_{FE} (Figure S8c). For any given bias point, however, it is only a fit parameter and is not necessarily indicative of the true mobility (μ_{eff}). Note that the fits for v_{sat}, on the other hand, are all done at high fields and high gate overdrive ($V_{DS} \ll 0$, $V_{OV} \gg 0$), which for our device geometry also corresponds to relatively high values of n, where the linear threshold extrapolation method is valid. Thus we can take our extractions for v_{sat} to be indicative of real carrier transport, even if the values for μ_{LF} might not be.

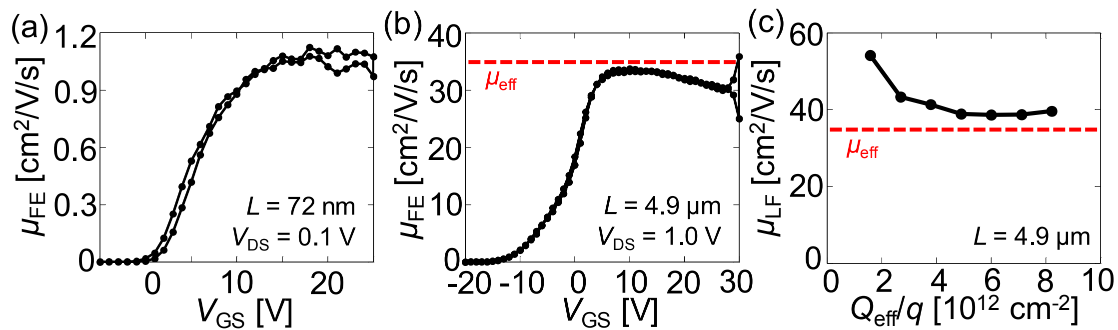


Figure S8. μ_{FE} vs. V_{GS} as extracted from: (a) I_D-V_{GS} sweeps of the 72 nm device in Figure S2; (b) 4.9 µm device in Figure S1. Note how for the long-channel device, $2R_C/R_{TOT} \ll 1$, and μ_{FE} approaches μ_{eff}; yet for the short-channel device, $2R_C/R_{TOT} \approx 0.8$, and μ_{FE} severely underestimates μ_{eff}. (c) μ_{LF} vs. $Q_{eff}/q = \langle n \rangle$, showing how the slopes of the low-field v_d vs. F curves exhibit the same behavior as μ_{eff}, approaching a minimum value for high $\langle n \rangle$.

I. Drift Velocity Data for Additional Temperatures

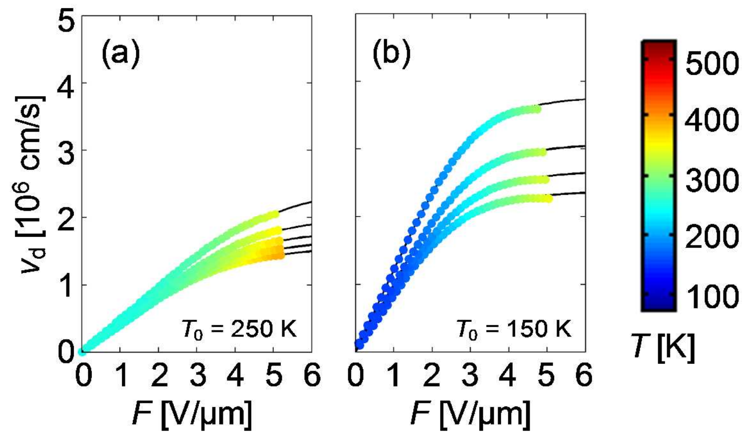


Figure S9. Extracted v_d vs. F for the same device in Figures 3 and 4 at (a) T_0 = 250 K and (b) 150 K ambient. The color bar and the colored symbols represent the estimated device temperature at each bias point. Black lines are fits using the Caughey-Thomas model, Eq. 5 in the main text.

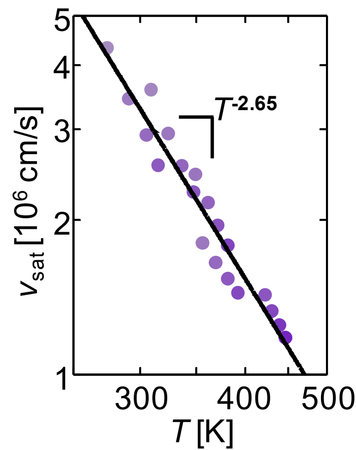


Figure S10. Data for measured v_{sat} vs. device T taken from Figures 4 and S9, showing a steep roll-off of $T^{-2.65}$. Note that due to the average carrier density in the channel changing as the drain is swept to more negative voltages, n also varies with T. More detailed calculations will need to be performed by, e.g., Monte Carlo simulations to decouple the effects of T, n, and differing conduction valley populations on v_{sat}.

J. Measurement and Modeling Uncertainty

To calculate uncertainty in v_{sat} and T, we return to our models for v_d and T. In the case of v_d, the largest sources of error come from the linear model for Q_{eff}, by way of both C_{ox} and V_T. Due to our use of a highly doped Si gate, C_{ox} changes slightly (≤ 6%) with V_{GS} as the semiconductor moves from inversion to depletion to accumulation; furthermore, there is a small amount of uncertainty associated with fitting V_T linearly from the I_D-V_{GS} data as shown in Figures S1 and S7. Due to the nature of these error terms, I_D-V_D sweeps at lower V_{GS} (corresponding to the uppermost curves in Figures 4 and S9) will have the largest uncertainty; this notwithstanding, we calculate the largest uncertainty in our estimates of v_{sat} to be ~13% (see Figure 4c). [The smallest uncertainty in v_{sat} is 2%, and the uncertainty in the measurement for v_{sat} at 291 K is ~10%, or $v_{sat} = (3.4 \pm 0.4) \times 10^6$ cm/s.]

For calculating device T, the largest source of uncertainty comes from our previous measurements[14] of the MoS_2-SiO_2 TBC, which is 14 ± 4 $MW/m^2/K$ at 300 K. By propagating the uncertainty of 4 $MW/m^2/K$ through our thermal model, we arrive at a maximum uncertainty in T of ~20 K.

K. Comparison with Saturation Velocity in Other Semiconductors and Graphene

	Material	Band Gap (eV)	Electron v_{sat} ($\times 10^7$ cm/s)	Hole v_{sat} ($\times 10^7$ cm/s)
Bulk	Si	1.12	1.02	0.72
Bulk	Ge	0.66	0.70	0.63
Bulk	GaAs	1.42	0.72	0.9
Bulk	InAs	0.35	0.9	0.5
Bulk	GaP	2.26	0.88	0.5
Bulk	InP	1.34	0.68	0.7
Bulk	GaN	3.2	1.4	-
Bulk	AlN	6.2	1.6	-
Bulk	InN	1.97	1.5 – 2.5	-
Bulk	InSb	0.18	~1	-
	SiC	2.36 – 3.33	2	-
	IGZO	2.7 – 3.5	0.39	-
	BP	0.3	-	0.55
<1 nm	CNTs	variable	3 – 5	-
<1 nm	Graphene	0	2 – 6	-
<1 nm	MoS_2	~2.3	0.34	-

Table S1. Comparison of saturation velocity values for electrons and holes in several materials at room temperature. This is the table version of Figure 5 from the main text. While 1L MoS_2 has the lowest electron v_{sat} of all materials on the table, it is also the only sub-nanometer thin semiconductor listed. Values are adapted from Refs. 17–27.

L. Electron Temperature

We note that for all our measurements, the electron temperature (T_e) is reasonably approximated by the lattice temperature T during device operation and self-heating. As shown in Ref. 28, the average velocity of electrons populating two valleys is given by

$$v = \frac{\mu_1 n_1 + \mu_2 n_2}{n_1 + n_2} \varepsilon \approx \mu\varepsilon \rightarrow v_{sat} , \qquad \text{(Eq. S6)}$$

with μ_i and n_i representing the effective mobility and carrier density in each valley, and ε being the lateral electric field. In the approximation that $\mu_1 \approx \mu_2$ (more valid here for 1L MoS_2 as opposed to high-mobility III-V materials, where $\mu_1 \gg \mu_2$), the equation collapses to the familiar form $v \approx \mu\varepsilon \rightarrow v_{sat}$. Furthermore, the electron temperature is determined through the energy relaxation time τ_e as:[28,29]

$$qv\varepsilon = \frac{k_B (T_e - T)}{\tau_e} . \qquad \text{(Eq. S7)}$$

Combining these equations with the relation $\mu = q\tau_e/m^*$ and replacing $\mu\varepsilon$ with v_{sat} in the limit of velocity saturation yields

$$T_e = T + \frac{m^*}{k_B} v\mu\varepsilon \rightarrow T + \frac{m^*}{k_B} v_{sat}^2 . \qquad \text{(Eq. S8)}$$

In the case of electrons in 1L MoS_2 with $v \sim 3.4\times10^6$ cm/s, the latter term is $\Delta T \approx 34$ K (at $T = 300$ K). At higher T, ΔT will be even smaller due to increased scattering events lowering v_{sat} further (e.g. $\Delta T = 5$ K at $T = 450$ K, when $v_{sat} = 1.3\times10^6$ cm/s).

Supporting Information References

(1) Smithe, K. K. H.; Suryavanshi, S. V.; Muñoz Rojo, M.; Tedjarati, A. D.; Pop, E. Low Variability in Synthetic Monolayer MoS_2 Devices. *ACS Nano* **2017**, *11* (8), 8456–8463. DOI: 10.1021/acsnano.7b04100.

(2) Suryavanshi, S. V.; Pop, E. S2DS: Physics-based compact model for circuit simulation of two-dimensional semiconductor devices including non-idealities. *J. Appl. Phys.* **2016**, *120* (22), 224503. DOI: 10.1063/1.4971404.

(3) Suryavanshi, S. V.; Pop, E. Stanford 2D Semiconductor (S2DS). URL: <https://nanohub.org/publications/18> DOI: 10.4231/D3ZC7RV9X.

(4) Berger, H. H. Models for contacts to planar devices. *Microelectron. Reliab.* **1972**, *15* (2), 145–158. DOI: 10.1016/0026-2714(72)90162-X.

(5) Schroder, D. K. *Semiconductor Material and Device Characterization: Third Edition*, 3rd ed.; John Wiley & Sons, 2005.

(6) Yan, R; Simpson, J. R.; Bertolazzi, S.; Brivio, J.; Watson, M.; Wu, X.; Kis, A.; Luo, T.; Walker, A. R. H.; Xing, H. G. Thermal Conductivity of Monolayer Molybdenum Disulfide Obtained from Temperature-Dependent Raman Spectroscopy. *ACS Nano* **2014**, *8* (1), 986–993. DOI: 10.1021/nn405826k.

(7) Yalon, E. et al. Energy Dissipation in Monolayer MoS_2 Electronics. *Nano Lett.* **2017**, *17* (6), 3429–3433. DOI: 10.1021/acs.nanolett.7b00252.

(8) Yalon, E. et al. Temperature-Dependent Thermal Boundary Conductance of Monolayer MoS_2 by Raman Thermometry. *ACS Appl. Mater. Interfaces* **2017**, *9* (49), 43013–43020. DOI: 10.1021/acsami.7b11641.

(9) Yamane, T.; Nagai, N.; Katayama, S.; Todoki, M. Measurement of thermal conductivity of silicon dioxide thin films using a 3 omega method. *J. Appl. Phys.* **2002**, *91* (12), 9772–9776. DOI: 10.1063/1.1481958.

(10) Andersson, S.; Dzhavadov, L. Thermal conductivity and heat capacity of amorphous SiO_2: pressure and volume dependence. *J. Phys. Condens. Matter* **1992**, *4*, 6209–6216. DOI: 10.1088/0953-8984/4/29/005.

(11) Chien, H. C.; Yao, D. J.; Huang, M. J.; Chang, T. Y. Thermal conductivity measurement and interface thermal resistance estimation using SiO_2 thin film. *Rev. Sci. Instrum.* **2008**, *79* (5), 054902. DOI: 10.1063/1.2927253.

(12) Yovanovich, M. M.; Culham, J. R.; Teertstra, P. Analytical Modeling of Spreading Resistance in Flux Tubes, Half Spaces, and Compound Disks. *IEEE Trans. Compon. Packaging. Manuf. Technol.* **1998**, *21* (1), 168–176. DOI: 10.1109/95.679046.

(13) Asheghi, M.; Kurabayashi, K.; Kasnavi, R.; Goodson, K. E. Thermal conduction in doped single-crystal silicon films. *J. Appl. Phys.* **2002**, *91* (8), 5079–5088. DOI: 10.1063/1.1458057.

(14) Asheghi, M.; Touzelbaev, M. N.; Goodson, K. E.; Leung, Y. K.; Wong, S. S. Temperature-Dependent Thermal Conductivity of Single-Crystal Silicon Layers in SOI Substrates. *J. Heat Transfer* **1998**, *120*, 30–36. DOI: 10.1115/1.2830059.

(15) Smithe, K. K. H.; English, C. D.; Suryavanshi, S. V; Pop, E. Intrinsic electrical transport and performance projections of synthetic monolayer MoS_2 devices. *2D Mater.* **2017**, *4*, 011009. DOI: 10.1088/2053-1583/4/1/011009.

(16) English, C. D.; Shine, G.; Dorgan, V. E.; Saraswat, K. C.; Pop, E. Improved Contacts to MoS_2 Field-Effect Transistors by Ultra-High Vacuum Metal Deposition. *Nano Lett.* **2016**, *16* (6), 3824–3830. DOI: 10.1021/acs.nanolett.6b01309.

(17) Quay, R.; Moglestue, C.; Palankovski, V.; Selberherr, S. A temperature dependent model for the saturation velocity in semiconductor materials. *Mater. Sci. Semicond. Process.* **2000**, *3* (1–2), 149–155. DOI: 10.1016/S1369-8001(00)00015-9.

(18) Anwar, A. F. M.; Wu, S.; Webster, R. T. Temperature Dependent Transport Properties in GaN, $Al_xGa_{1-x}N$, and $In_xGa_{1-x}N$ Semiconductors. *IEEE Trans. Electron Devices* **2001**, *48* (3), 567–572. DOI: 10.1117/12.2084164.

(19) Yamoah, M. A.; Yang, W.; Pop, E.; Goldhaber-Gordon, D. High-Velocity Saturation in Graphene Encapsulated by Hexagonal Boron Nitride. *ACS Nano* **2017**, *11* (10), 9914–9919. DOI: 10.1021/acsnano.7b03878.

(20) Zhu, W.; Park, S.; Yogeesh, M. N.; McNicholas, K. M.; Bank, S. R.; Akinwande, D. Black Phosphorus Flexible Thin Film Transistors at Gighertz Frequencies. *Nano Lett.* **2016**, *16* (4), 2301–2306. DOI: 10.1021/acs.nanolett.5b04768.

(21) Matsuda, S.; Kikuchi, E.; Yamane, Y.; Okazaki, Y.; Yamazaki, S. Channel length dependence of field-effect mobility of c-axis-aligned crystalline In–Ga–Zn–O field-effect transistors. *Jpn. J. Appl. Phys.* **2015**, *54* (4), 041103. DOI: 10.7567/JJAP.54.041103.

(22) Dorgan, V. E.; Bae, M. H.; Pop, E. Mobility and saturation velocity in graphene on SiO_2. *Appl. Phys. Lett.* **2010**, *97* (8), 82112. DOI: 10.1063/1.3483130.

(23) Perebeinos, V.; Tersoff, J.; Avouris, P. Electron-phonon interaction and transport in semiconducting carbon nanotubes. *Phys. Rev. Lett.* **2005**, *94* (8), 86802. DOI: 10.1103/PhysRevLett.94.086802.

(24) Verma, A.; Kauser, M. Z.; Ruden, P. P. Ensemble Monte Carlo transport simulations for semiconducting carbon nanotubes. *J. Appl. Phys.* **2005**, *97* (11), 114319. DOI: 10.1063/1.1925763.

(25) Polyakov, V. M.; Schwierz, F. Low-field electron mobility in wurtzite InN. *Appl. Phys. Lett.* **2006**, *88* (3), 032101. DOI: 10.1063/1.2166195.

(26) Rodilla, H.; González, T.; Pardo, D.; Mateos, J. High-mobility heterostructures based on InAs and InSb: A Monte Carlo study. *J. Appl. Phys.* **2009**, *105* (11), 113705. DOI: 10.1063/1.3132863.

(27) Roschke, M.; Schwierz, F. Electron mobility models for 4H, 6H, and 3C SiC. *IEEE Trans. Electron Devices* **2001**, *48* (7), 1442–1447.

(28) Sze, S. M.; Ng, K. K. *Physics of Semiconductor Devices*, 3rd ed.; John Wiley & Sons: Hoboken, NJ, 2007.

(29) Jacoboni, C.; Canali, C.; Ottaviani, G.; Alberigi Quaranta, A. A review of some charge transport properties of silicon. *Solid State Electron.* **1977**, *20*, 77–89. DOI: 10.1016/0038-1101(77)90054-5.