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Article

Spatially-Resolved Thermometry of Filamentary Nanoscale Hot Spots in TiO_2 Resistive Random Access Memories to Address Device Variability

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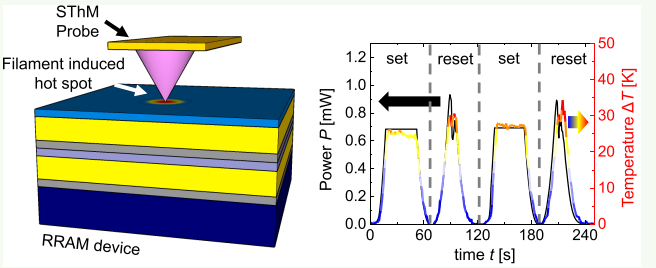
ABSTRACT: Resistive random access memories (RRAM), based on the formation and rupture of conductive nanoscale filaments, have attracted increased attention for application in neuromorphic and in-memory computing. However, this technology is, in part, limited by its variability, which originates from the stochastic formation and extreme heating of its nanoscale filaments. In this study, we used scanning thermal microscopy (SThM) to assess the effect of filament-induced heat spreading on the surface of metal oxide RRAMs with different device designs. We evaluate the variability of TiO_2 RRAM devices with area sizes of 2 × 2 and 5 × 5 μm^2. Electrical characterization shows that the variability indicated by the standard deviation of the forming voltage is ∼2 times larger for 5 × 5 μm^2 devices than for the 2 × 2 μm^2 ones. Further knowledge on the reason for this variability is gained through the SThM thermal maps. These maps show that for 2 × 2 μm^2 devices the formation of one filament, i.e., hot spot at the device surface, happens reliably at the same location, while the filament location varies for the 5 × 5 μm^2 devices. The thermal information, combined with the electrical, interfacial, and geometric characteristics of the device, provides additional insights into the operation and variability of RRAMs. This work suggests thermal engineering and characterization routes to optimize the efficiency and reliability of these devices.



KEYWORDS: *resistive random access memory, scanning thermal microscopy, device variability, conductive filaments, heat dissipation in electronics*

INTRODUCTION

Resistive switching devices are considered promising for nonvolatile memory and neuromorphic computing.[1−3] A type of such devices is resistive random access memory (RRAM), which tends to feature low power consumption, high speed, and simple device configuration.[4] RRAM devices typically consist of an oxide insulator sandwiched in a two-terminal metal−insulator−metal layered structure.[5] The principle of operation of an RRAM device is based on the formation (set) and breaking (reset) of a conductive filament in the oxide layer.[6,7] In the recent past, resistive switching has been investigated in a wide variety of metal oxides, like HfO_2,[8−10] Ta_2O_5,[11,12] or TiO_2.[13−15] Some of the major challenges associated with these devices are related to a lack of reliability in device operation and storage mechanisms that results in high variability of their electrical performance.[16,17] Understanding the underlying fundamental operation, like filament size,[18] position,[19] current density,[20] and heating,[21] is therefore essential for the evaluation, design, and optimization of RRAMs. Different studies have estimated that the diameter of conductive filaments could be below 10 nm.[22,23] Through these confined conductive regions flow large currents that can lead to high power densities >10^{13} W/cm^3.[9] Deshmukh et al.[9] determined that these high power densities can cause extremely high temperature rise, over 1000 K in HfO_2-based RRAM filaments. These elevated temperatures not only reduce the endurance and performance of devices themselves but also threaten the operation of the electronics in the vicinity because of potential thermal crosstalk. Within this context, thermal management is becoming essential in memory circuits, like those for neuromorphic computing, where controlling temperature variation is needed for efficient and stable data processing.[24] Therefore, further observations and analyses of filament-induced hot spots in RRAMs are relevant for achieving optimum, reliable, and efficient performance.

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The need to improve the reliability of RRAM devices has been a topic of ample discussion.[25−27] Park et al.[26] characterized the existence of multiple conductive paths in Ta_2O_{5-x}/TaO_{2-x} RRAM devices by means of transmission electron microscopy (TEM). However, on the basis of these measurements, no conclusions can be drawn on the heat distribution associated with these filament-based devices during operation. Baeumer et al.[27] observed the change of the position of the active conductive filament as a consequence of $I-V$ cycling in $SrTiO_3$ RRAM devices using photoelectron emission microscopy (PEEM). The filament is localized through the analysis of the photoemission threshold difference across the device area. PEEM is limited by its depth of field of a few nanometers and by the lack of information toward the current or heat distribution in steady state. Because of the depth limitation, the PEEM studies must also be performed on special device structures, for example, by using photoelectron-transparent graphene electrodes.[27]

Scanning thermal microscopy (SThM)[28−34] is a scanning probe microscopy (SPM)-based technique that offers new possibilities to explore the operation of electronic devices. It uses a special temperature sensitive probe with high precision (<1 K) that enables the characterization of thermal phenomena with nanoscale spatial resolution. SThM has been applied to study the energy dissipation of different devices, like memories,[9,35,36] and phase change materials (PCM).[30,37] Importantly, the combination of high thermal and spatial resolution makes SThM an ideal tool for analyzing heating in filament-based RRAM devices.[34,38] As an example, Datye et al.[35] employed SThM for surface mapping of the hot spots due to conductive bridges formed in $MoTe_2$ memory devices. Recently, Deshmukh et al.[9] imaged the spatial extent and temperature of the filament operation in HfO_x-based RRAMs, assessing the effect of heat spreading on memory operation. Similarly, Nandi et al.[36] investigated the temperature distribution in NbO_x-based RRAM devices. Additional studies on the fundamental thermal behavior of filamentary memories are essential for gaining further insight toward how the switching mechanisms are influenced by geometry, materials, and contacts. This will enable new thermal engineering routes for more efficient and reliable RRAMs.

In this work, we used SThM to characterize the localized filamentary heating in TiO_2-based cross-point RRAM devices and correlate these observations with device performance and reliability. While previous reports using SThM analysis on memories[9,35,36] focus on the fundamental assessment of filament-induced heat spreading, the evaluation of the memory switching variability by combining electrical and thermal data has not previously been carried out. The analysis of the thermal maps obtained by SThM is capable of providing further insights into the cause of device switching variability. We chose TiO_2 as the switching material for the RRAM, given its widespread use for these devices and because it is reliable and is easy to grow, which makes it a good candidate for the characterization of different areas.[39,40] We observed significant differences in the thermal behavior of devices with two different cross-point areas, i.e., 2×2 and 5×5 μm^2, in terms of their $I-V$ switching variability and the stability of the conductive filament. SThM provides valuable information to evaluate sources of variation and to suggest routes for optimizing device performance and reducing variability.

EXPERIMENTAL RESULTS

Fabrication of the RRAM Device Structure. Figure 1 shows a cross-sectional schematic of the investigated RRAM structure based on a thin TiO_2/Ti layer (from bottom to top) sandwiched between two Au electrodes. To fabricate this RRAM, we first deposited a thin 10 nm Ti layer for adhesion on top of a Si/SiO_2 (300 nm) substrate. Then, we used e-beam evaporation to deposit the bottom Au electrodes with a thickness of 30 nm. The switching material consists of a TiO_2/Ti bilayer where each layer has a thickness of 10 nm, deposited by e-beam evaporation (Ti) and atomic layer deposition (TiO_2). A 30 nm thick top Au electrode was evaporated with e-beam. Finally, we covered the whole structure with a 10 nm thick Al_2O_3 capping layer grown by atomic layer deposition (ALD) to electrically insulate the sample. The top view of the device consists of a cross-point structure with contact pad sizes of 100×100 μm^2. For the purpose of this study, we fabricated devices with two different cross-point areas: 2×2 and 5×5 μm^2 (see Supporting Information Section S1).

Characterization of the Current−Voltage Characteristics. The filament formation process in metal oxide RRAMs is achieved when applying a forming voltage (up to 3 V) to the device, which is associated with the creation of a conductive path that results from the connection of oxygen vacancies.[1] Forming is accompanied by a sharp decrease of the device resistance from native oxide resistance to a low resistive state (LRS). The filament can be (partially or completely) broken when a sufficiently high reverse bias (-1.5 V $< V <$ -1 V) is applied to the device (reset process), causing an increased resistance also referred to as high resistive state (HRS). The device can switch to LRS on applying a voltage, lower than during forming (0.5 V $< V <$ 1.5 V), showing the bipolar nature of our devices (set process). The electrical measurements were performed in a probe station connected to a Keithley 4200 A-SCS semiconductor parameter analyzer (SPA) applying voltage or current bias at room temperature. In pristine TiO_2 RRAMs described above, we formed the filament by applying a positive voltage sweep with an initial current compliance of $I_{cc} = 1$ μA. After initial forming, we repeated these measurements ($I_{cc} \leq 1$ mA) for ten cycles to ensure cyclability of the devices (see Supporting Information Section S2). Figure 1 show two examples of multiple $I-V$ curves obtained at two devices with an area of (b) 2×2 μm^2 and (c)

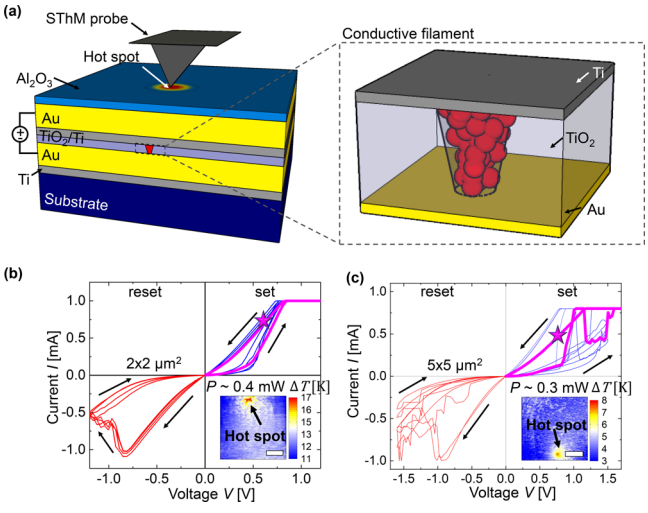

Figure 1. (a) Cartoon diagram of the device and measurement setup, showing the SThM probe on top of the RRAM. The zoom-in schematic shows the conductive filament formed in the active TiO_2/Ti layer upon application of an electrical bias V. (b, c) Measured $I-V$ characteristics of the devices for four cycles. The inset figures at the bottom right show the SThM temperature map of the same device at the bias point corresponding to the star symbol. The thermal maps reveal the hot spot generated by the filament for a device area of (b) 2×2 μm^2 (scale bar 350 nm) and (c) 5×5 μm^2 (scale bar 1 μm).

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$5 \times 5\ \mu m^2$. In both examples we observed the previously mentioned sharp increase and decrease of the electric current during the set and reset processes, respectively. After measuring more than 40 devices both electrically and thermally, we observed a higher cycle-to-cycle variability in the $5 \times 5\ \mu m^2$ devices compared to the $2 \times 2\ \mu m^2$ ones, as can be seen in Figure 1b,c. Additionally, we observed a higher intrinsic device-to-device variability in the $5 \times 5\ \mu m^2$ devices (see Supporting Information Section S3).

Thermal Characterization with SThM. SThM measurements were performed on our RRAMs to simultaneously image the topography and heating features on the device surface, while electrical bias is applied to the device. To obtain thermal maps with SThM, we used an Asylum atomic force microscope (AFM) and an SThM thermoresistive probe (Pd on SiN from Bruker). These SThM probes can correlate temperature variations in the tip to changes in electrical resistance with $\Delta R_{probe} \propto \Delta T_{probe}$.[41] The SThM probe is electrically connected to an external Wheatstone bridge consisting of two fixed resistances (1 kΩ each), a potentiometer (R_{pot}), and the resistance of the probe (R_{probe}). When the SThM is operated, a voltage bias is applied to the Wheatstone bridge to induce an electric current. The potential measured across the bridge (V_{SThM}) allows us to determine accurately the changes of the electrical resistance of the probe and, hence, temperature variations on the surface of the device. Note that the electric current through the probe causes Joule self-heating and an increase in probe temperature, which consequently results in an increase in its electrical resistance. For thermal sensing, this current must be as low as possible to keep the probe self-heating low compared to the temperature of the surface being scanned. During SThM scans, a constant electrical bias was applied between the two electrodes of the RRAM device. The conversion of SThM electrical probe signals into surface temperature to determine the heating of the RRAM devices is possible because of a process of calibration. For more details about the calibration, we would like to refer to ref 42 and Supporting Information Section S4.

As illustrated in Figure 1a, after the conductive filament is formed in the RRAM device, SThM can map the hot spot generated on the surface of the device due to Joule heating. In the insets of Figure 1b,c, we present two steady-state temperature maps with their corresponding $I-V$ curves. The star symbol indicates the voltage bias applied to the device while performing the SThM scan. In both cases, we observed a hot spot with a surface temperature increase of $\Delta T = 17$ and 8 K in the 2×2 and the $5 \times 5\ \mu m^2$ device, respectively, when powers of ~400 μW and ~300 μW were applied. We recall that this temperature was measured at the surface; therefore, it is not the internal temperature of the filaments, and one needs to consider that the heat generated by the filament in the metal oxide also spreads along the top and bottom electrodes. Therefore, both the temperature and the size of the heating spot at the surface differ from those of the buried filament, as shown by Deshmukh et al.[9]

Steady-State Measurements. Figure 2a shows the topography of a RRAM device scanned with an SThM probe. The topography of the devices can vary in their surface roughness. However, we observed the peak of the heating independently from the topographical artifacts (Supporting Information Section S5). Figure 2b shows a 3D representation of two thermal maps obtained for a $5 \times 5\ \mu m^2$ device at 0 mW power and at 0.24 mW in its LRS. During the first scan at the bottom, we scanned the cross-point area while no power is applied to the device, so the device is not heated. For the second map above, we applied a power of $P = 0.24$ mW to the device. In this case, a current of $I \sim 0.4$ mA passes through the filament, which results in a localized hot spot on the surface. Considering a stable filament resistance, the magnitude of the resulting surface temperature mostly depends on the power and polarity of the electric current applied to the device.

Figure 2 shows multiple temperature maps obtained on the device presented in Figure 2b after the device was set (c) vs reset (d). In the LRS the hot spot is localized at the same location, and its temperature scales up as the power applied to the device increases (same LRS, i.e., no cycling between images). We observed that the maximum hot spot temperature increased from 9 K at 0.14 mW to 14 K at 0.24 mW. The power itself does not impact the shape of the hot spot, but it increases

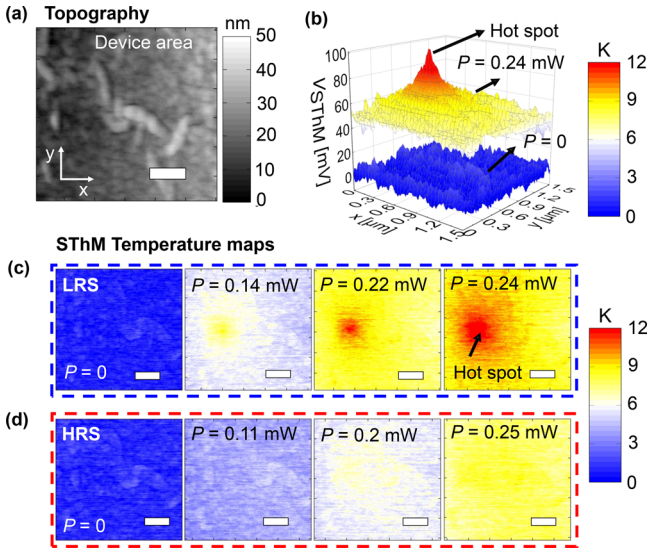

Figure 2. (a) Topographic image of a device with an area of $5 \times 5\ \mu m^2$ (scale bar 300 nm). (b) SThM thermal signal V_{SThM} (z-axis) map obtained for the device shown in (a) when applying a power of $P = 0.24$ mW and under no power applied ($P = 0$). The difference in SThM signal between heated and nonheated case is converted into a temperature change (Supporting Information Section S4), as represented by the color scheme. (c, d) SThM temperature maps with four different power levels after (c) setting the device at positive polarity (blue dashed rectangle) and after (d) resetting the device at negative polarity (red dashed rectangle) (scale bar = 300 nm).

the temperature. After reset, we obtained temperature maps for similar powers as in the set case but with reversed polarity (see Figure 2d). Considering the higher resistance in the reset, we applied higher voltages than in the LRS. At a power of 0.11 mW, we barely see any visible localized heating. At higher power we observed mostly uniform heating on the device, with little localized heating that could eventually be related to a partial but not complete breaking of the filament during the reset process. As an example, in Figure 2d at 0.2 mW, it looks like the breaking of the filament is not fully complete, as minor heating is still visible at the initial position of the filament. At sufficiently high power we observed a partial set of the device in agreement with the $I-V$ characteristics. In the $2 \times 2\ \mu m^2$ device of Figure 1b, we observed a softer breaking of the filament in accordance with the $I-V$ cycling behavior of the device (see Supporting Information Section S5).

The results in Figure 2 present the temperatures of the RRAM devices at the surface. For the characterization of the filament temperature, we employed an electrothermal simulation in COMSOL Multiphysics (see Supporting Information Section S6). Thus, we estimated the relevant material and contact characteristics in order to fit the temperature profiles of the maps in Figure 2 and the corresponding potential measured in our devices. As a result, we calculated the maximum filament temperature rise to be between 172 and 245 K above the ambient temperature, depending on the power applied to the device ranging from 0.14 to 0.24 mW (see Supporting Information Section S7).

In-Operando SThM Measurements at the Hot Spot. Next, we aimed to correlate the heating of the hot spot with the operando electrical $I-V$ behavior of the devices during cycling. For that purpose, we kept the SThM probe static at the position of the hot spot, which we localized during the steady-state measurements, while running $I-V$ sweeps on the device. The SThM software provides a logger option that records the operando SThM thermal signal as a function of time. This approach allows investigation of how the hot spot on the surface heats depending on the operando power applied. Figure 3 shows the $I-V$ measurements for devices with an area of (a) $2 \times 2\ \mu m^2$ and (b) $5 \times 5\ \mu m^2$. The right axes of these figures show the

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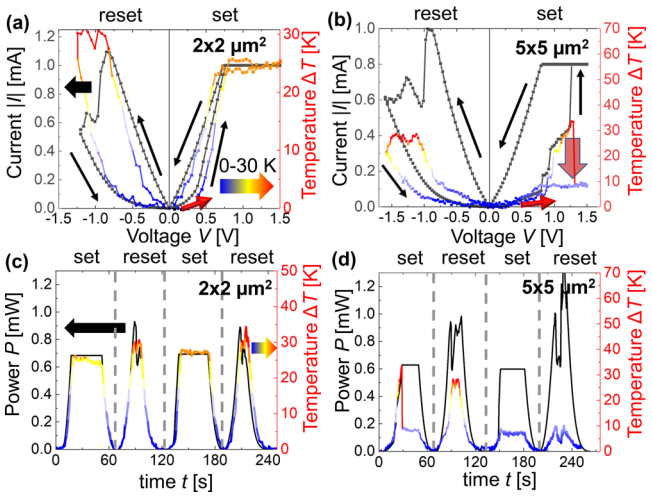

Figure 3. (a, b) Absolute electric current $|I|$ (left axis) and temperature increase ΔT (right axis) for one cycle (set and reset) as a function of the sweeping voltage for a device area of (a) 2 × 2 μm^2 and (b) 5 × 5 μm^2. The red arrows indicate the beginning of the sweep. (c, d) Electrical power (left axis) and temperature increase (ΔT, right axis) for two full cycles of set and reset as a function of time for a device area of (c) 2 × 2 μm^2 and (d) 5 × 5 μm^2. The color scale of the temperature graphs ranges from 0 K (blue) to ~30 K (red).

surface temperature measured by the SThM, which increases as the power of the devices rises. The temperature evolution in Figure 3a,b for the 2 × 2 and 5 × 5 μm^2 devices, respectively, follows the same trend as the $I-V$ curve for low voltages. However, we observed a drop in the temperature in the 5 × 5 μm^2 device illustrated by the partially transparent arrow during set, which is not in line with the $I-V$ curve obtained at higher voltages. Simultaneously the current sharply increases, which corresponds to the shift from HRS to LRS. With the aim to obtain more insights into this observation, we compared the SThM temperature measurements with the electrical power applied to the device.

Figure 3 shows the power and ΔT over different cycles of set and reset. Figure 3c shows that the heating measured by the SThM probe in the original position of the hot spot for the 2 × 2 μm^2 device is consistent for different cycles of set and reset. This is indicative of having a reliable filament that forms and breaks in the same device location, which we observed reliably for >10 devices. However, Figure 3d shows that the heating around the original filament location for the 5 × 5 μm^2 device varies during set and reset. This is indicative of position variation of the conductive filament, and it was observed in five devices. To further analyze this observation, we characterized how the steady-state measurements of the same devices as displayed in Figure 3 varied with cycling.

Steady-State Characterization after Cycling. In order to determine whether the location of the hot spot varies between set and reset cycles, we performed steady-state thermal maps of the same devices after $I-V$ sweeps. To verify a constant tip position during in-operando measurements, we used the same tip offset in the steady-state measurements before and after cycling. Figure 4 shows temperature maps together with the topographic image of the device for the two areas under study, i.e., (a) 2 × 2 μm^2 and (b) 5 × 5 μm^2. Each device was set and reset multiple times, and the steady-state thermal maps were obtained in the LRS between cycles.

The maps of the 2 × 2 μm^2 device reveal that the position of the hot spot and thus of the filament remained unchanged after cycling (Figure 4a). However, we observed a shift of the hot spot location in the maps of the 5 × 5 μm^2 device with an average distance of 1.6 μm between each other (Figure 4b). These SThM observations enable evaluation of the cycle-to-cycle variation by measuring the shift of the

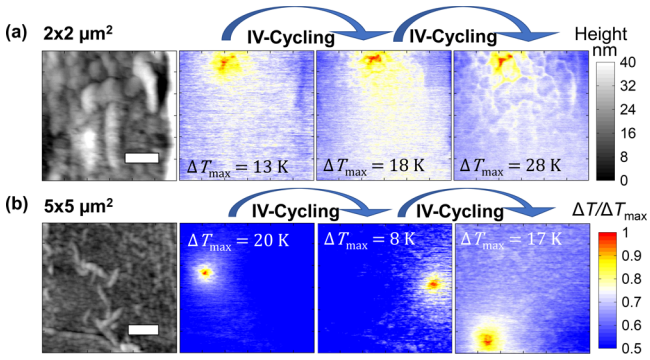

Figure 4. Topography (left) and surface temperature maps of the device (right) with area of (a) 2 × 2 μm^2 and (b) 5 × 5 μm^2 during steady-state measurements. The gray scale represents the topographical changes and the colored scale the temperature changes in these maps. Power P applied to the devices during the scans in (a) are 0.21, 0.4, and 0.57 mW and in (b) these are 0.39, 0.15, and 0.37 mW with a maximum temperature as labeled on each plot. The device power is the product of the voltage across and the current flowing through the device; differences in the resistance of the filament therefore affect the electrical power values.

filament position in RRAM devices, which cannot be done by electrical measurements.

DISCUSSION

With the thermal information provided here, we can observe the heat distribution on the surface of relevant RRAM devices during the set and reset processes. As an example, from Figure 4b we can see that the hot spot is moving, which relates to the formation of filaments in separate locations. The electrical information combined with the thermal SThM analysis displayed in this work for TiO_2 RRAM devices provides information relevant to the parameters that affect their reliability. In this case, the electrical and thermal signatures of the device allow us to draw conclusions on how the geometry and electrical connections affect the operation. More specifically, for a better understanding of these results, we discuss the differences in heating between the 2 × 2 and 5 × 5 μm^2 devices, considering (i) the area of the devices and (ii) the resistance of the top and bottom metal lines that connect the device with the electrode pads, which is equivalent to a series resistor.

First, we observed a shift of the hot spot location in five different devices with an area of 5 × 5 μm^2. The distance between each hot spot (distance between temperature peak) varied between 1.5 and 3 μm with an average distance of 2.21 ± 0.87 μm, and there were up to three possible hot spot locations with reversible switching at similar power conditions (see Supporting Information Section S8). This average distance between hot spots is larger than the size of the 2 × 2 μm^2 devices. Therefore, we suggest that the size of the device could be a limiting factor for the filament to relocate, being more favorable to form just one filament in smaller devices, <2 × 2 μm^2 (as hypothesized before).[43]

Second, an additional perspective correlates with the different widths of the metal lines connecting the top and bottom electrode with the pads. The size of the metal lines in the 2 × 2 μm^2 devices is smaller than in the 5 × 5 μm^2 devices, which results in a higher series resistance and lower capacitance. We measured the line resistance for both devices by applying a current between the electrode pad and the end of

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the electrode line. The resistance of the electrode metal lines for the 2 × 2 and 5 × 5 μm^2 devices were 308 and 123 Ω, respectively. However, the total series resistance is higher, as can be estimated from the measured $I-V$, following the work of Fantini et al.[44] From this estimation we obtained a total series resistance of around 1000 and 300 Ω for 2 × 2 and 5 × 5 μm^2 devices, respectively (see Supporting Information Section S9). The remaining resistance could originate from the conduction through the Ti layer and TiO_2/Ti interface, where a partial oxidation of the Ti occurs due to the oxygen exchange reaction.[45,46] Using an integrated series resistance has been shown to be an effective method to decrease transient current overshoot in RRAM devices.[47,48] The higher series resistance and lower capacitance in the 2 × 2 μm^2 devices makes them more robust against current overshoot during electroforming and set events, which could be responsible for the change of the active filament position observed in the larger 5 × 5 μm^2 devices.

Finally, in this work, we also analyzed the potential impact of cycling at the interfaces of the device. For that purpose, we employed a high-angle annular dark field scanning transmission electron microscope (HAADF-STEM) to characterize the device structure before and after filament forming and cycling. We used an energy-dispersive X-ray spectroscopy (EDX) detector to analyze the elemental distribution of the relevant elements (i.e., Ti, Au, and O) in the metal/insulator/metal structure (see Supporting Information Section S10). We observed a continuous interface between layers in the active area of the pristine devices. However, we observed small gaps at the interface between TiO_2 and the Au bottom electrode for the cycled devices regardless of cross-point area. Similar observations were noted by Carta et al.[49] in Pt/TiO_2/Pt devices. They observed a delamination between the TiO_2 and the top electrode for cycled devices, which they claimed to be induced from the O_2 gas generated during the filament forming process. The delamination may contribute to the cycle-to-cycle and device-to-device variabilities and further lead to performance degradation in the RRAM devices, though more evidence is required. Despite this effect, our $I-V$ characteristics and SThM images show that the device keeps switching during cycling with similar thermal and electrical characteristics. Therefore, we can conclude that the set and reset stem from the formation and breaking of the filament rather than being dominated by delamination effects.

CONCLUSION

In conclusion, we used SThM to obtain surface temperature maps of TiO_2 memory devices with multiple sizes, operating under both steady-state and operando conditions, to evaluate their heating features. The thermal insights obtained for the device combined with its electrical characteristics allowed us to correlate the reliability of the devices with their design parameters. The results obtained reveal that the position shift of filaments is a significant cause of the electrical variability in RRAM devices. Additionally, these results are indicative for the existence of multiple possible filament positions in specific designs of RRAM devices and demonstrated that heat dissipation can vary locally as a function of cycling. Future studies should continue analyzing the impact of the area, line resistance, and interfacial structure during cycling in other RRAM devices to gain a better understanding of how it affects their performance. On one hand, the SThM measurement approach presented in this study can be conveniently expanded for the thermal characterization of other filament-based switching memristive devices (e.g., unipolar and diffusive memristors). On the other hand, a more fundamental analysis of the forming process and filament features could also be addressed in the future, requiring carefully designed electrothermal experiments (e.g., measurements on various devices with different switching mechanisms) combined with filamentary electrothermal model analysis. Overall, SThM proves itself as a powerful approach to gain further insights into RRAM operation. This provides new routes for thermal and electrical characterization and engineering of RRAM not only restricted to metal oxide-based resistive switching.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaelm.3c00782.

Section S1: schematic of device structure with fabrication specifications; Section S2: $I-V$ curves of devices with up to 50 full cycles; Section S3: $I-V$ curves of devices that display cycle variability depending on the device area; Section S4: schematic and results of the SThM calibration approach; Section S5: SThM steady-state temperature maps of a 2 × 2 μm^2 device for different power and resistive states; Section S6: COMSOL model used for the characterization of the filament temperature; Section S7: FEM temperature profiles of a hot spot surface temperature in comparison to experimental results; Section S8: 3D SThM temperature maps of two devices of different area size as a function of cycling; Section S9: $I-V$ graphs of the electrodes for the characterization of the line resistance; Section S10: STEM micrographs and EDX maps of a pristine and cycled RRAM device; Section S11: $I-V$ and logger temperature evolution graphs for two devices with higher cycle number (PDF)

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Conceptualization: T.S., M.M.R., and M.L. Formal analysis: T.S., X.G., C.R., S.D., and Ç.K. Investigation: T.S., X.G., C.R., K.Z., Y.Y., and F.H. Methodology: T.S., X.G., C.R., M.M.R., H.H., and M.L. Supervision: M.M.R., M.L., H.H., and E.P. Visualization: T.S. and M.M.R. Writing−original draft: T.S. and M.M.R. Writing−review and editing: the manuscript was written through contributions of all authors. All the figures that appear in this article, in the supporting file, and in the table of contents were created by the authors. All authors have given approval to the final version of the manuscript.

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Notes

The authors declare no competing financial interest.

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Supporting Information: Spatially-resolved thermometry of filamentary nanoscale hot spots in TiO_2 resistive random access memories to address device variability

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S1 Fabrication of the samples

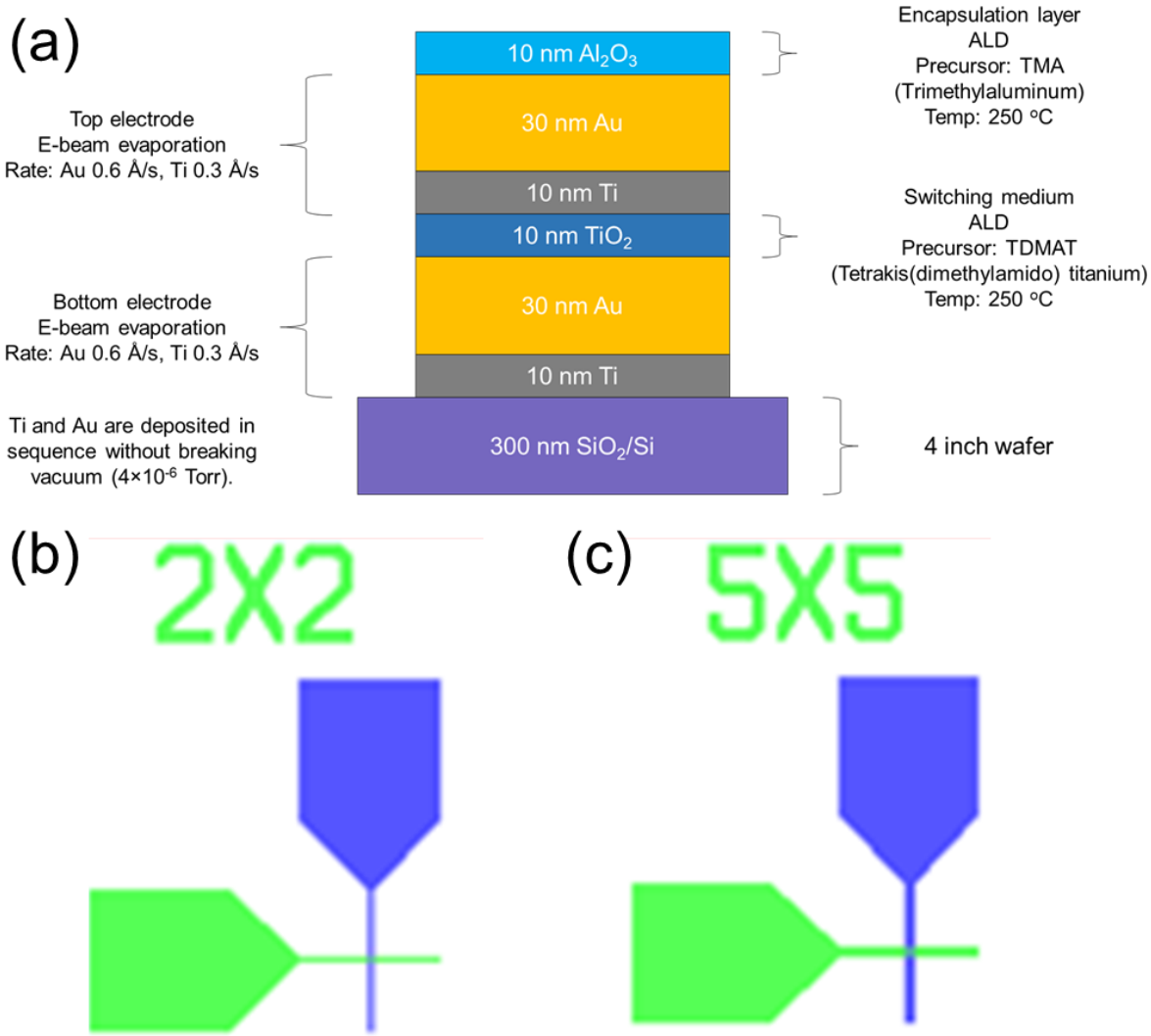

Figure S1. (a) Schematic of the fabrication procedure of the investigated samples. The thickness and fabrication method of each layer is indicated in the drawing. **(b,c)** Schematic of the cross-point structure for the (b) 2x2 μm^2 devices and (c) 5x5 μm^2 devices.

We fabricated our sample structure on top of a 300 nm SiO_2/Si substrate. We deposited 30 nm of Au as the bottom electrode on top of a 10 nm thick adhesion layer by means of e-beam evaporation. Then, we deposited the 10 nm TiO_2 active layer by means of atomic layer deposition (ALD) and 10 nm Ti through e-beam evaporation. After that, we deposited 30 nm Au top electrode by means of e-beam evaporation. For the purpose of electrical isolation, we capped the whole structure with a 10 nm thin Al_2O_3 capping layer. The details of the device layers are illustrated in Figure S1 (a). We arranged the devices in a cross-point structure with an active area size of (b) 2x2 and (c) 5x5 μm^2. The contact pad size is 100x100 μm^2 in both cases.

S2. Electrical characterization in RRAM

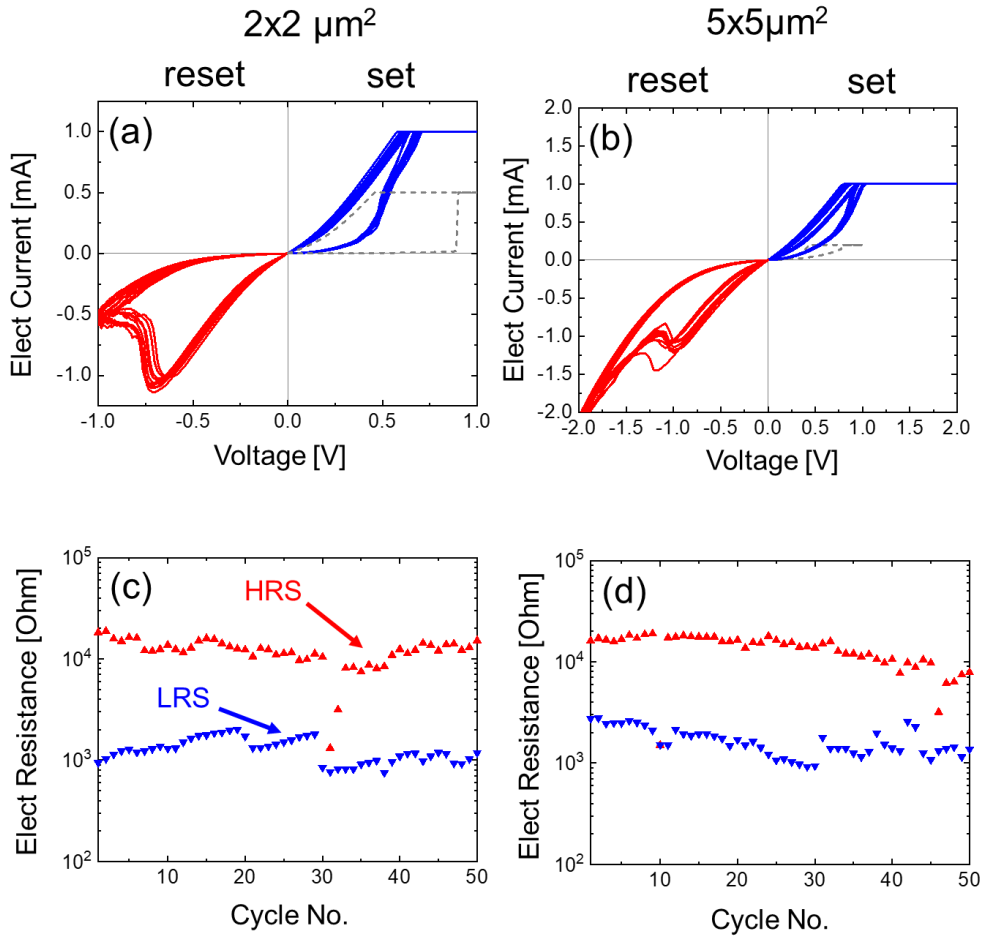

Figure S2. (a,b) Electric current as a function of the electrical voltage during the set (blue) and reset process (red) for 10 cycles in a (a) 2x2 µm² and in a (b) 5x5 µm² device. The grey dashed curves show the forming process. **(c,d)** Electrical resistance in the high resistive state (HRS) in red and the low resistive state (LRS) in blue of the RRAM devices vs number of cycles for a cross-point area size of (c) 2x2 µm² and (d) 5x5 µm².

For the electrical switching process of our resistive random access memory (RRAM) devices we performed electric voltage sweeps using a semiconductor parameter analyzer (SPA). Before forming the filament, we used an initial current compliance of I_{cc} = 1 µA, in order to decrease the severity of overshooting effects. However typically we required to use higher compliances in order to form the filament completely. The forming voltage $V_{forming}$ in between devices varied usually in the range of 0.5 to 2 V having a higher magnitude than the subsequent set voltage which is in line with observations in the literature.[1] After the forming process we reset the device by applying a reversed bias with a higher I_{cc} than in the last set or forming process. To ensure the cyclability of the devices we set and reset them for at least 10 cycles before we checked them with the scanning thermal microscope (SThM).

Figure S2 (a,b) show two examples of one 2x2 µm² and one 5x5 µm² devices representing ten full cycles. During the cycles we applied a constant current compliance during the set process to achieve consistent set conditions. Figure S2 (c,d) show the electrical resistance in the high resistive state (HRS) and the low resistive state (LRS) for two devices with a cross-point area of (c) 2x2 µm² and (d) 5x5 µm² during 50 full cycles. The HRS and LRS values were read at 0.07 V before and after the switching in the set process. The results support that our devices are capable of switching for more than 50 cycles.

S3. Device-to-device (D2D) and cycle-to-cycle (C2C) variability

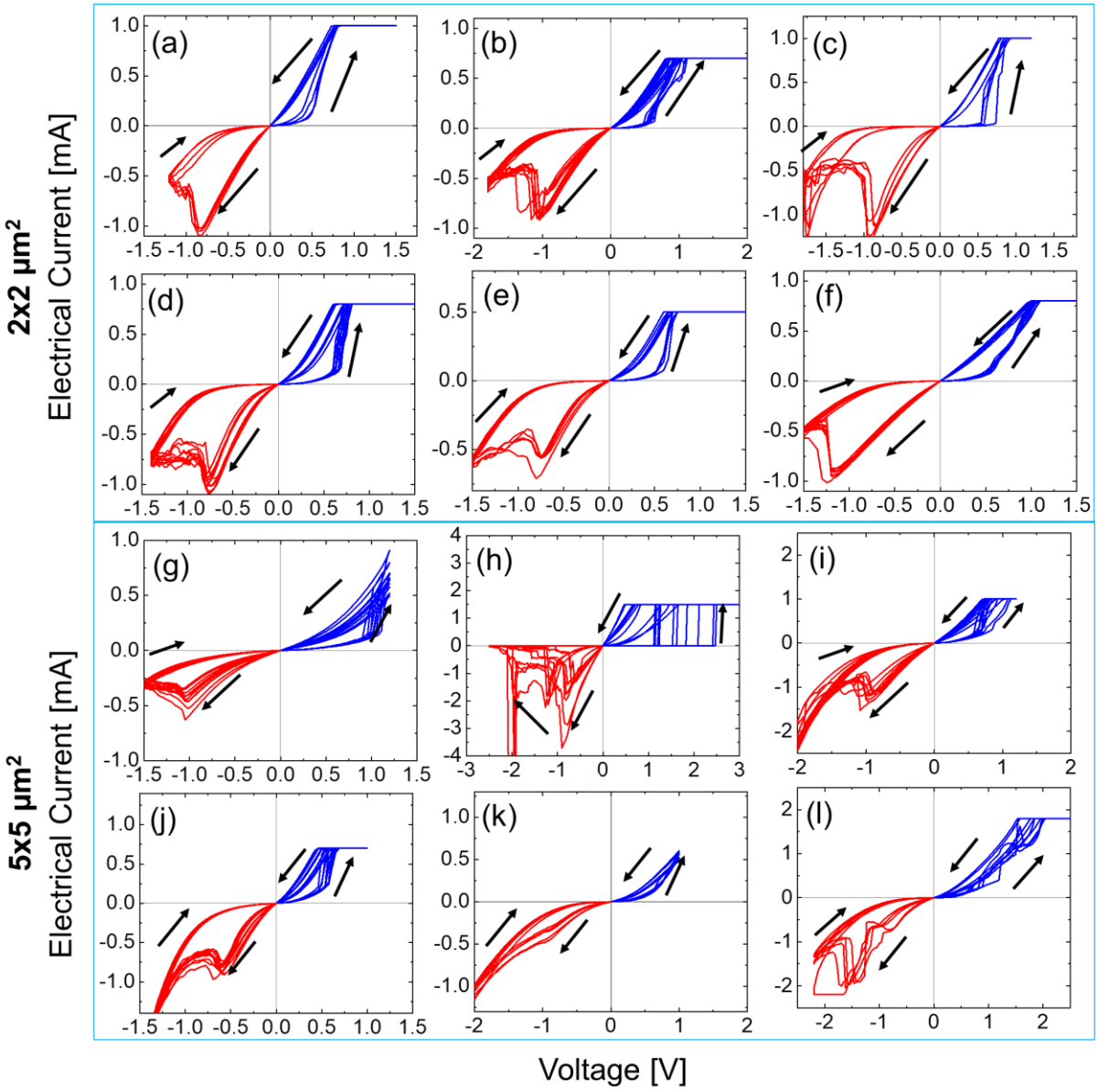

Figure S3. Measured *I-V* cycle characteristics for RRAM devices with a Crosspoint area of **(a-f)** 2x2 µm^2 and **(g-l)** 5x5 µm^2 for six devices each. The blue and the red graphs symbolize the set and reset processes, respectively. The black arrows present the direction of the set and the reset process.

One of the major limitations in RRAM devices is connected with the variability of the *I-V* characteristics. Figure S3 (a-f) show *I-V* cycles in six investigated 2x2 µm^2 devices which we investigated in-operando. In all the six devices we observed a relative stable cycle-to-cycle (C2C) behavior, i.e., the curves of the various cycles matched within the same device. In all the devices we can see a clear trend going from a small slope in the *I-V* curves to a sharp increase at a higher voltage magnitude during the set process. However, these graphs distinguish through the steepness of their slope.

Figure S3 (g-l) show *I-V* cycles in six investigated 5x5 µm^2 devices which we investigated in-operando. On contrary to the 2x2 µm^2 we saw an increased C2C and D2D variability illustrated due to a decay of the current (g), variation of the set voltage and strong reset (h), change of the set slope (i) or by multiple set steps (l). On average we observed a standard deviation of the forming voltage

of 10 % for the 2x2 μm^2 and 19 % for the 5x5 μm^2 devices showing an increased C2C variability in the 5x5 μm^2 devices.

In conclusion, we saw a significant difference in the stability of the *I-V* cycle behavior when comparing the 2x2 and the 5x5 μm^2 devices. The distinct types of set curves of the 5x5 μm^2 devices indicate a non-uniform formation step of the conductive filaments. These results demonstrate the need of thermal characterization of our devices in order to identify the source of the variability in these devices.

S4 Calibration of scanning thermal microscope (SThM)

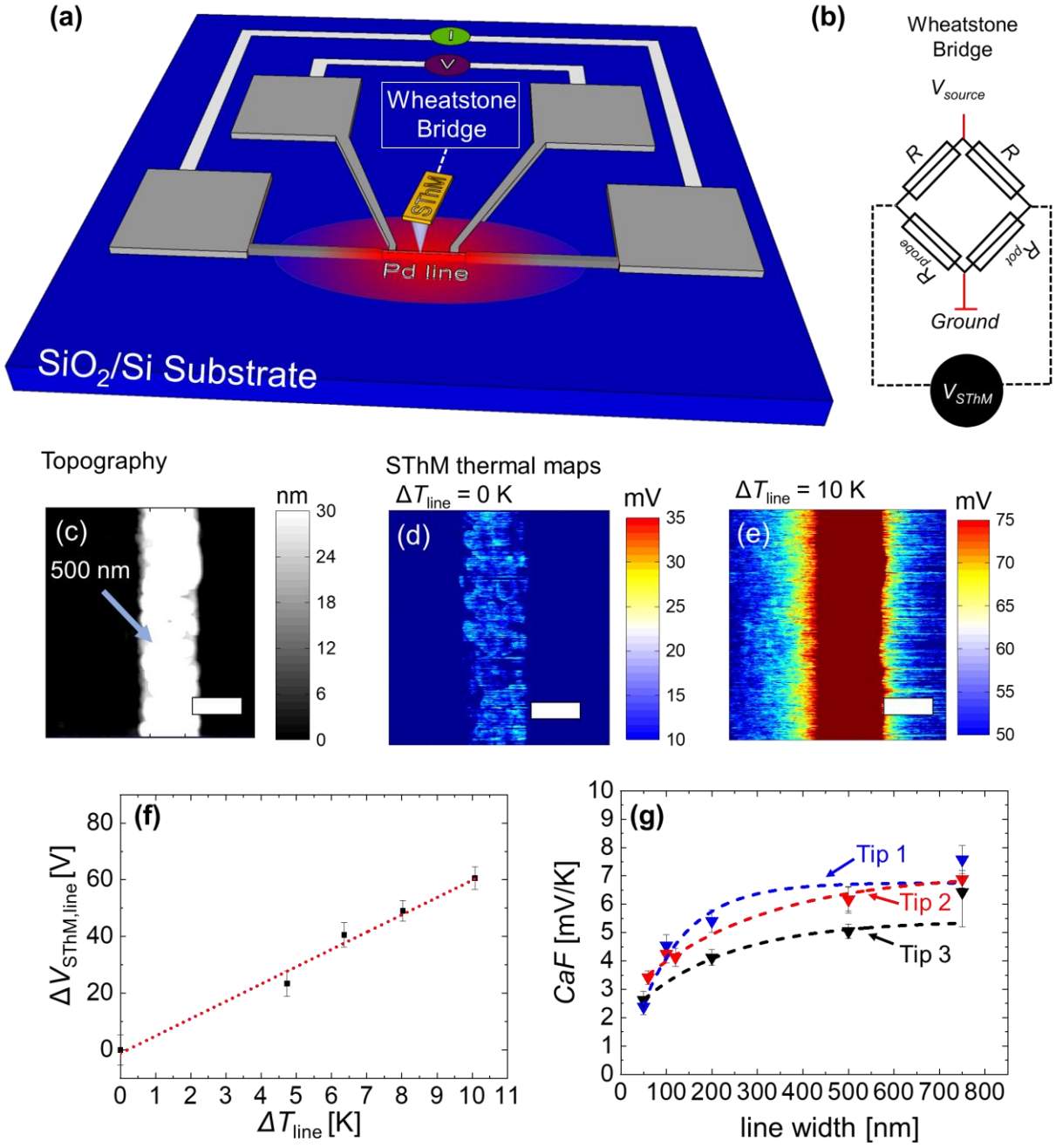

Figure S4. (a) Calibration sample and measurement configurations. Scanning thermal microscope (SThM) probe scans over heated palladium (Pd) lines of different widths (50-750 nm) connected to four Pd heater pads each. The thermoresistive metal lines are characterized electrically by four-Point probe measurements to determine the heating temperature of the lines. **(b)** Design of the Wheatstone bridge connected to the SThM probe during the scan. A constant bridge voltage V_{source} is applied during the measurement and the change in temperature is read due to changes in the bridge signal V_{SThM}. **(c)** Topography image of a 500 nm wide Pd line. **(d,e)** SThM thermal maps of the same line obtained with a temperature increase of the line ΔT_{line} of (d) 0 K (non-heated) and (e) 10 K (heated). (Scale bar is equal to 500 nm). **(f)** SThM thermal Signal of a 500 nm wide Pd line $\Delta V_{SThM,line}$ as a function of ΔT_{line}. **(g)** SThM Calibration Factor (*CaF*) estimated by means of the slope of the $\Delta V_{SThM,line}$ vs ΔT_{line} graphs as a function of the line width for the three different tips we used for the thermal characterization of our devices.

For the calibration of our scanning thermal microscope (SThM) probes, we used an approach as previously applied in literature.[2,3] Figure S4 (a) illustrates the calibration approach which we followed for the SThM thermo-resistive probes used in this study. For the calibration sample, we deposited four 2nm Ti/50 nm Pd heater pads by means of optical lithography and e-beam evaporation. Subsequently we fabricated 2 nm Ti/30 nm Pd metal lines of different widths (50-750 nm) through e-beam lithography and evaporation. To electrically isolate the sample from the probe we further deposited a thin 10 nm Al_2O_3 film on top of the calibration sample using pulsed laser deposition (PLD).[3]

We started with electrically characterizing the different Pd metal lines by applying four-point probe measurements. Therefore, we applied an electric current through the outer heater pads while measuring the voltage drop along the Pd lines through the inner pads, as shown in Figure S4 (a) by means of a semiconductor parameter analyzer (SPA). Pd is a thermo-resistive material meaning its electrical resistance R_{line} is temperature dependent and its value at a temperature T described as follows:

$$R_{\mathrm{line}}(T) = R_{\mathrm{line},0} \cdot (1 + TCR \cdot (T - T_0)) \tag{S1}$$

By means of equation S1 we can estimate the temperature at R_{line} of the line by knowing its temperature coefficient of resistance (TCR) and a reference value $R_{\mathrm{line},0}$ at the temperature T_0. The TCR is a material specific characteristic which we determined by measuring the resistance vs power curves of the lines for different temperatures (room temperature to 340 K) using a temperature adjustable sample stage. Using the TCR we calculated the temperature increase of the line as a function of the power applied to it. A more detailed description of the electrical characterization process can be found in our previous paper.[3]

In the second step we scanned the non-heated and heated metal lines with our SThM probes. In operation the SThM probes were connected to a Wheatstone bridge as illustrated in Figure S4 (b). This electrical network consists of two fixed resistances R (1 kΩ), one adjustable resistance R_{pot} and the resistance of the probe R_{probe}. In operation we applied a voltage across the bridge V_{source} of 0.5 V resulting in a power of 19 µW. In contact with the sample, we nullified the signal measured along the line V_{SThM}. Our SThM probes consists of a thin Pd resistor on top a SiN film. Thus, the resistance of the thermoresistive Pd probe correlates with the temperature of the probe. By that we measured differences in the surface temperature ΔT due to changes in V_{SThM} during the scan.

During the fabrication step we used the nullified SThM probe to estimate the temperature rise of the heated metal lines. As an example, Figure S4 (c) shows the topography map of a 500 nm wide line. In Figure S4 (d) and (e) we plotted two thermal maps obtained on the same line in a (d) non-heated (ΔT_{line} = 0 K) and (e) heated case ($\Delta T_{\mathrm{line}} \approx$ 10 K). In this case we still observed some minor signal variation in the non-heated case at the line, which are originated by differences in the tip to surface interaction. Therefore, we estimated the signal difference at the heated line $\Delta V_{\mathrm{SThM,line}}$ (ΔT_{line}) in comparison with $\Delta V_{\mathrm{SThM,line}}$(0) at a reference non-heated map to minimize the impact of topographical artefacts. Additionally, we determined the mean value of $\Delta V_{\mathrm{SThM,line}}$ along the line in order to reduce variation of the scan.

By following this principle, we estimated $\Delta V_{\mathrm{SThM,line}}$, measured with the SThM as a function of ΔT_{line} characterized electrically. Figure S4 (f) shows the $\Delta V_{\mathrm{SThM,line}}$ vs ΔT_{line} graph for the 500 nm wide Pd line obtained for five different heating configurations. As in previous studies, we observed a linear correlation of the SThM signal at the line and its temperature.[2,3] Hence, we calculated the calibration factor (*CaF*) of our SThM probes as a function of the line width by determining the slope of each $\Delta V_{\mathrm{SThM,line}}$ vs ΔT_{line} graph.

Figure S4 (g) shows the *CaF* vs line width graphs for the three tips used for the measurements of this study. All of the three graphs show the characteristic saturation behavior of *CaF* for higher line widths as observed before.[2,3] When comparing the three graphs we observed different saturation

values as also differences in the cut off line width of the graphs. Therefore, it is essential to calibrate each probe in order to maximize the accuracy of the calibration process. Each of the three probes are from different patches and therefore can vary in their characteristics.

For example, we obtained that the calibration factor for tip 2 saturated at a value of *CaF* = 7.1 $\pm$ 0.5 mV/K for surface temperature features above 680 nm. This *CaF* was used to calculate the temperatures of most of the hot spots observed experimentally, e.g., for the results in Figure 1 of the main manuscript where the full widths at half maximum (FWHM) of the hot spots exceed the cut-off line width. The electrical signal in mV measured with SThM (ΔV_{SThM}) was calculated as the difference between the heated maps and a reference map at zero power. Overall, ΔV_{SThM} can be converted to the temperature increase (ΔT) in K as follows:

$$\Delta T = \frac{\Delta V_{\mathrm{SThM}}}{CaF} \tag{S2}$$

At this point it is worth noting that a careful calibration allows this approach to be extended for the study of even smaller devices. As can be seen from the graphs in Figure S4 (g) we observe a drop in the calibration factor at a certain cut-off line width. This is related to the disc-shaped thermal exchange area between the tip and the sample. When the size of the device heating feature lies below the size of the cut-off line width, the heat exchange between the tip and device is truncated and the calibration factor decreases. However, beyond the cut-off, one should notice that the conversion factor drastically reduces. For devices or hot spots below ~50 nm determining an accurate value could be very challenging and might also involve considerable uncertainty. Therefore, additional strategies to alleviate it could be to measure in vacuum, i.e. to reduce the thermal exchange radius between the tip apex and the surface by removing heat transfer mechanisms like convection or water meniscus,[4] or to improve the signal processing techniques, like the deconvolution approach described by Deshmukh *et al*.[2]

S5. Steady state SThM characterization

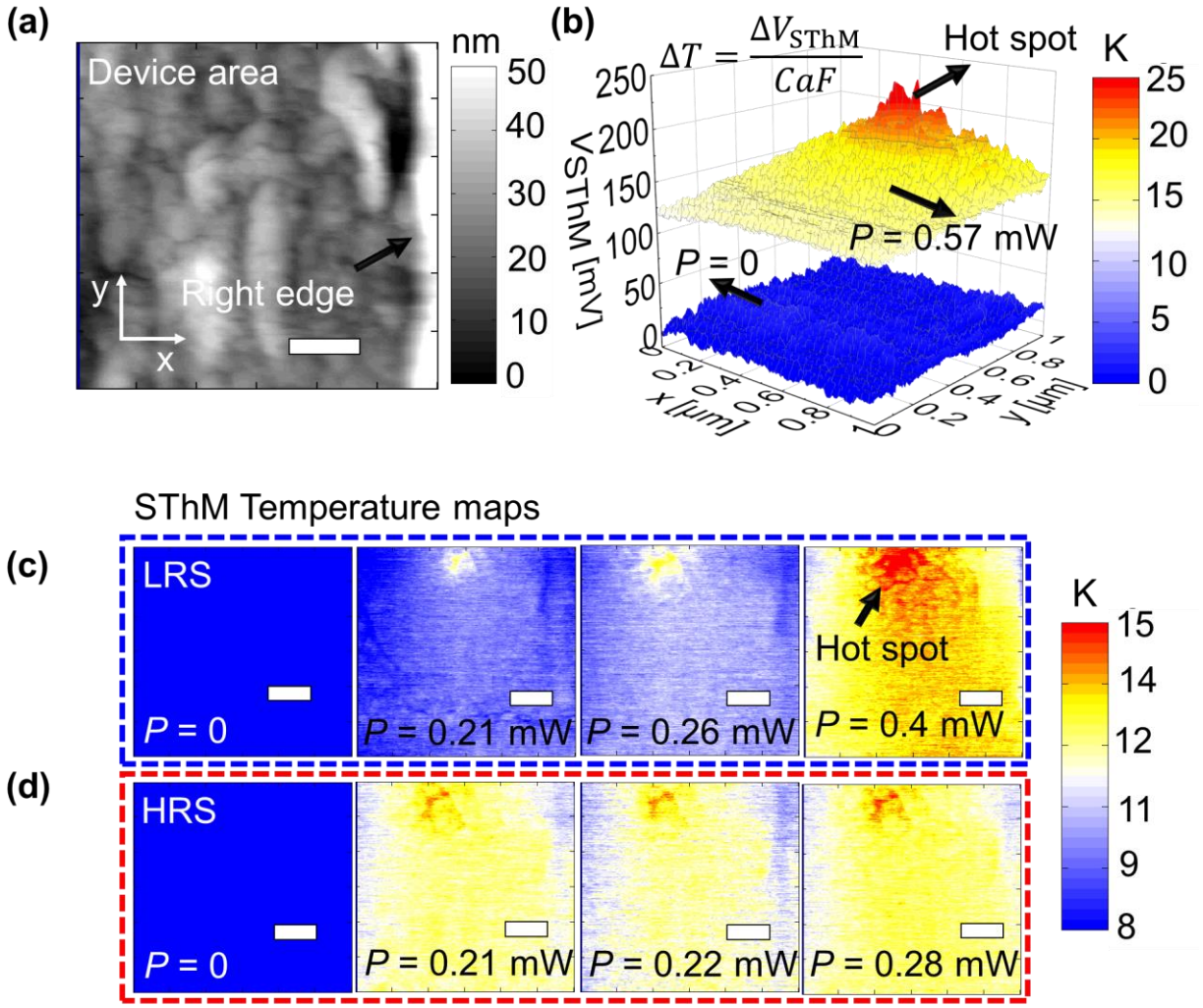

Figure S5. (a) Topographic image of a device with an area of 2x2 μm^2 (scale bar 200 nm) **(b)** 3D SThM temperature V_{SThM} (z-axis) map obtained for the device shown in (a) when applying a power of P = 0.57 mW and under no power applied (P = 0). The difference in SThM signal between heated *vs* non-heated case was converted into a temperature change by using a calibration factor of CaF = 7.1 mV/K. **(c)** and **(d)** SThM temperature maps for four different power magnitudes after (c) setting the device at a positive polarity (blue dashed rectangle) and after (d) resetting the device at the reverse negative polarity (red dashed rectangle). (scale bar 200 nm).

We repeated the procedure described in the main text for the thermal characterization of the hot spot for all our RRAM devices. Figure S5 (a) shows the topography map of a RRAM device with a cross-point area of 2x2 μm^2 obtained with a SThM probe. At this point it is worth mentioning that we observed a variation in the topography roughness of our devices as can be seen when comparing the topography in **Figure S5 (a)** with the one in **Figure 2 (a).** However, we want to clarify that the position of the hot spots is localized independent from any wrinkles or surface roughness variations. Therefore, we estimate that the formation of the filament is not triggered by topographical artifacts. Figure S5 (b) shows a 3D representation of two thermal maps obtained for the same 2x2 μm^2 device. Here we present two maps obtained for a non-heated case (P = 0 mW) and for a heated case (P = 0.57 mW). In the heated case we observed a hot spot induced by current passing through the conductive filament.

Figure S5 (c) shows multiple temperature maps obtained on the same device after the device is set (blue dashed rectangular) vs reset (red dashed rectangular). In the set state we can see that the hot spot is localized at the same location and its temperature scales up as the power applied to the device increases (same set state, i.e., no cycling between images). We observed that the maximum hot spot temperature increased from 13 K at 0.21 mW to 18 K at 0.4 mW. After resetting the device, we carried out temperature maps for similar powers as in the set case but with the reversed polarity (see Figure S5 (d)).

In comparison with the results in Figure 2 of the main text the differences in between the set and reset state are relatively low. By looking at the thermal maps during the reset state we still observed an elevated heating at the initial hot spot position but less localized than in the set state. So, as also observed with a weaker effect in the 5x5 μm^2 device, the filament breakdown is not fully complete. When comparing the set *I-V* curves of the two devices in Figure 1 (b) we can see that the difference before and after the set is comparable low in the 2x2 μm^2 device. Therefore, the smaller difference in between set and reset heating might originate from a less complete breakdown.

S6. COMSOL model for the characterization of the filament temperature

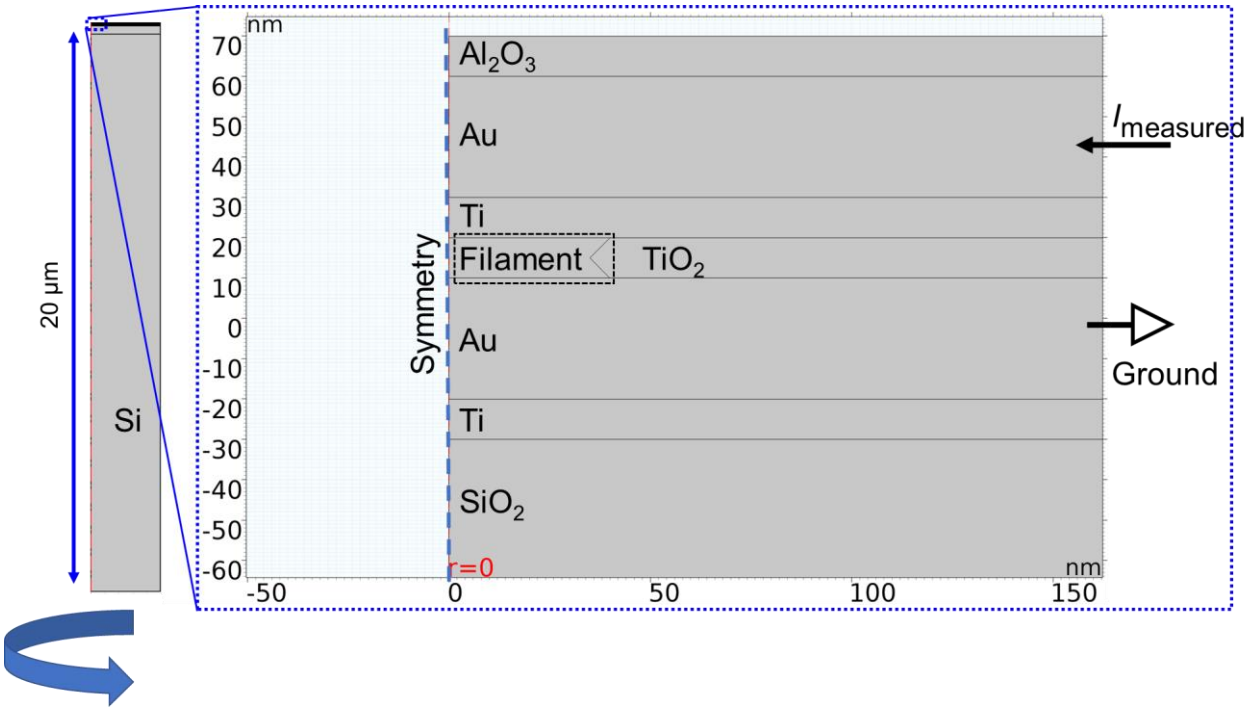

Figure S6. Finite element method (FEM) model geometry of the applied model for the characterization of the hot spot temperature. The model has a cylindrical symmetry around the central axis with a structure equivalent to the experimental TiO_2 RRAM devices with an hourglass shaped filament. An electric current $I_{measured}$ is applied from the top electrode to the bottom electrode.

In order to confirm the experimentally obtained temperatures and to estimate the filament temperature we employed an electrothermal finite element method (FEM) model in COMSOL Multiphysics. We built our model on base considering the same boundary and heat flux conditions of the results obtained in a study by Deshmukh *et al.*[2] By means of that we replicated the structure of the 5x5 µm^2 device which results are shown in Figure 2 of the main text. Therefore, we used a 2.5 x 2.5 x 20 µm model with a cylindrical symmetry around the central axis as shown in Figure S6. We adjusted the geometry to mimic our current $Si/SiO_2/Ti/Au/TiO_2/Ti/Au/Al_2O_3$ as described in Section S1. As can be seen in Figure S6 we shaped the Filament on the left edge of the TiO_2 using an hourglass structure, as this approach showed the best fitting.

In accordance with previous studies we estimated the thermal contact conductance in between the oxide and the top electrode $G_{TiO2\text{-}Ti/Au}$ using the full width at half maximum (FWHM) of our SThM scans of the hot spot as follows.[2] The thermal healing length of the hot spot is

$$L_H = \sqrt{\frac{k_{th,TE} \cdot t_{TE}}{G_{TiO2-Ti/Au}}} \quad \text{(S3)}$$

where $k_{th,TE}$ and t_{TE} are the thermal conductivity and thickness of the top electrode, respectively. In our RRAM devices we can estimate FWHM ≈ $2L_H$ given the small size of our filaments ($d_{CF} \ll L_H$). Therefore, we estimated the FWHM of the hot spot temperature peaks for the three images investigated. The thickness and thermal conductivity of the top electrode as also the remaining material characteristics are assembled from the literature and the COMSOL library. Table S1 shows the fixed material and contact parameters used for this FEM simulation. It is worth noting that one can reduce the heat spreading from the filament to the surface by reducing the thickness of the top electrode. On the other hand, it is also important to take into account that another key restricting factor for this heat spreading is the thermal interface between the filament and the top electrode, as discussed by Deshmukh et al.[2]

For the characterization of the Joule heating, we adjusted the top electrode as a current source with an applied current equal to the values measured during the SThM mapping $I_{measured}$. The bottom electrode acts as the electrical ground at which the potential is 0 V.

Table S1. Model Parameters used in the COMSOL Simulation

Parameter	Value at room temperature	Reference
σ_{Au}	**$14.28 \cdot 10^6$ S/m**	[7]
k_{Au}	**90 W/(m·K)**	[7]
k_{TiO2}	**0.8 W/(m·K)**	[8]
k_{Ti}	**8.2 W/(m·K)**	[9]
$G_{TiO2\text{-}Ti/Au}$	**1.25 MW/(m^2·K)**	[2]
σ_{TiO2}	**10^{-15} S/m**	[2]
k_{SiO2}	**1.4 W/(m·K)**	COMSOL Database
k_{Si}	**150 W/(m·K)**	[2]
k_{Al2O3}	**3 W/(m·K)**	[2]
$G_{SiO2\text{-}Ti/Au}$	**80 MW/(m^2·K)**	[10]
$G_{SiO2\text{-}Si}$	**434 MW/(m^2·K)**	[2]

S7. Estimation of the hot spot characteristics

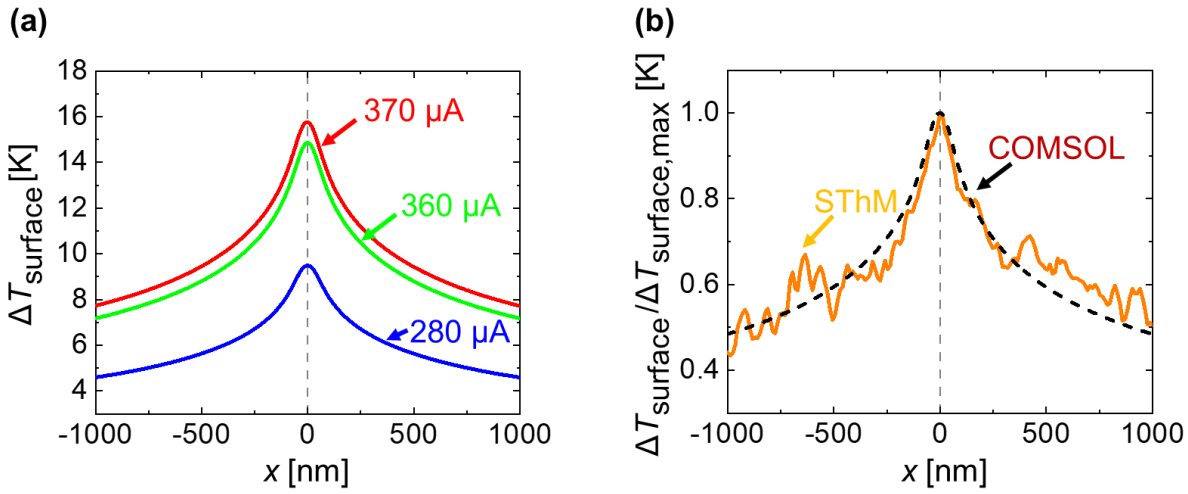

Figure S7. (a) Simulated temperature increase along the surface $\Delta T_{surface}$ of the 5x5 µm^2 RRAM device structure for three different currents $I_{measured}$ (280 µA in blue, 360 µA in green and 370 µA in red). **(b)** Normalized simulated (dashed line) and measured SThM (straight line) temperature increase $\Delta T_{surface}/\Delta T_{surface,max}$ along the surface of the RRAM device for an electric current $I_{measured}$ of 280 µA.

For the estimation of the hot spot characteristics, we adjusted the remaining model parameters in order to fit the surface temperature, FWHM and the electrical potential measured during the SThM scans. The sweep parameter included the size characteristics of the filament (top radius, bottom radius and the center radius) the thermal conductivity of the filament $k_{th,filament}$ the thermal contact conductance in between the filament and the top and bottom electrode $G_{CF\text{-}TE}$ and $G_{CF\text{-}BE}$ respectively and the electrical contact resistance in between the filament and the top electrode $\rho_{c,\,CF\text{-}TE}$. The initial values for these parameters were estimated on base of the simulation characteristics displayed in ref.[2]

Table S2. Comparison of the hot spot characteristics of the SThM measurements and the COMSOL Multiphysics simulation for the three investigated scans. Also shown are the corresponding sweep parameters that showed the best fits.

Characteristic	**$I_{measured}$ = 280 µA**	**$I_{measured}$ = 360 µA**	**$I_{measured}$ = 370 µA**
Experimental observations			
FWHM [nm]	**1820**	**1920**	**1820**
$\Delta T_{max,surface}$ [K]	**8.62**	**12.52**	**13.9**
Potential [V]	**0.41**	**0.49**	**0.54**
COMSOL Multiphysics results			
FWHM [nm]	**1880**	**1820**	**1820**
$\Delta T_{max,surface}$ [K]	**9.48**	**14.75**	**15.82**
Potential [V]	**0.41**	**0.49**	**0.54**
$\Delta T_{max,filament}$ [K]	**171.61**	**238.85**	**245**
Sweep Parameter			
$k_{th,\,filament}$ [W/(m·K)]	**3**	**3**	**3**
***Bottom radius* [nm]**	**43**	**44**	**47**
***Top radius* [nm]**	**41**	**43**	**43**
***Center radius* [nm]**	**38.5**	**41**	**41.5**
$G_{CF\text{-}TE}$ [MW/(m^2·K)]	**12**	**12**	**12**
$G_{CF\text{-}BE}$ [MW/(m^2·K)]	**100**	**100**	**100**
$\rho_{C,\,CF\text{-}TE}$ [Ω·cm^2]	**4.76 · 10^{-8}**	**5 · 10^{-8}**	**5.26 · 10^{-8}**

Table S2 shows the sweep parameter and the results of the COMSOL simulation which presented the best fit with the experimental results. Figure S7 (a) shows the corresponding simulated temperature profiles at the surface of the RRAM devices for the best fitting parameters of the three investigated SThM maps. In general, we observed a good fit of the FWHM and the potential drop in between experiments and simulation. We obtained slightly higher (10-15 %) values for the maximum temperature at the surface $\Delta T_{max,surface}$ from the simulation in comparison with the experimental results. Considering the error of our calibration factor and the other material parameters this temperature difference is in a reasonable range. Figure 7 (b) shows a fit of the experimentally obtained surface temperature profile (straight line) with the profile obtained from the COMSOL simulation (dashed line) for $I_{measured}$ = 280 µA. In this graph we normalized the temperature in order to take the temperature difference into account.

It is worth noting that heat dissipation depends on the device area. For wider area devices, electrodes can carry away heat more easily which leads to a decrease in the maximum surface temperature under identical thermal interfaces, filament size and electrode thermal conductivity.

In comparison to the results of Deshmukh *et al.*[2] we estimated a higher $k_{th,filament}$, which can be originated from the difference in the material characteristics and higher thickness of the titanium oxide layer and thus the filament. Additionally, our simulations results indicate a relatively high filament diameter of around 41-44 nm, which is connected to the relatively high electric currents applied to the device. Finally, the maximum temperature increases of the filaments $\Delta T_{max,filament}$ is estimated to be in between 172 and 245 K, correlating with the power applied to the device.

S8. Hot spot location with cycling

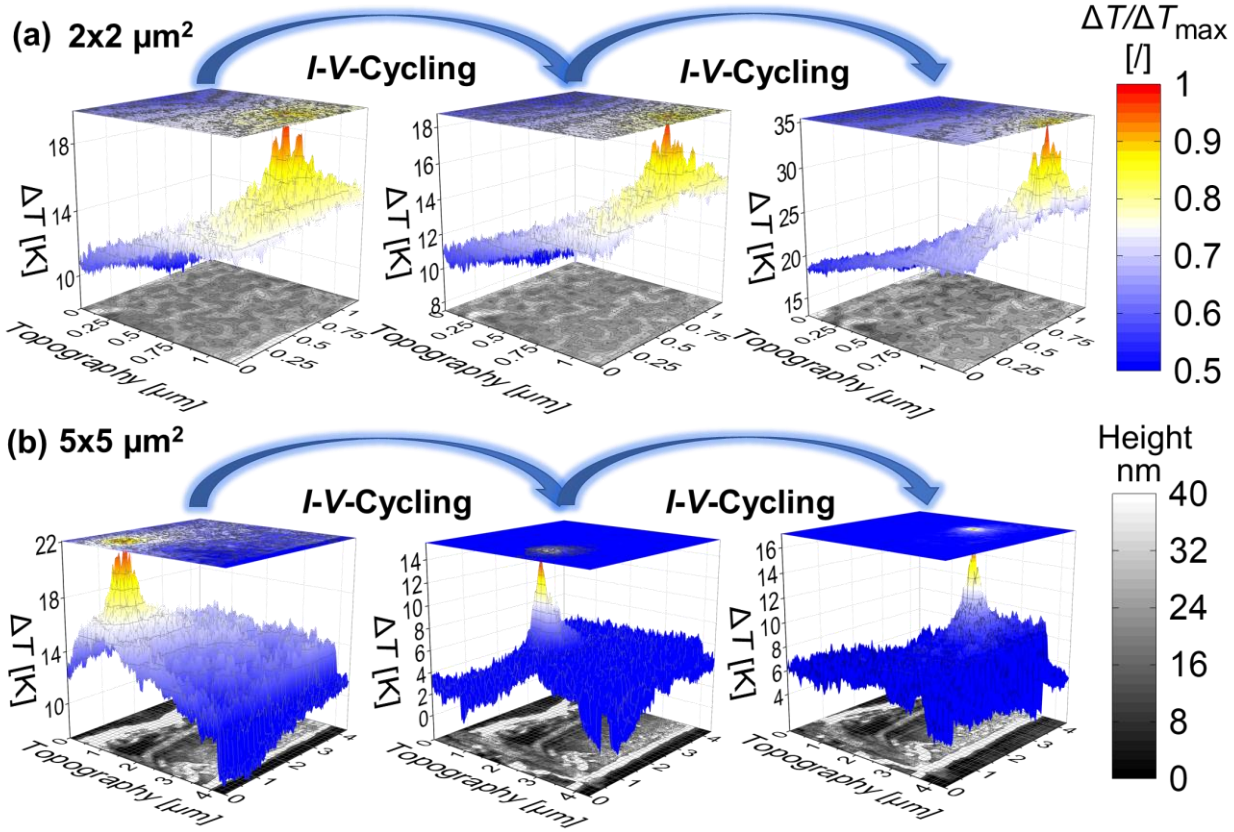

Figure S8. 3D surface temperature maps (z-axis) plotted over the 2D topography (x and y axis) of devices with an area of **(a)** 2x2 µm² and **(b)** 5x5 µm². The 2D topographic maps at the bottom show the height differences in the scanned area (greyscale bar on the bottom right). The color scheme of the 3D plots shows the temperature increase during the steady state measurements (colored bar on the top right). Power *P* applied to the devices during the scans in (a) are 0.33 mW/0.32 mW/0.59 mW and in (b) are 0.27 mW/0.55 mW/0.47 mW from left to right.

For the characterization of the hot spot moveability, we repeated the steady state measurements of the devices after *I-V* cycling, Figure S8 (a) and (b) show two examples of heat dissipation in set devices at different stages of cyclability for a (a) 2x2 µm² and (b) 5x5 µm² device. In addition to the maps of Figure 4 of the main text, we observed a static hot spot position in the 2x2 µm² device while a shift of the hot spot occurred in the 5x5 µm² device.

S9. Characterization of the line resistance

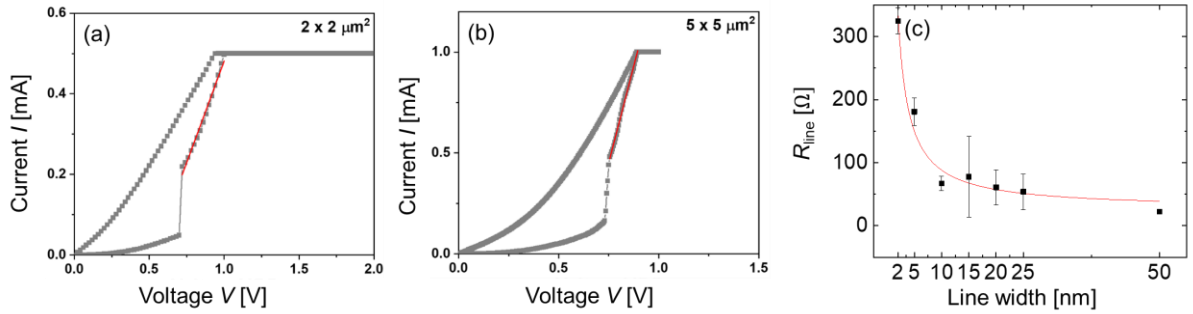

Figure S9. (a) and (b) Measured *I-V* characteristics of the 2x2 µm^2 and 5x5 µm^2 devices, respectively. The red line is the fit of the linear region. (c) Measured line resistance R_{line} of the bottom and top electrode as a function of the line width of the device.

The *I-V* curves we measured are the extrinsic *I-V* characteristics. The voltage drops not only on the memory cell but also on the series resistance, which includes the line resistance of the electrodes, the contact resistance of the probes and pads and other contributions from the device stack, as for example the vertical conduction in the electrodes. By subtracting the voltage drop over the series resistance, the intrinsic *I-V* characteristics can be obtained.[5] Fantini et al.[5] reported that the intrinsic *I-V* behavior of resistive switching devices shows that the set is triggered at a certain threshold voltage and is followed by a snapback to a voltage value where the differential resistance *dV/dI* is approximately 0, i.e. a vertical line in the *I-V* characteristics. Taking this into account, the series resistance can be estimated by calculating the series resistance value that transforms the extrinsic *I-V* curve into the intrinsic one, exhibiting the vertical transition behavior.

We extracted the approximate value of the series resistance for 2x2 µm^2 and 5x5 µm^2 devices from the extrinsic *I-V* curves in Figure S9 based on the abovementioned method. During the set process, after the abrupt jump at the threshold voltage, the current shows a linear dependence with the voltage before reaching the compliance. This is caused by the series resistance. Its value can be estimated from the slope of the curve in the linear region (the red line in Figure S9). The estimated series resistance of 2x2 µm^2 and 5x5 µm^2 devices is 1 kΩ and 300 Ω, respectively. The contact resistance between the probe and the electrode is similar due to the same measurement method, therefore the line resistance and the other electrode contributions should be the dominating cause of the difference in the series resistance. To be noted, these values are not for the pristine devices, but for the devices that switched for at least 20 cycles.

Additionally, we measured the line resistance of both the top and bottom electrode for various pristine devices. Figure S9 (c) shows the measured combined line resistance R_{line} of the bottom and top electrode as a function of the line width. At a higher line width, we observed a relatively constant value for R_{line}. In these cases, we expect the contact resistance between the measuring probes and the electrode surface to be the dominating factor of R_{line}. For the relevant line widths (2 µm and 5 µm) we measured an increment in the line resistance based on the decreased line area. By subtracting the estimate of the contact resistance, we obtained a R_{line} of 123 Ω and 308 Ω for the 5x5 and 2x2 µm^2 devices, respectively. The difference from the measured line resistance and the estimated series resistance stems from the contact resistance between the lines and the active area and possible other resistances which are not included in the line resistance.

S10. STEM characterization of the layer structure in pristine and cycled devices

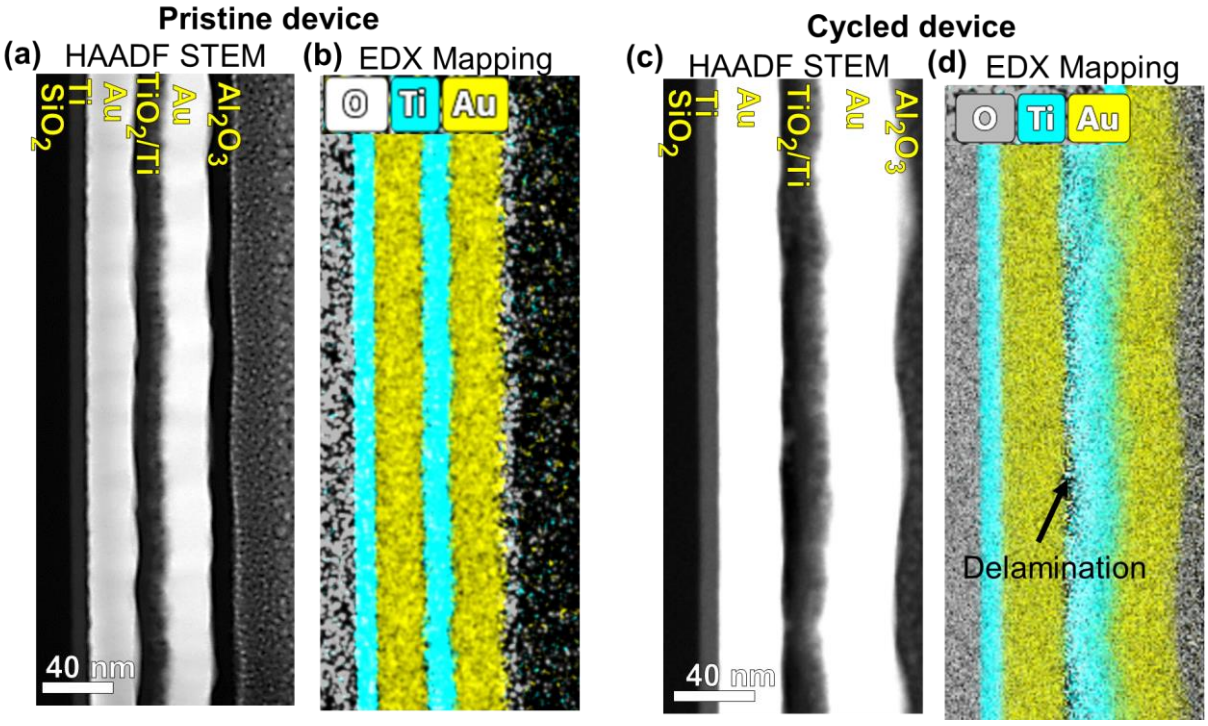

Figure S10. (a) High-angle annular dark field scanning transmission electron microscopy (HAADF STEM) images of a crosspoint device area of one pristine 5x5 µm^2 TiO_2 RRAM device. (b) Energy-dispersive X-ray spectroscopy (EDX) images showing the gold (gold), titanium (light blue) and oxygen (grey) compositions of the same area as in (a). (c) High-angle annular dark field scanning transmission electron microscopy (HAADF STEM) images of a cross-point device area of one cycled 5x5 µm^2 TiO_2 RRAM device. (d) Energy-dispersive X-ray spectroscopy (EDX) image showing the Gold (gold), Titanium (light blue) and oxygen (grey) compositions of the same area as in (c).

In order to investigate the impact of the electrical forming and cycling of the device on the material structure we employed high-angle annular dark field scanning transmission microscopy (HAADF-STEM) with an energy-dispersive X-ray spectroscopy (EDX) detector. First, we cut the samples out of the cross-point area of our RRAM devices using the focused ion beam (FIB) technique. Second, we employed transmission electron microscopy (TEM) in the cross-section direction for the characterization and evaluation of the device layer structure. By means of that we aimed to evaluate the chemical composition and distribution of the three main elements i.e., Au, Ti and O which are the building blocks for the metal/insulator/metal (Au/TiO_2/Ti/Au) structure of our RRAM devices.

Figure S10 (a) and (b) show the HAADF and the EDX images obtained from a pristine, i.e., not electrically formed device. Hereby, the HAADF imaging method enables us to clearly identify the high atomic number Au electrodes. The remaining layers are indicated in Figure S10 (a) according to the device structure. We clearly observed a continuous Ti and O signal along the TiO_2/Ti areas in between the electrodes.

Figure S10 (c) and (d) show the HAADF and the EDX images obtained of an already cycled 5x5 µm^2 device. Similar to the pristine device the EDX image shows a clear Au signal at the position of the electrodes. However, we observed a small but not continuous drop of the Ti and O signal at the transition area in between the TiO_2 layer and the bottom electrode.

Similar observations have been made by Carta *et al.*[6] in a Pt/TiO_2/Pt RRAM device. In their study, they investigated the material structure of their RRAM devices in pristine and in formed state. They performed HAADF-STEM measurements with an EDX detector for the characterization of the

devices before and after electrical cycling. On the one hand they observed a continuous Ti and O signal in the pristine device. On the other hand, the measurements revealed a drop in the Ti and O signal in between the TiO_2 layer and the Pt top electrode in the formed devices referred to delamination. This delamination effect was claimed to be originated from the development of O_2 gas during the formation of the conductive filament.

From our results we cannot make a solid conclusion about the impact of the layer delamination observed in our devices on their *I-V* or heating variation during cycling. However, we should emphasize that this effect might lead to a limitation in the electrical performance and variability of RRAM devices. Presumably, the delamination should lead to a reduction of the effective cross-point area of the devices.

S11. *I-Vs* and thermal data for multiple cycles

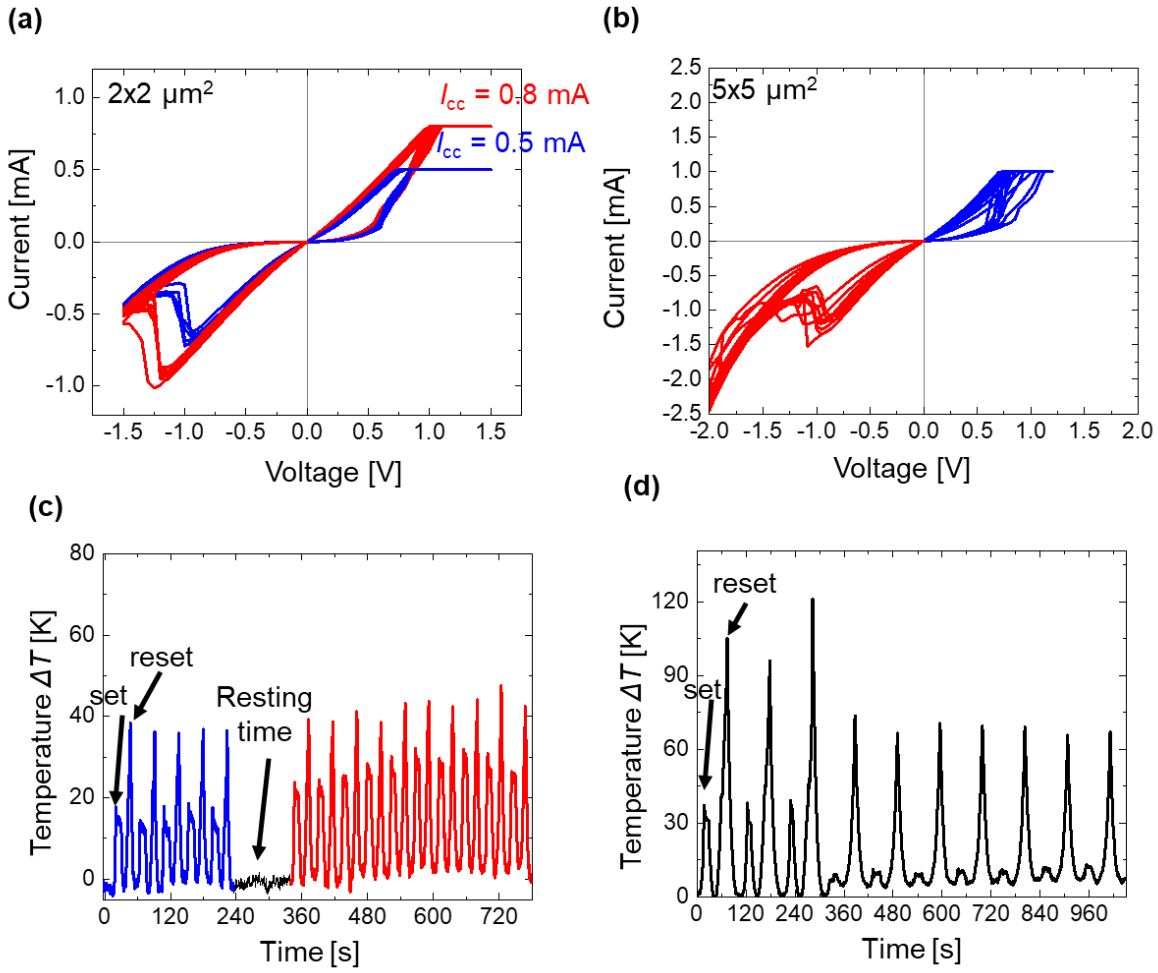

Figure S11. (a) and (b) *I-V* curves for 15 and 10 cycles for 2x2 µm² and a 5x5 µm² devices, respectively. (c) and (d) logger temperature measured for the different set and reset cycles of the devices shown in (a) and (b), respectively, at same SThM probe location.

Figure S11 shows two examples of *I-V* graphs and the corresponding SThM-temperature logger graphs of a 2x2 µm² and a 5x5 µm² device. Figure S11 (a) and (b) show the current vs voltage behavior of the devices during cycling. Figure S11 (c) and (d) show the temperature evolution at the initial hot spot location measured simultaneously during the *I-V* cycling for 15 and 10 full cycles, respectively. The cycling behavior of the 2x2 µm² device remains constant, accompanied by a consistent series of set-reset temperature evolutions in the logger graphs, indicating a static hot spot location. This can also be observed at different current compliances I_{cc} (blue I_{cc} = 0.5 mA vs red I_{cc} = 0.8 mA). However, in the 5x5 µm² device we observe a drastic change of the temperature evolution in accordance with the variability of the *I-V* curves. The device still remains cyclable, but the temperature becomes lower after a certain number of cycles. These observations indicate that a new filament is eventually formed at a different location. This behavior can be extrapolated to more cycles, simply based on the reliability of the device. As we show in supporting information section S2, our devices remain cyclable after 50 switching cycles.

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