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Lateral electrical transport and field-effect characteristics of sputtered p-type chalcogenide thin films

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ABSTRACT

Investigating lateral electrical transport in p-type thin film chalcogenides is important to evaluate their potential for field-effect transistors (FETs) and phase-change memory applications. For instance, p-type FETs with materials sputtered at low temperature ($\leq$ 250 °C) could play a role in flexible electronics or back-end-of-line silicon-compatible processes. Here, we explore lateral transport in chalcogenide films (Sb_2Te_3, $Ge_2Sb_2Te_5$, and $Ge_4Sb_6Te_7$) and multilayers, with Hall measurements (in $\leq$ 50 nm thin films) and with p-type transistors (in $\leq$ 5 nm ultrathin films). The highest Hall mobilities are measured for Sb_2Te_3/GeTe superlattices ($\sim$18 cm^2 V^{-1} s^{-1} at room temperature), over 2–3× higher than the other films. In ultrathin p-type FETs with $Ge_2Sb_2Te_5$, we achieve field-effect mobility up to $\sim$5.5 cm^2 V^{-1} s^{-1} with on/off current ratio of $\sim$10^4, the highest for $Ge_2Sb_2Te_5$ transistors to date. We also explore process optimizations (e.g., the AlO_x capping layer, type of developer for lithography) and uncover their tradeoffs toward the realization of p-type transistors with acceptable mobility and on/off current ratio. Our study provides essential insights into the optimization of electronic devices based on p-type chalcogenides.

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Sputtered tellurium (Te) based chalcogenides with germanium (Ge) and antimony (Sb) have attracted attention for various electronic applications, such as phase-change memory, transistors, and thermoelectrics.[1–5] A key advantage of these materials is their low deposition and crystallization temperature ($\leq$250 °C), which makes them compatible with both flexible electronics[6] and silicon back-end-of-line (BEOL) applications[7] ($\leq$500 °C). In addition, these materials also have p-type semiconducting properties, which make them particularly interesting for low-power complementary metal-oxide semiconductor (CMOS) applications, because very few inorganic p-type materials can be deposited with low-cost, large-area methods.[8,9] For instance, p-type semiconducting oxides suffer from structural defects and material instability.[10] Furthermore, integration of p-type carbon nanotubes is more challenging due to chirality and diameter variation,[11] requiring solution-based purification with polymers, which must be later removed.[12,13]

In this regard, sputtered p-type chalcogenides can provide a promising alternative because their low crystallization temperature enables good mobility within a thermal budget below 250 °C. Lateral (in-plane) transport studies of bulk crystalline films of these chalcogenides using Hall measurements demonstrate good hole mobility at room temperature: $\sim$350–400 cm^2 V^{-1} s^{-1} for Sb_2Te_3,[14,15] $\sim$120 cm^2 V^{-1} s^{-1} for GeTe,[16,17] and $\sim$30–50 cm^2 V^{-1} s^{-1} for $Ge_2Sb_2Te_5$.[16,18] Despite showing reasonably high Hall hole mobility, Sb_2Te_3 has not been explored as a potential candidate for FETs. There are only few reports involving $Ge_2Sb_2Te_5$ thin film (10–100 nm) transistors that show limited performance,[2,19–23] not reaching the high mobility found in bulk and an on/off current ratio less than 20. Recently, 5 nm thick $Ge_2Sb_2Te_5$ was used in flexible thin film transistors[24,25] achieving an improved on/off ratio up to $\sim$388 at room temperature. These chalcogenides also remain popular phase-change materials because of their large resistance contrast (up to five orders of magnitude) between their crystalline and amorphous phases.[26] Moreover, recent developments in phase-change memory technology have made use of chalcogenide superlattices consisting of layers only a few nanometers thick.[27,28] Therefore, the electrical transport study of such thin chalcogenide films will also be useful for optimizing their applications in phase-change memory.

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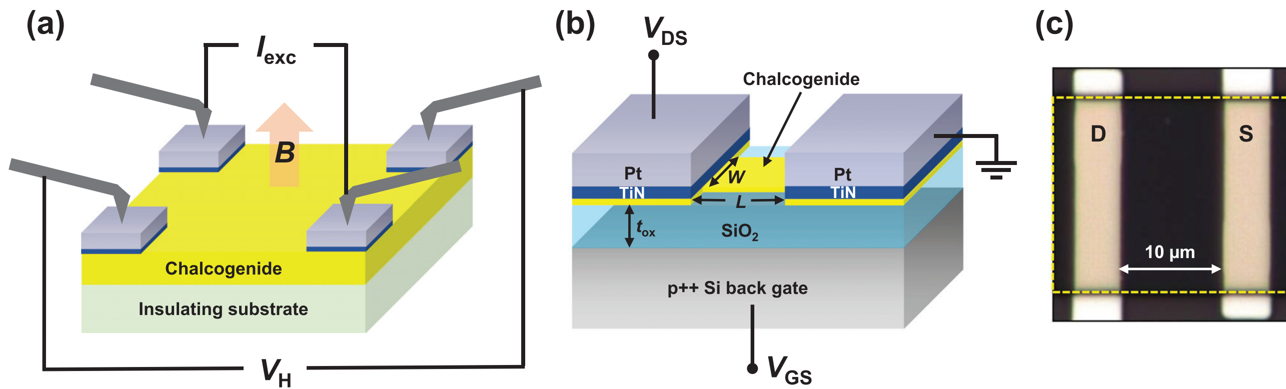

FIG. 1. (a) Schematic of the fabricated van der Pauw Hall measurement structure. (b) Schematic of back-gated transistor structure for field-effect measurements. (c) Top-view optical image of a fabricated transistor. Yellow dashes mark the outline of the chalcogenide channel, here with $L = 10\ \mu m$ and $W = 20\ \mu m$. I_{exc} = excitation current, V_H = Hall voltage, B = magnetic field, V_{DS} = drain–source voltage, V_{GS} = gate–source voltage, L = channel length, W = channel width, t_{ox} = oxide thickness, D = drain, and S = source.

In this work, we investigate the lateral electrical transport properties of ~50 nm thick single-layer Ge, Sb, and Te-based chalcogenide compounds, which include Sb_2Te_3, $Ge_2Sb_2Te_5$, and $Ge_4Sb_6Te_7$, a relatively new composition.[29] We compare their properties with multilayer films (23 and 53 nm total thickness) consisting of Sb_2Te_3/GeTe (4/1 nm/nm) superlattices[28,30] using the Hall effect and transfer length method (TLM) measurements. We also fabricate transistors with ultrathin (4–5 nm) films of Sb_2Te_3, $Ge_2Sb_2Te_5$, and $Ge_4Sb_6Te_7$, as well as bilayer $Sb_2Te_3/Ge_2Sb_2Te_5$ (2/3 nm/nm); all sputtered at ≤180 °C. Then, we draw a comparison among different materials and among devices with or without AlO_x capping. In doing so, we determine the optimized device performance in terms of field-effect mobility (and, thus, on-state current) and the gate modulation capability (the on/off current ratio) of the films.

We start by performing Hall measurements on ~50 nm thin films of Sb_2Te_3, $Ge_2Sb_2Te_5$, and $Ge_4Sb_6Te_7$, as well as multilayer Sb_2Te_3/GeTe stacks, before fabricating back-gated transistors with ultrathin films of these materials. A schematic of the van der Pauw Hall measurement structure is shown in Fig. 1(a), while the schematic and top-view optical images of the fabricated transistors are shown in Figs. 1(b) and 1(c), respectively. The results from Hall effect measurement are summarized in Table I. We also determine the mobility and carrier concentration of the multilayer samples using TLM and find similar values compared to the Hall measurements. The Hall and TLM sample fabrication and measurement parameters are described in the supplementary material (Secs. S1 and S2). We plot these results of mobility vs carrier concentration together with the reported literature[24,31–33] on similar superlattices (Sb_2Te_3/GeTe or $Sb_2Te_3/Ge_2Sb_2Te_5$) as well as Sb_2Te_3, $Ge_2Sb_2Te_5$, and $Ge_6Sb_1Te_2$ thin films (≤100 nm) in Fig. 2. This comparison reveals significant improvement in mobility of multilayer films compared to the single-layer chalcogenides. This can be attributed to the ordering of vacancies and formation of van der Waals-like gaps in the multilayer films,[30,31,34] which can enhance the lateral transport due to improved interfaces.

The Hall measurements also determine p-type conductivity with very high carrier concentration in all thin films, thus forming p-type degenerate semiconductors. This is possibly due to high concentration of Ge or Sb vacancies (in $Ge_2Sb_2Te_5$)[32,35] or Sb_{Te} anti-site defects (in Sb_2Te_3)[36] in the crystalline phases of these materials. The results are in line with the reported literature on $Ge_2Sb_2Te_5$ and Sb_2Te_3 films (as shown in Fig. 2). In this work, we also perform the first Hall measurements on the newly discovered[29] composition $Ge_4Sb_6Te_7$. This material exhibits higher hole concentration, which could be attributed to the lower bandgap of crystalline $Ge_4Sb_6Te_7$; the Hall mobility is also lower, which could be due to the co-existence of mixed-phase (Ge-Sb-Te and Sb-Te) regions, as reported by Kusne *et al.*[29] with high resolution transmission electron microscopy. However, we note that the resistivity (i.e., the inverse of the product of mobility and hole concentration) of the $Ge_4Sb_6Te_7$ film is only ~1.7× higher than that of $Ge_2Sb_2Te_5$ deposited and annealed under similar conditions, as shown in Table I.

TABLE I. Hall measurement data for p-type polycrystalline chalcogenide thin films and superlattices. All measurements are at room temperature in air. Annealing was also performed in air.

Material	Thickness (nm)	Annealing (A) or deposition (D) temperature (°C)	Carrier type	Carrier concentration (cm^{-3})	Hall mobility ($cm^2\ V^{-1}\ s^{-1}$)	Resistivity (Ω·cm)
Sb_2Te_3	50	180 (A)	p	5.1×10^{20}	8.5	1.5×10^{-3}
$Ge_2Sb_2Te_5$	50	180 (A)	p	2.6×10^{20}	6.4	3.8×10^{-3}
$Ge_4Sb_6Te_7$	50	200 (A)	p	8.4×10^{20}	1.2	6.4×10^{-3}
Sb_2Te_3/GeTe	53	180 (D)	p	2.2×10^{20}	16.3	1.8×10^{-3}
Sb_2Te_3/GeTe	23	180 (D)	p	2.1×10^{20}	18.0	1.7×10^{-3}

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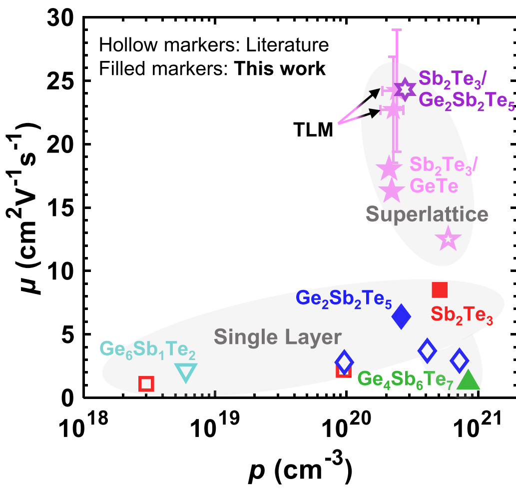

FIG. 2. Plot of hole mobility (μ) vs hole concentration (p) for single-layer and superlattice chalcogenides with $\leq$ 100 nm film thickness.[24,31–33] All data are from Hall measurements, unless otherwise indicated. Error bars in the transfer length method (TLM) data represent standard deviation among four TLM structures with at least six different channel lengths.

Unfortunately, for field-effect transistor applications [Figs. 1(b) and 1(c)], the transistor channel with such high carrier concentrations cannot be easily depleted, which prevents appreciable gate modulation in films with tens of nanometers thickness. In this case, fully depleting the semiconductor with the gate-induced electric field to "turn off" such transistors requires an ultrathin semiconductor channel. Thinning down the material has proven effective for improved gate modulation[24] partially aided by a possible increase in its bandgap at sub-5 nm thickness.[37] Thus, we investigate the behavior of chalcogenide transistors at a reduced thickness of 4–5 nm. We fabricate both single and bilayer channel transistors of two types: uncapped and *ex situ* Al-capped (naturally oxidized to AlO_x, hereafter referred to as AlO_x-capped), where the latter prevents damage to the chalcogenide during contact patterning in optical ultraviolet (UV) lithography (for details see supplementary material Secs. S1 and S3). The devices are annealed at or above their respective crystallization temperatures ($\sim$110 °C for Sb_2Te_3,[4] $\sim$150 °C for $Ge_2Sb_2Te_5$,[1] and $\sim$200 °C for $Ge_4Sb_6Te_7$[29]) to ensure polycrystallinity irrespective of their deposition temperatures.

Figure 3 displays measured drain current (I_D) vs gate voltage (V_{GS}) for the devices with a 10 μm channel length at a drain-source voltage of -1 V. In all cases, the uncapped devices (solid line) have lower on and off-state current ($I_{on} = I_D$ at $V_{GS} = -70$ V; $I_{off} = I_D$ at

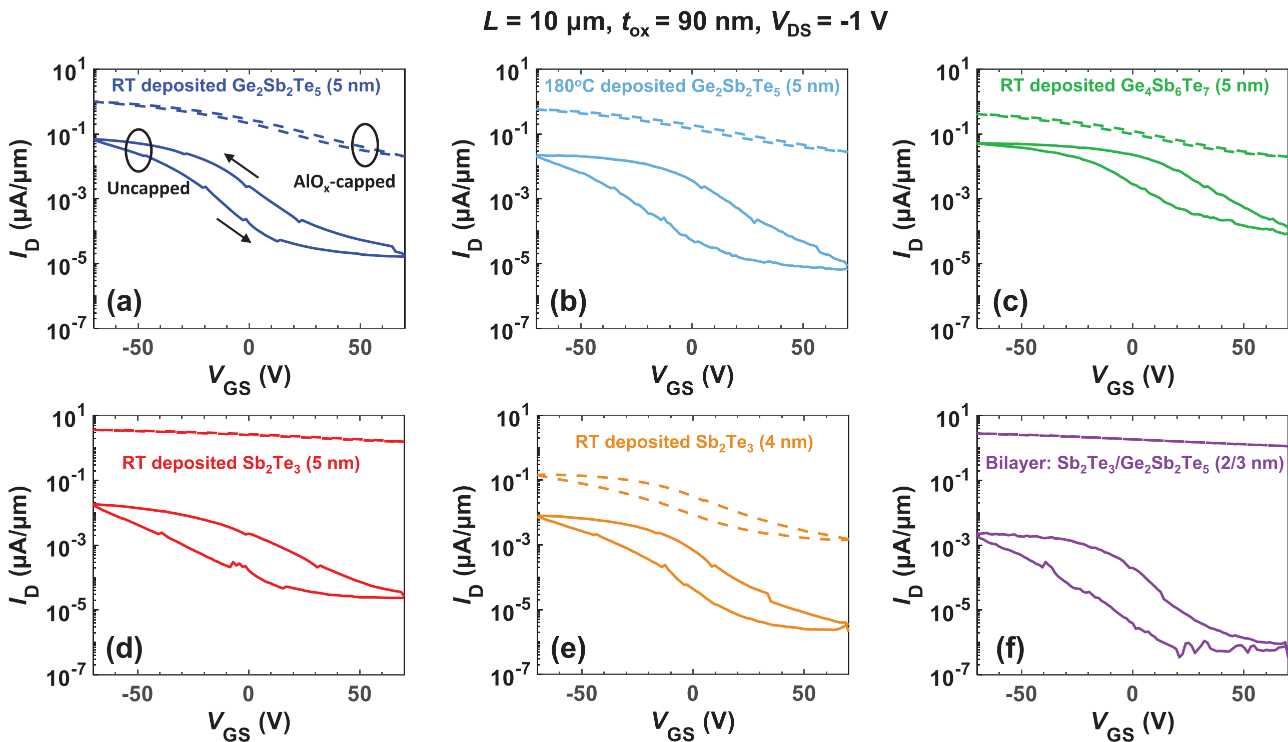

FIG. 3. Measured transfer characteristics (I_D vs V_{GS}) of uncapped (solid line) and AlO_x-capped (dashed line) 5 nm thick (a) $Ge_2Sb_2Te_5$ deposited at room temperature (RT), (b) $Ge_2Sb_2Te_5$ deposited at 180 °C, (c) $Ge_4Sb_6Te_7$ deposited at RT, (d) Sb_2Te_3 deposited at RT, (d) 4 nm thick Sb_2Te_3 deposited at RT, and (f) 5 nm thick bilayer (2 nm Sb_2Te_3/3 nm $Ge_2Sb_2Te_5$) devices. The gate currents of all devices were negligible, below $\sim$0.1 nA/μm. Arrows indicate voltage sweep direction, revealing some hysteresis in these uncapped transistors, measured in air. L = channel length, t_{ox} = oxide thickness, V_{DS} = drain–source voltage.

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$V_{GS} = 70$ V) but better gate modulation compared to the AlO_x-capped devices (dashed line). The lower I_{on} in the uncapped devices may be attributed to the basic photoresist developer partially etching the semiconductor underneath the contact region, leading to partially degraded contacts in these devices. The devices capped with AlO_x, which is intended to circumvent this issue, show improved on-state current, but their on/off current ratio (I_{on}/I_{off}) is lowered drastically mainly due to higher off-state current compared to their uncapped counterparts. Possible reasons for this will be discussed below.

In addition, using a more benign developer can shed more light into the effect of developer solution on the contact region. Both electron-beam lithography (EBL) and deep ultraviolet (DUV) lithography utilize a benign solvent-based developer,[38,39] which is not detrimental to the underlying chalcogenide. As a result, we pattern two of the samples ($Ge_2Sb_2Te_5$ deposited at 180 °C and bilayer Sb_2Te_3/$Ge_2Sb_2Te_5$) with EBL (details in supplementary material Sec. S1) and compare their performance with the devices patterned with UV lithography. The transfer characteristics (I_D vs V_{GS}) and the output characteristics (I_D vs V_{DS}) of the EBL devices patterned with solvent-based developer are shown in Fig. 4. Both devices show similar on/off current ratio as their respective uncapped devices patterned with UV lithography. However, there is a significant improvement in their on-state currents, which is ∼15× for the $Ge_2Sb_2Te_5$ deposited at 180 °C. We attribute the improvement in on-state current to the contact region being unaffected by the developer during the contact patterning process. However, we note that EBL poses processing challenges for some flexible substrates, limited by thermal and radiation tolerances and/or unwanted charging effects.[40] EBL is also not an easily scalable manufacturing technique; therefore, the use of optical lithography on such chalcogenides should be carefully considered based on the type of substrate, developer solution, etc.

To gain more insights, Fig. 5 compares the on-state current and field-effect mobility (μ_{FE}) of different materials vs the on/off current ratio. Overall, the uncapped samples show higher on/off ratio, whereas the AlO_x-capped samples have lower on/off ratio, as shown by the two shaded regions in Fig. 5. While EBL patterned uncapped samples (triangle symbols) show improved on-state current compared to uncapped devices patterned with UV lithography (circle symbols), the

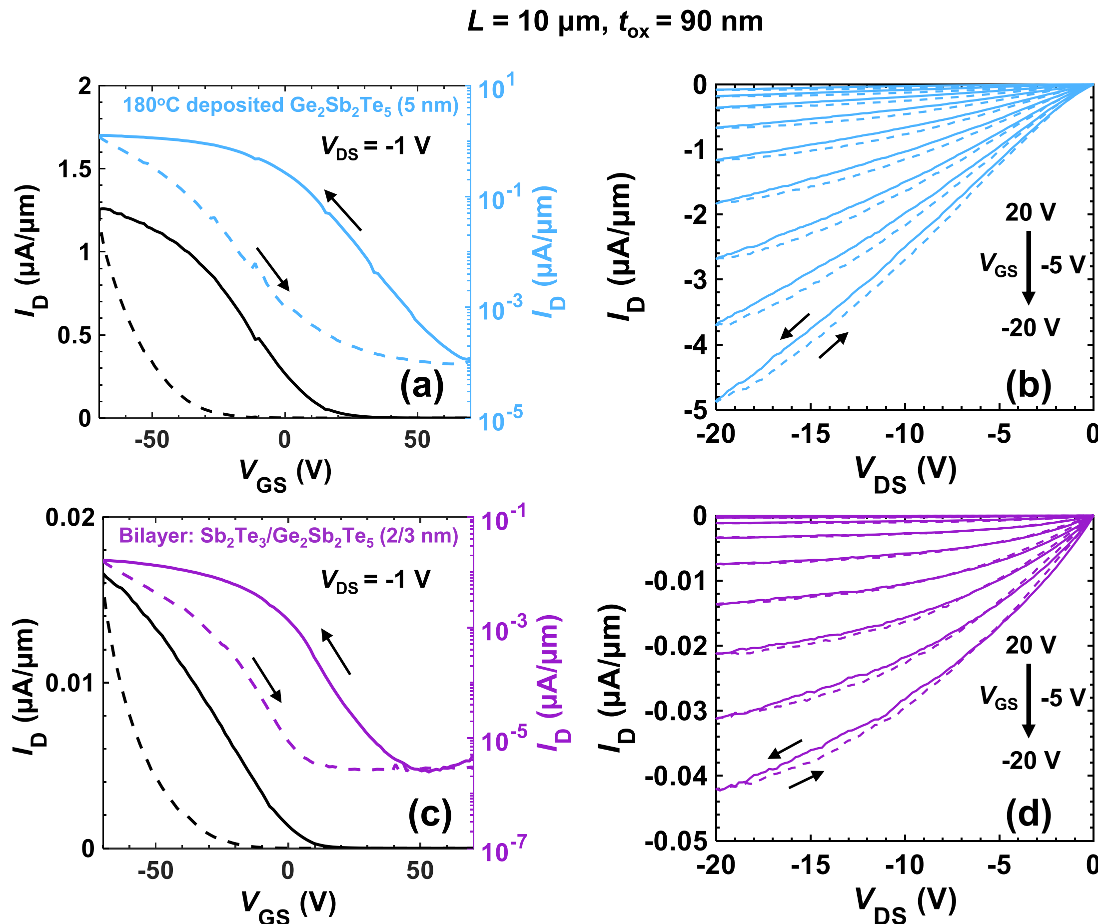

FIG. 4. Measured (a) transfer and (b) output characteristics of uncapped 5 nm thick $Ge_2Sb_2Te_5$ deposited at 180 °C. This represents a "hero" device, with field-effect mobility $\mu_{FE} \approx 5.5\ cm^2\ V^{-1}\ s^{-1}$ at room temperature. Measured (c) transfer and (d) output characteristics of a bilayer (2 nm Sb_2Te_3/3 nm $Ge_2Sb_2Te_5$) device. Both devices were patterned with electron-beam lithography (EBL). Small arrows represent voltage sweep directions. Note linear and logarithmic scales in (a) and (c).

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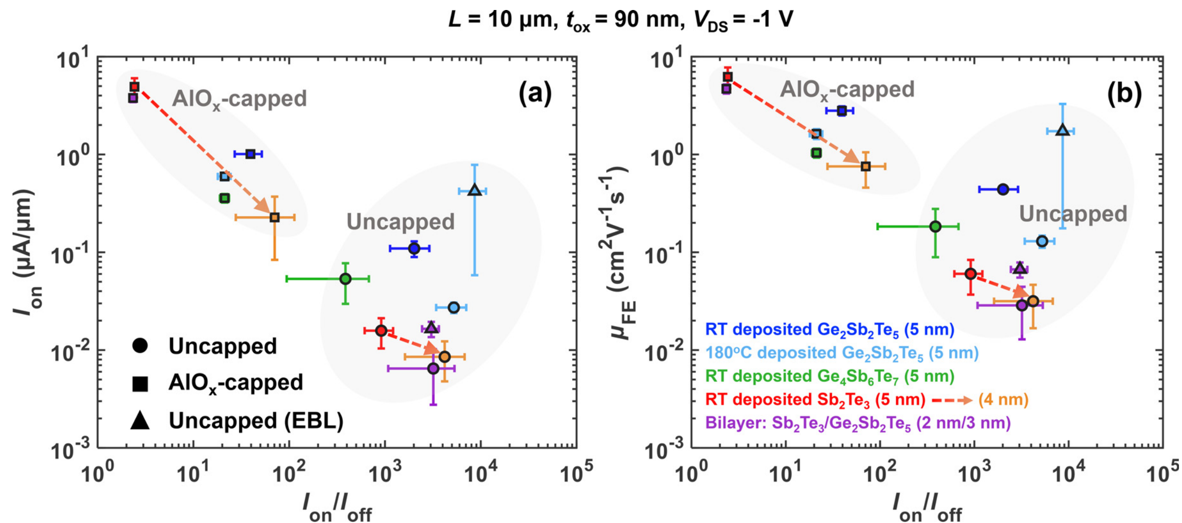

FIG. 5. Plot of our measured (a) on-state current (I_{on}) and (b) field-effect mobility (μ_{FE}) vs on/off current ratio (I_{on}/I_{off}) for various fabricated transistors. RT = room temperature, EBL = electron-beam lithography; Error bars represent standard deviation among 5–10 devices.

AlO_x-capped samples (square symbols) still show significantly higher on-state current. This indicates an additional phenomenon responsible for higher on-state current in the AlO_x-capped devices. Here, we observe a simultaneous increase in both on-state and off-state current, indicating higher mobility and/or carrier concentration, which could be attributed to possible Al diffusion into the chalcogenide film[41] or an interfacial doping effect.[42,43] In order to understand this, we perform x-ray diffraction (XRD) analysis on uncapped and AlO_x-capped $Ge_2Sb_2Te_5$ (20 nm thick), noting enhanced crystallization peaks in the sample capped with 2 nm AlO_x (see supplementary material Sec. S4). This is possibly due to Al-induced crystallization of the $Ge_2Sb_2Te_5$ film, a common phenomenon for amorphous silicon[44,45] and germanium.[46] This enhanced crystallinity of the films is also in agreement with the higher on-state current in the AlO_x-capped devices.

The effect of reducing the channel thickness is also shown in Fig. 5 with a dashed arrow. We fabricate both uncapped and AlO_x-capped Sb_2Te_3 samples with thinner sputtered channels (4, 3, and 2 nm) in order to improve the gate modulation. The 4 nm thick Sb_2Te_3 sample (shown in Fig. 5) expectedly shows higher on/off ratio but lower on-state current because there is a trade-off when scaling down the thickness. The 3 and 2 nm samples showed very low on-state current and, hence, are not included in the plot. The lowering of mobility is possibly caused by increased carrier scattering at reduced channel thickness.[37] As a result of such degradation at lower sputtered thicknesses, we kept our investigation of other materials down to 5 nm thick channels.

Interestingly, we do not observe improved performance for the bilayer $Sb_2Te_3/Ge_2Sb_2Te_5$ transistor compared to its single-layer counterparts, as was indicated by the Hall and TLM measurements of thicker (23 and 53 nm) superlattice stacks. This could be because the bilayer sample was fabricated with a thickness limited to 5 nm in order to achieve appreciable gate modulation. It should be noted that the bilayer and superlattice structures are fabricated by first depositing a seed layer (Sb_2Te_3) at room temperature before the subsequent chalcogenide deposition(s) at high temperature. This leads to highly oriented crystalline layers with van der Waals-like gaps as reported in the literature.[27,30,47] As a result, the multilayer stacks can have improved interfaces between the high-temperature deposited chalcogenide layers, following the first interface with the seed layer. On the other hand, the only interface in the bilayer sample is between the seed layer and the high-temperature deposited layer. The top layers and/or interfaces could be responsible for facilitating the lateral transport in the thicker superlattices, and thus, the improvement is not observed in the bilayer sample. Moreover, the superlattice stack is formed with thicker Sb_2Te_3 layers (both as a seed layer and in subsequent sub-layers) in contrast to using only a 2 nm Sb_2Te_3 seed layer in the bilayer sample, which could have a distinct role in crystallization of the subsequent layer(s).[47]

Overall, we achieve the most optimized performance for our p-channel transistors with 5 nm $Ge_2Sb_2Te_5$ deposited at 180 °C, patterned with benign solvent-based developer. A cross-sectional scanning electron microscopy (SEM) image of an optimized device and the corresponding channel thickness measured with atomic force microscopy (AFM) are shown in supplementary material Fig. S4. Our "hero" device reaches $I_{on} \approx 1.26\,\mu A/\mu m$ at $V_{DS} = -1$ V and $\mu_{FE} \approx 5.5\,cm^2\,V^{-1}\,s^{-1}$, with $I_{on}/I_{off} \approx 10^4$, and is shown in Figs. 4(a) and 4(b). The average devices have $I_{on} \approx 0.42\,\mu A/\mu m$ at $V_{DS} = -1$ V and $\mu_{FE} \approx 1.7\,cm^2V^{-1}s^{-1}$, with $I_{on}/I_{off} \approx 8640$, and the data measured on all such devices are summarized in supplementary material Fig. S5. (All transistors have $L = 10\,\mu m$ and are not limited by their contact resistance.[48]) The only other study in the literature,[24,25] which reports Ge, Sb, and Te-based chalcogenide thin film transistors below 10 nm thickness, is for as-deposited (amorphous) $Ge_2Sb_2Te_5$ films, which show the on-state current and the field-effect mobility of $\sim$0.01 $\mu A/\mu m$ and $\sim$ 0.04 $cm^2\,V^{-1}\,s^{-1}$, respectively, with I_{on}/I_{off} up to 388. Notably, their annealed (crystalline) films at 5 nm thickness showed deteriorated performance, which was attributed to a degradation of the contact and surface area during annealing.[24] In comparison, our hero (average) device shows $\sim$140$\times$ ($\sim$40$\times$) improvement in field-effect mobility, and nearly 30$\times$ improvement in on/off current ratio. A comparative analysis of our work with relevant material systems

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using BEOL-compatible large-scale deposition methods is illustrated in supplementary material Table S2.

In conclusion, we have shown that it is possible to obtain p-channel transistors with a mobility of 5.5 cm^2 V^{-1} s^{-1} and an on/off current ratio of $\sim 10^4$ at room temperature, using 5 nm thick $Ge_2Sb_2Te_5$ films sputtered at 180 °C, a deposition process, which is compatible with both flexible substrates and BEOL integration. This is important, because there are very few p-channel transistor options,[10,49,50] as the majority of chalcogenide or oxide transistors are known to be n-type.[51,52] We also find hole Hall mobility up to 18 cm^2 V^{-1} s^{-1} in 23 nm thick Sb_2Te_3/GeTe superlattices and field-effect mobility up to 6.2 cm^2 V^{-1} s^{-1} in 5 nm thick Sb_2Te_3 capped with AlO_x, at room temperature. These results are also important for further optimization of emerging phase-change memory structures, where both electrical and thermal material properties play a crucial role. Future work must continue to optimize such chalcogenide thin films, e.g., by atomic layer deposition (ALD) or controlled thinning of the channel region of thicker deposited films, which could lead to further improvement in gate modulation with minimal degradation in mobility. The addition of thin high-κ dielectrics or double-gates could also improve the on/off current ratio of such p-type transistors.

See the supplementary material for details about sample fabrication, measurement, and characterization.

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AUTHOR DECLARATIONS

Conflict of Interest

The author have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Supplementary Material

Lateral Electrical Transport and Field-Effect Characteristics of Sputtered P-Type Chalcogenide Thin Films

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S1. Fabrication Details

I. Van der Pauw Hall Measurement Structures

We fabricate van der Pauw structures for Hall measurements by depositing chalcogenide thin films on insulating substrates (sapphire, or 450 nm SiO_2 on Si). For this, we deposit ~50 nm thick single layer films of Sb_2Te_3, $Ge_2Sb_2Te_5$ and $Ge_4Sb_6Te_7$ at room temperature by direct current (DC) and/or radio frequency (RF) magnetron sputtering using an AJA ATC 1800-F sputtering system (details in Table S1). Then, we sputter four metal contacts of TiN (10-20 nm)/Pt (40-50 nm) on the corners of the sample using a shadow mask. The films are then annealed *ex situ* for ~30 minutes in air on a hot plate at a temperature of 180ºC for Sb_2Te_3 and $Ge_2Sb_2Te_5$ and 200ºC for $Ge_4Sb_6Te_7$, at or above their respective crystallization temperatures.[1-3] Other than films with a single type of chalcogenide, we also investigate the transport properties of multilayer chalcogenide films of Sb_2Te_3/GeTe. For this, we first deposit a 3 nm thick Sb_2Te_3 seed layer at room temperature, which is annealed *in situ* at 180ºC before depositing alternating stacks of GeTe (1 nm) / Sb_2Te_3 (4 nm) at 180ºC without breaking vacuum (~10^{-7} Torr). It has been reported in literature that such seed layers enable the deposition of crystalline and layered films in superlattice stacks.[4-6] We fabricate two samples of such chalcogenide superlattices with total 4 and 10 periods, thus making 23 and 53 nm thick multilayer films, respectively.

TABLE S1. Parameters used for sputtering

Material	Power (W)	Deposition Pressure (mTorr)	Ar flow (sccm)	Rate (nm/min)
$Ge_2Sb_2Te_5$	12 (DC)	2	20	5.6
$Ge_4Sb_6Te_7$	12 (DC)	2	20	6.0
Sb_2Te_3	30 (RF)	4	30	1.2
GeTe	30 (RF)	4	30	2.4

*sccm: standard cubic centimeters per minute

II. Back-gated Field-Effect Transistor Structures

A schematic diagram illustrating the basic steps of transistor fabrication process is shown in Fig. S1. Single and bilayer material transistors are fabricated on 90 nm thick SiO_2 on a degenerately doped p++ silicon substrate which is used as the back-gate electrode. The SiO_2 back-gate dielectric is formed through dry thermal oxidation of the substrate. For both uncapped and AlO_x-capped devices, we deposit the single layer chalcogenide film (4 to 5 nm) at room temperature or an elevated temperature (180ºC) using DC and/or RF magnetron sputtering (details in Table S1). For the bilayer films, 2 nm Sb_2Te_3 is deposited at room temperature as a seed layer, followed by a deposition of 3 nm $Ge_2Sb_2Te_5$ at 180ºC. In case of AlO_x-capped devices, an *ex-situ* deposition of ~2 nm Al is done on top of the chalcogenide using electron beam

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evaporation. The deposited Al layer is then allowed to immediately oxidize in air forming an AlO_x capping layer on the semiconductor.

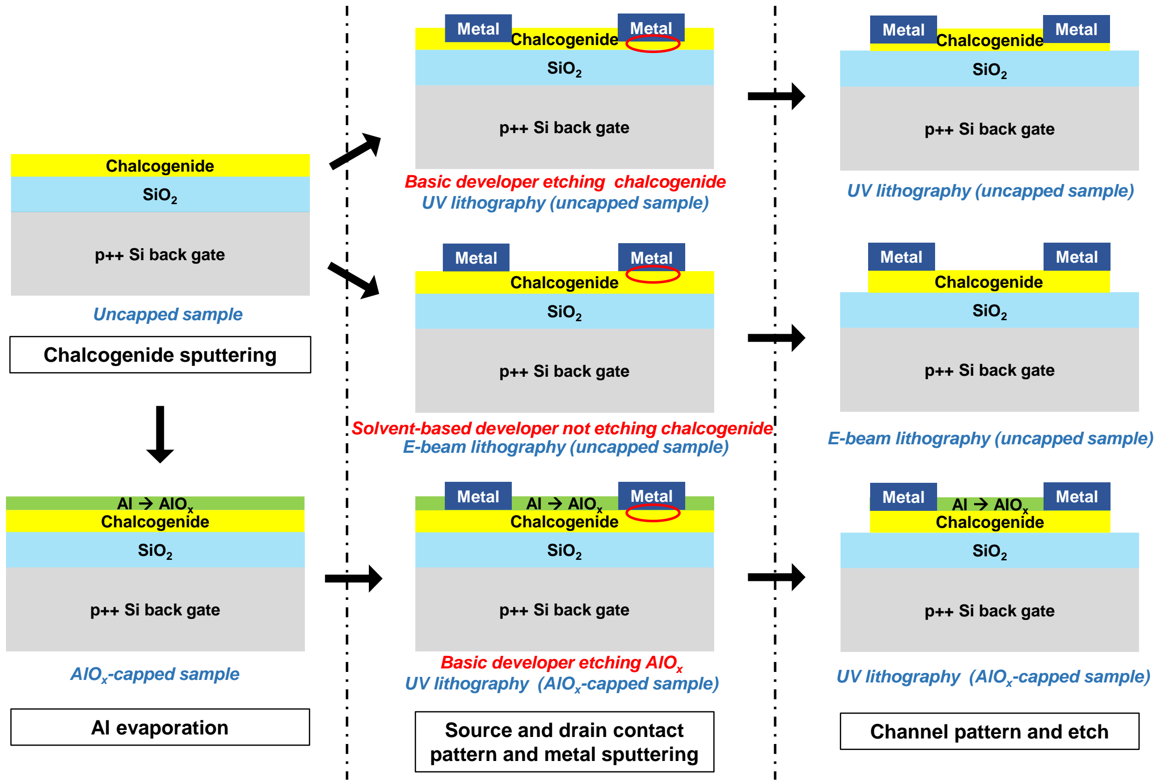

FIG. S1. A schematic illustration of the fabrication process flow.

Next, we define the source and drain metal contacts by optical ultraviolet (UV) lithography in all the samples. In this step, LOL-2000 is used as the lift-off layer (generating an undercut in the resist stack), which is baked at 180ºC for 5 minutes; then, SPR-3612 is used as the photoresist layer (baked at 90ºC for 1 min). The baking step above the crystallization temperatures of Sb_2Te_3 and $Ge_2Sb_2Te_5$ ensures that our investigated films are polycrystalline even in case of a room-temperature deposition. The $Ge_4Sb_6Te_7$ sample, which has a higher crystallization temperature (~200ºC),[3] is later annealed on a hot plate in air at 200ºC for ~30 minutes to ensure polycrystalline film formation. After resist baking, the samples are exposed to 405 nm wavelength laser using a direct write lithography tool (Heidelberg MLA150). Microposit MF-26A, an aqueous developer containing TMAH, is used to develop the pattern in 30-40 sec., which needs to be handled carefully because such developer can attack the underlying semiconductor film (see Section S3).

For two of the samples (180ºC deposited $Ge_2Sb_2Te_5$ and bilayer $Sb_2Te_3/Ge_2Sb_2Te_5$), we also employ electron-beam lithography (EBL) to define the source and drain contacts. Polymethyl methacrylate (PMMA) 495K A2 (lift-off layer) followed by PMMA 950K A4 form the resist stack (each baked at 180ºC for 5 minutes) for the lift-off process in EBL. The JEOL JBX-6300 electron-beam lithography tool is used to expose the samples to electron beam with a dose of 800 μC cm^{-2}, and current of 4 nA (fine contact regions) or 9 nA (etch regions for channel patterning). Then we use a 1:1 solution of methyl isobutyl ketone (MIBK) : isopropyl alcohol (IPA) for 30 seconds for pattern development. This is a solvent-based developer which shows no sign of chalcogenide etching. For all the samples, with the exception of room temperature deposited $Ge_2Sb_2Te_5$, a bilayer metal stack of TiN (10-20 nm) / Pt (40-50 nm) is then sputtered and lifted-off to form the source and drain metal pads. For the room temperature deposited $Ge_2Sb_2Te_5$ an e-beam evaporated Ge/Ni/Au (5 nm/5 nm/30 nm) stack is used as contacts.[7,8] Note, because we investigate long

channel devices (10 μm), the transistors are not limited by their contact resistance[9] and the difference in contact materials does not significantly affect our results. Finally, the chalcogenide channel region is patterned with UV lithography and reactive ion etching, 10 mTorr pressure using CF_4, CH_4 and Ar gases at 60 W bias RF forward power and 400 W ICP RF forward power.

S2. Electrical Measurements

The Hall measurements are performed using a Lakeshore 8404 Hall Measurement tool, applying an excitation current (I_{exc}) of 0.1 mA and a DC magnetic field (B) of 0.5 T. The electrical measurements for TLM and transistor devices are done at room temperature in air using a probe station combined with a Keithley 4200-SCS. The TLM measurements were done at V_{DS} = -1 V and the parameters were extracted at V_{GS} = 0 V. In all the TLM and transistor measurements, the gate current did not exceed ~0.1 nA/μm, which is significantly lower than the measured on-state current of the devices.

S3. Atomic Force Microscopy (AFM) to determine etching by photoresist developer

During the UV lithography process, the thickness of the chalcogenide etched by the MF-26A developer is determined by measuring the step height from the non-contact atomic force microscope (AFM) images, captured using Asylum AFM MFP-3D (Fig. S2). The numbers, however, may vary because the samples are developed manually, and the rate of agitation or stirring is not identical for all three samples. Nonetheless, because pattern development takes at least 20 to 25 sec. (to wash away the photoresist in the developed regions), the total development time had to be ~30 to 40 sec. to ensure reliable pattern development throughout the chip. During this time, the chalcogenide thickness etched by the developer is ~1.2, 1.6 and 2.1 nm in 30 seconds of total development time for $Ge_2Sb_2Te_5$, $Ge_4Sb_6Te_7$ and Sb_2Te_3, respectively.

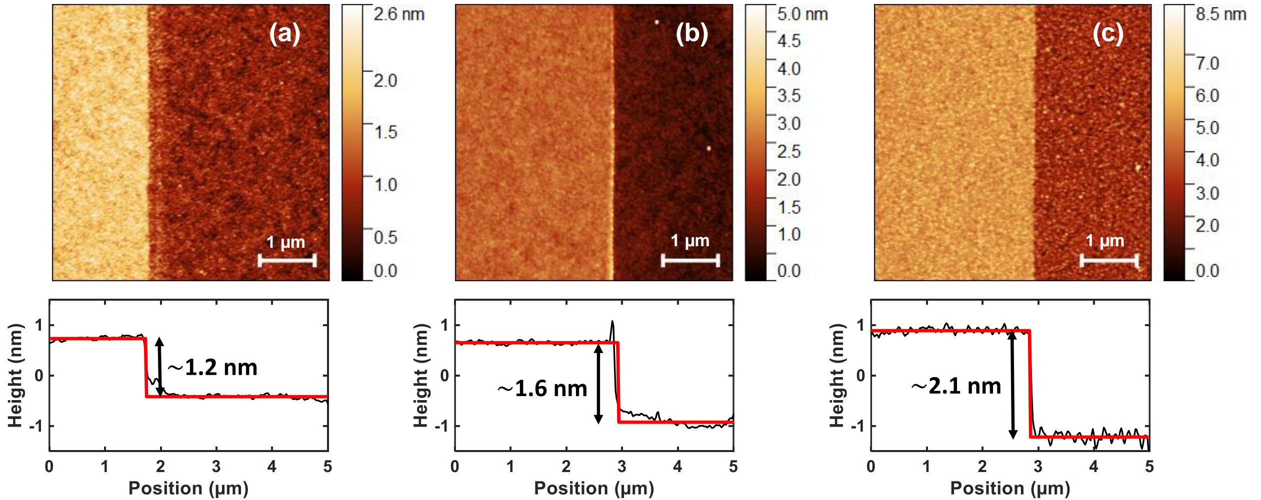

FIG. S2. Atomic force microscope (AFM) images along with respective step heights across the edges of (a) $Ge_2Sb_2Te_5$, (b) $Ge_4Sb_6Te_7$, and (c) Sb_2Te_3 samples etched by MF-26A developer.

S4. X-Ray Diffraction (XRD)

For X-Ray diffraction analysis, we prepare two samples where 20 nm thick $Ge_2Sb_2Te_5$ films are deposited at room temperature. One of the samples is capped with 2 nm thick e-beam evaporated Al (naturally oxidized to AlO_x) and then both samples are baked at 180ºC for 5 min. in air to mimic the lithography baking steps. Next, we perform the XRD tests using PANalytical X'Pert 2 diffractometer with a Cu Kα (λ = 0.154056 nm) radiation source, aligned to the silicon (400) plane. Figure S3 displays increased intensity

in the crystallization peaks of the AlO_x-capped sample (magenta solid line) compared to the uncapped sample (blue dashed line), showing enhanced crystallization in the AlO_x-capped film.

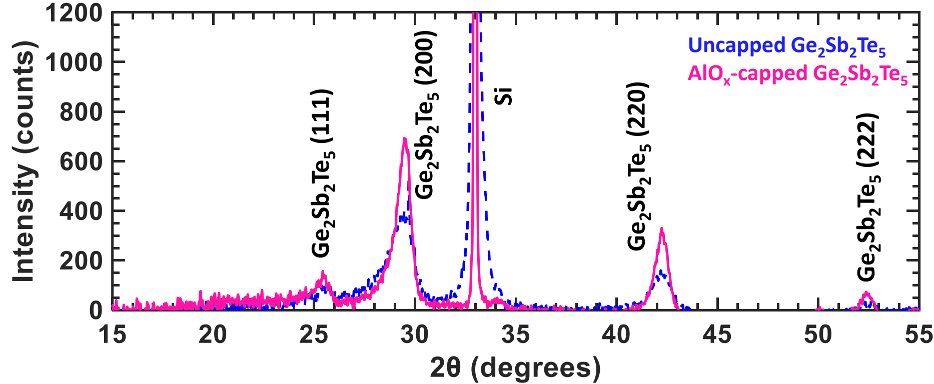

FIG. S3. X-Ray diffraction analysis on uncapped and AlO_x-capped 20 nm thick $Ge_2Sb_2Te_5$ samples deposited at room temperature.

S5. Scanning Electron Microscopy (SEM) and AFM for channel thickness

We perform cross-sectional scanning electron microscopy (SEM) on a device from the $Ge_2Sb_2Te_5$ sample deposited at 180ºC and patterned with e-beam lithography, showing the cross-section under the contact region. Figure S4(a) clearly shows the SiO_2 gate dielectric and Pt contact layer on the Si substrate whereas the TiN contact layer and the $Ge_2Sb_2Te_5$ channel are seen in the zoomed inset. A FEI Helios NanoLab 600i DualBeam Focused Ion Beam (FIB) and SEM is used to take the cross-sectional image at 20 kV accelerating voltage and 0.17 nA probe current. Park XE-100 scanning probe microscopy is used to get the non-contact AFM image of the channel using NSC15/Al BS tips. The corresponding step height confirms the channel thickness to be 5.3 ± 0.4 nm (denoted as ~5 nm). The error range of the thickness is a fitting error for the step profile. The spike at the edge of the channel is due to hardened residual resist from the dry etch.

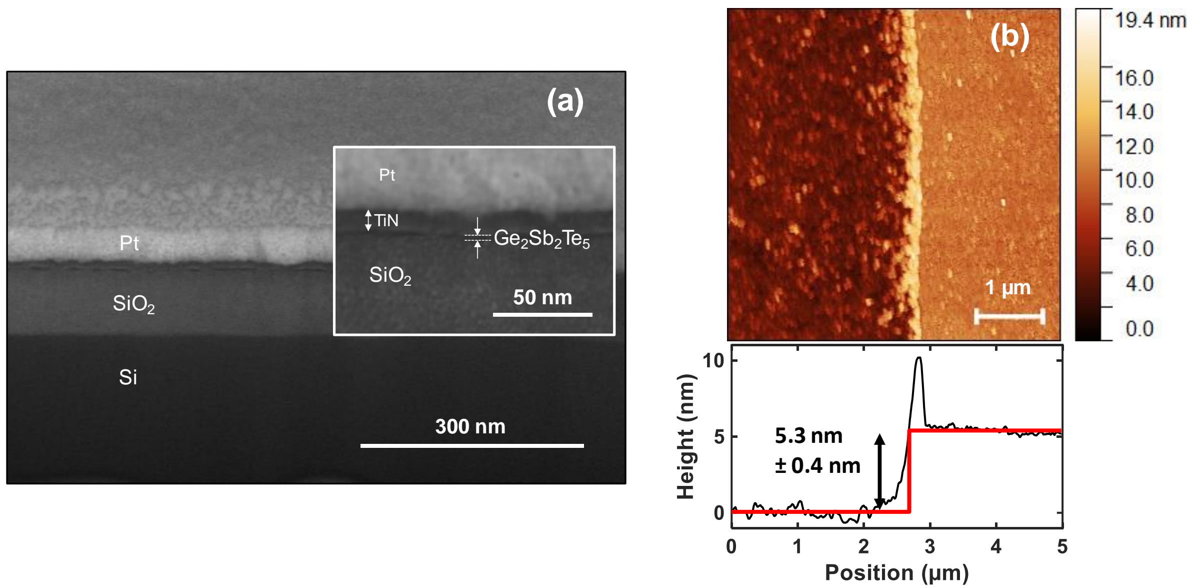

FIG. S4. (a) Cross-sectional scanning electron microscopy (SEM) image of the device underneath the contact, with zoomed view in the inset taken at a 52º angle tilt. (b) Atomic force microscope (AFM) image along with step height showing the channel thickness.

S6. Bar graphs of $Ge_2Sb_2Te_5$ transistor measurements

The data for field-effect mobility (μ_{FE}), on-state current (I_{on}) and current on/off ratio (I_{on}/I_{off}) in the 11 measured transistors for $Ge_2Sb_2Te_5$ deposited at 180ºC and patterned with solvent-based developer, are illustrated in Fig. S5. I_{on} refers to I_D at V_{GS} = -70 V and I_{off} refers to I_D at V_{GS} = 70 V. All transistors have L = 10 µm and are measured at V_{DS} = -1 V.

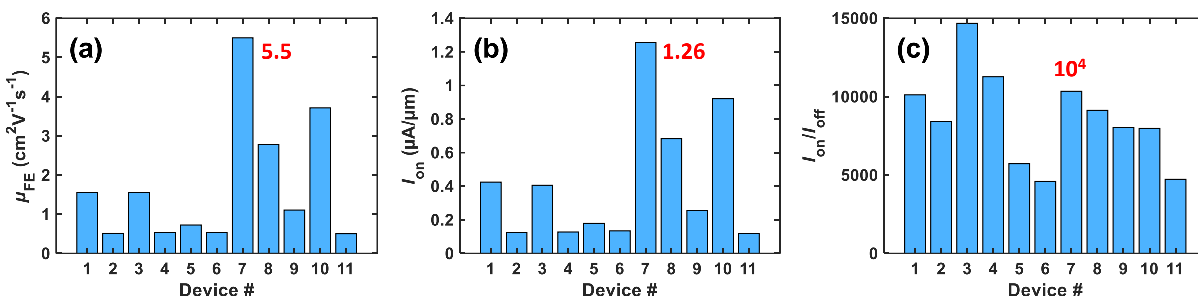

FIG. S5. (a) Field-effect mobility (μ_{FE}), (b) on-state current (I_{on}) at V_{DS} = -1 V, and (c) current on/off ratio (I_{on}/I_{off}) for different devices in the $Ge_2Sb_2Te_5$ sample deposited at 180ºC and patterned with solvent-based developer. Device # 7 (marked by the red label) represents the 'hero' device mentioned in the main text. The average values are: $\mu_{FE} \approx 1.7$ cm^{2}V^{-1}s^{-1}, $I_{on} \approx 0.42$ µA/µm at V_{DS} = -1 V, and $I_{on}/I_{off} \approx 8640$.

S7. Comparison table of BEOL-compatible p-FETs based on chalcogenide compounds

Table S2 compares our data for $Ge_2Sb_2Te_5$, Sb_2Te_3 and $Ge_4Sb_6Te_7$ with reported studies of similar chalcogenide compounds, deposited at a BEOL-compatible temperature (≤ 500ºC) using industrial-scale methods. The average values of I_{on}, μ_{FE}, and I_{on}/I_{off} are mentioned for all three materials whereas the 'hero' device for the most optimized sample is presented in parentheses.

Table S2: Comparison of p-type FETs with chalcogenide compounds achieved using BEOL-compatible, large-scale deposition methods

Deposition method*	**Temp. (ºC)#**	**Channel Material**	**Channel thickness (nm)**	**L (µm)**	**I_{on} at V_{DS} = -1 V (µA/µm)**	**μ_{FE} (cm^{2}V^{-1}s^{-1})**	**I_{on}/I_{off}**	**Ref.**
Co-sputt.	-	c-$Ge_2Sb_2Te_5$	80	30	~120	-	13.68	10
Sputt.	135 (A)	c-$Ge_2Sb_2Te_5$	10	0.4	~0.003	-	3.67	11
Sputt.	300 (A)	c-$Ge_2Sb_2Te_5$	50	2	~0.006	-	~20	12
DC mag. sputt.	RT (D)	a-$Ge_2Sb_2Te_5$	5	10	0.01	0.04	388	7
	200 (A)	c-$Ge_2Sb_2Te_5$	10	10	1.3	6.72	16	7
Seleniz.	450 (P)	$PdSe_2$	8	6000	5.3×10^{-4}	~7.9	~5	13
CVD	500 (G), 300 (A)	$PtSe_2$	1.6	-	-	13.86	40	14
PLD	300 (A)	ZnTe	75	20	1.75×10^{-3}	0.01	~2.3	15
DC mag. sputt.	180 (D)	c-$Ge_2Sb_2Te_5$	5	10	0.42 (1.26)	1.7 (5.5)	8640 (~10^4)	This work†
RF mag. sputt.	180 (A)	c-Sb_2Te_3	5	10	0.016	0.06	914	This work
DC mag. sputt.	200 (A)	c-$Ge_4Sb_6Te_7$	5	10	0.05	0.18	387	This work

* Sputt. = sputtering; mag. = magnetron; seleniz. = selenization; CVD = chemical vapor deposition; PLD = pulsed laser deposition; DC = direct current; RF = radio frequency
# A = Annealing; D = Deposition; P = Processing; G = Growth
† Hero device is shown in parentheses

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